

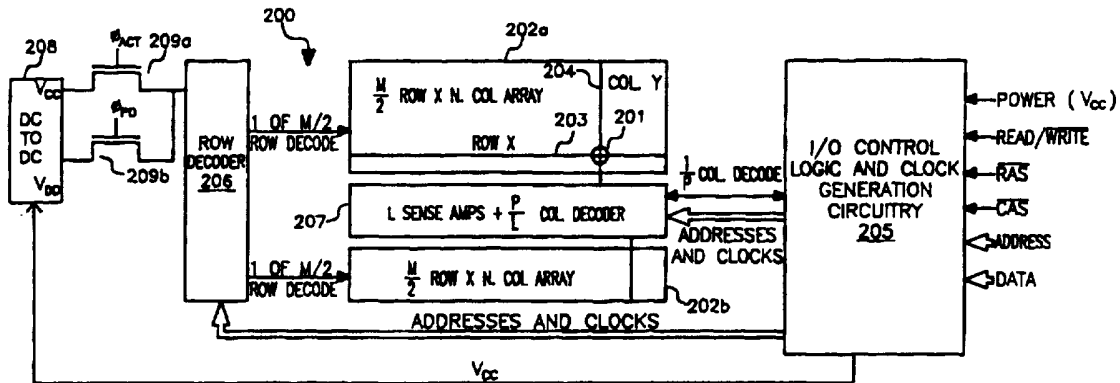


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(54) Title: CIRCUITS, SYSTEMS AND METHODS FOR IMPROVING ROW SELECT SPEED IN A ROW SELECT MEMORY DEVICE



(57) Abstract

A memory device (200) is provided which includes an array (202) of rows and columns of memory cells (201). Row decoder circuitry (206) is provided for selecting a given row of cells (201) for access. Circuitry (208, 209) is included for providing a selected one of a plurality of supply voltages to the row decoder circuitry (206), a first positive voltage provided during an active state of the row decoder circuitry (206) and a second positive voltage provided during an inactive state of the row decoder circuitry (206).

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 96/01351

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G11C11/408

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 498 251 (IBM CO.) 12 August 1992 see abstract see column 3, line 35 - column 4, line 50; figure 1 ---	1,6,11, 16,19
A	US,A,3 621 302 (PRICER) 16 November 1971 see abstract see column 2, line 47 - column 4, line 32; figures 1-3 -----	1,6,11, 16,19

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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Information on patent family members

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