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(54) **Title:** STATISTICAL DELAY AND NOISE CALCULATION CONSIDERING CELL AND INTERCONNECT VARIATIONS

(57) **Abstract:** The electrical circuit timing method provides accurate nominal delay together with the delay sensitivities with respect to different circuit elements {e.g., cells, interconnects, etc.) and variational parameters (e.g., process variations; environmental variations). All the sensitivity computations are based on closed-form formulas; as a consequence, the method provides rapidly and at low cost high accuracy and high numerical stability.

Title

STATISTICAL DELAY AND NOISE CALCULATION CONSIDERING CELL AND INTERCONNECT VARIATIONS

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RELATED APPLICATIONS

[001] This application claims priority from US provisional application 60/663,219, filed March 18, 2005, and the contents of which are incorporated in their entirety as if fully set forth herein.

GOVERNMENT FUNDING

[002] Not applicable.

BACKGROUND

Field of the Invention

[003] The invention generally relates to the field of integrated circuit design performance analysis and optimization, and particularly to the delay and crosstalk noise calculation for logic cells used in statistical static timing analysis of digital integrated circuit.

Description of the Related Art

[004] In modern very large-scale integrated circuit (VLSI) design, it is very important to improve the circuit operating speed and to verify if the circuit can perform at a target frequency. To achieve these goals, circuit designers extensively use timing verification and optimization software from Electronic Design Automation (EDA) vendors on their designs. Two main methodologies for timing verification are used: 1) transistor-level simulation based method and 2) cell/gate-level static timing analysis. The transistor-level simulation method can accurately simulate the circuit timing behavior, but this method is very time-consuming and is not feasible for a full-chip analysis. Static timing analysis provides a fast method to estimate circuit timing performance, and can be used for full-chip analysis.

[005] In VLSI digital circuits, logic cells are the basic building blocks; logic cells are interconnected with metal wires. In static timing analysis, logic cell delay models are becoming more and more complicated as semiconductor technologies evolve. Prior to the 1980s, cell delays could be modeled as a constant number. During the 1980s, CMOS technologies were widely used, and cell delays became a function of input transition time and load capacitance. Early in the 1990's, due to interconnect scaling, logic cell delays became a function of gate and RC (resistance capacitance) interconnect loading. In the early 2000s, the increased thickness of metal wire (relative to the feature size) has resulted in strong coupling capacitance between different interconnects; and logic cell delay has become a function of coupling interconnect (*i.e.,* crosstalk).

[006] Moreover, the further decrease in feature sizes for nanoscale CMOS technologies increases the importance of process variations. These variations

introduce uncertainty in circuit behaviors and significantly impact the circuit performance and product yield. The increased variability has given a new set of problems for circuit timing analysis. However, current delay calculation methods do not handle process and environmental variations from both cells and interconnects. The corner-based methodology for worst-case analysis traditionally used in static timing analysis may be overly pessimistic as well as extremely inaccurate. A better circuit timing methodology is needed to more accurately account for circuit behavior as it is influenced by process variations.

[007] Attempts to solve the statistical timing analysis problem can be largely be categorized as being in one of two approaches: either a path-based approach or a block-based approach. (*See* J. A. G. Jess and K. Kalafala et al, "Statistical timing for parametric yield prediction of digital integrated circuits", Design Automation Conference (DAC), pp. 932-937, June 2003; H. Chang and S. S. Sapatnekar, "Statistical Timing Analysis Considering Spatial Correlations using a Single Pert-like Transversal", ICCAD 2003, pp. 621-625, Nov 2003; Aseem Agarwal, David Blaauw, Vladimir Zolotov and Sarma B. K. Vrudhula, "Statistical Timing Analysis Using Bounds", DATE 2003, pp. 10062-10067; Anirudh Devgan and Chandramouli Kashyap, "Block-based Static Timing Analysis with Uncertainty", ICCAD 2003, November 2003; Jiayong Le, Xin Li and L. Pileggi, "STAC: statistical timing analysis with correlation," IEEE Design Automation Conference, 2004).

[008] However, both path based and block based approaches focus not on delay calculation but on high level timing propagation problems wherein the delay is assumed (based on a simple model) rather than calculated. With the decreasing of feature size in semiconductor technology, statistical cell delay can no longer be modeled as a simple value or function. The non-linear input waveform, the metal

interconnect resistiveness, and non-linear receiver capacitance all have strong effects on cell delay. While some of these factors are accounted for in nominal delay calculation techniques, other factors have yet to be modeled. Process variations cause these factors to have statistical distributions. Consequently, all nominal delay calculation approaches (such as, for example, the effective capacitance method) are not currently able to capture statistical information accurately. A statistical delay calculation methodology is needed for greater accuracy in statistical timing analysis.

[009] Crosstalk between nanoscale size features also complicates statistical timing analysis. At nanoscale feature sizes, the dominant portion of wiring capacitance is the inter-layer neighboring wire capacitance. Consequently, the delay of a gate can be greatly impacted by the switching activity on neighboring wires (see R. Arunachalam, K. Rajagopal and L. Pileggi, :TACO: Timing Analysis with Coupling" Proceedings of the Design Automation Conference, pp. 266-269, June 2000). Accounting for this cross-talk effect, therefore, is a critical part of the statistical timing analysis process.

[0010] The "crosstalk effect" becomes significant when the coupling capacitance between adjacent interconnects increases. A coupled interconnect system includes a victim net and several aggressor nets. For a good discussion of coupled interconnect systems, see R. Arunachalam, K. Rajagopal and L. Pileggi, :TACO: Timing Analysis with Coupling" Proceedings of the Design Automation Conference, pp. 266-269, June 2000- which is incorporated by reference as if fully set forth herein. A net is a set of nodes resistively connected. A net has one driver node, one or more fanout nodes, and may have a number of intermediate nodes that are part of the interconnect. "Fanout" is the ability of a logic gate to drive further logic gates; fanout refers to or is quantified by referring to the number of gates before voltage falloff causes errors.

[0011] An "aggressor net" is a net that has significant coupling capacitance to the

victim net so as to be able to influence the delay of the victim gate. A gate is a logic unit or cell. Each net has its ground capacitances, and there are coupling capacitances between different nets. When circuit feature size decreases, the space between interconnects is reduced and the ratio of coupling capacitance and substrate capacitance increases proportionally.

[0012] The effects of crosstalk ("crosstalk effect") pose two major problems. In the case where the victim net is quiet (non-switching), capacitive crosstalk can induce noise (glitches) and potentially cause functional failures. For example, if a glitch happens when the clock signal of a register is switching, the data in the register may be flipped accidentally. Alternatively, in a case where the victim net is active, crosstalk can change the delay of the victim if the aggressor is also switching. If the aggressor is switching in the opposite direction, crosstalk can lead to an increase in delay, which may cause "setup time violations." If the aggressor is switching in the same direction as the victim, crosstalk may lead to the delay decreasing, and may cause "hold time violations."

[0013] What is needed is a method of statistical timing that accounts for crosstalk as well as accounting for cell delay and noise.

SUMMARY OF INVENTION

[0014] The invention provides a sensitivity-based statistical delay calculation methodology. The inventive method provides accurate nominal delay together with the delay sensitivities with respect to different circuit elements (*e.g.*, cells, interconnects, etc.) and variational parameters such as fabrication process and environmental variations. The invention provides a statistical delay calculation methodology, which

can efficiently calculate nominal delay and its sensitivity over different parameters. In the inventive statistical effective capacitance approach, all the sensitivity computations are based on closed-form formulas; consequently, the inventive method provides, rapidly and at low cost, high accuracy and high numerical stability.

[0015] The invention also provides a method for calculating waveform-based statistical noise and cross-talk delay. By means of "built-in" noise waveform alignment techniques, the method can accurately calculate statistical noise waveform and its impact on delay. The invention taught herein applies statistical Max and Sum operations to statistical noise waveform and noise envelope calculations.

[0016] The invention taught herein is broadly represented in Fig 1. The invention provides statistical delay calculation 302 considering non-linear cell input noise waveform and receiver capacitance. The invention further provides statistical noise calculation 304 considering non-linear victim driver resistance model and multiple timing windows. The invention further provides statistical crosstalk delay calculation 306 combining non-cross-talk statistical delay and statistical noise information – using pure analytical approaches and guaranteeing pessimism.

[0017] The inventive method of calculating delay comprises a first step of calculating a statistical driving circuit , and includes the sub-steps of calculating statistical compact interconnect load; calculating nominal effective capacitance through an equilibrium equation; and calculating statistical driving Thevenin/Norton circuit.

[0018] Once the Thevenin circuit is parameterized, the invention further provides for determining statistical delay and transition by: calculating the statistical transfer function to fanout pins; calculating the statistical voltage waveforms at the fanout pins; and calculating the statistical delay and the transition from the waveforms.

[0019] The inventive method further provides the step of statistical noise calculation including the sub-steps of: a) calculating statistical noise waveform and envelope for a given input pin of a given aggressor cell; b) repeating Step a for all input pins of a given aggressor cell; c) calculating the statistical Max of the noise envelopes from all input pins of a given aggressor cell; d) repeating Step c for all aggressor cells; e) calculating the statistical Sum of the noise envelopes from all aggressors cells.

[0020] Also taught is a method of crosstalk delay calculation that includes the steps of: calculating statistical output waveform as the statistical Sum of the statistical fanout waveform of the victim cell (the value of the statistical fanout waveform from the victim cell is provided by the delay calculation of the method taught herein) and statistical noise waveform from the aggressor cells (the value of the statistical noise waveform from the aggressor cells is provided by the noise calculation of the method taught herein) and calculating crosstalk delay from statistical waveform using an equation $td_i = -\frac{v_i(td) + n_i(td)}{\partial v(td)/\partial td + \partial v(td)/\partial td}$ where td= time delay, v=voltage and n=noise .

[0021] As can easily be appreciated, the system and method may be implemented via software – computer readable media- or any configuration of components capable of delivering instructions to a central processing unit of any computing device. Moreover, an apparatus for performing the invention as well as a product resulting from the invention are within the scope of the teaching and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the drawings in which:

[0023] Fig 1 is a summary chart of the invention taught herein, and some components (statistical delay calculation, statistical noise calculation, statistical crosstalk delay evaluation) and relationships of those components in the preferred embodiment.

[0024] Fig 2 a-c illustrates the main steps in the method of statistical delay calculation, which includes statistical driving circuit constructing and statistical fanout waveform and delay/transition calculation.

[0025] Fig 3a-b is pseudo code representing the method of statistical delay calculation.

[0026] Fig 4 is a flow chart depicting the steps of Fig 2a-c and Fig 3a-b according to the preferred embodiment.

[0027] Fig 5 a - c inclusive illustrates the main steps of the method for statistical noise and statistical crosstalk delay calculation, including noise/envelope statistical operation and worst case crosstalk delay calculations.

[0028] Fig 6 a-b, inclusive, is pseudo code representing the method for determining statistical noise and crosstalk delay.

[0029] Fig 7 is a flow chart depicting the steps of Fig 5 a-c and Fig 6a-b according to the preferred embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0030] The invention taught herein is broadly represented in Fig 1. The invention provides a method of determining statistical delay 302 considering non-linear input waveform and receiver capacitance. The invention further provides a method for statistical noise calculation 304 considering non-linear victim driver resistance model and multiple timing windows. The invention further provides statistical crosstalk

delay calculation 306 combining non-cross-talk statistical delay and statistical noise information using pure analytical approaches and guarantee pessimism (*i.e.*, satisfying a verification condition ensuring the IC chip circuits function).

[0031] In modern VLSI digital circuit, logical cell delay is a function of different physical sources. Cell delay is a function of non-linear input waveform, non-linear receiver load capacitances, resistive interconnect load, crosstalk effect and process and environmental variations.

[0032] With the increasing effects of interconnect resistance, gate output waveforms becomes increasingly non-digital and can no longer be modeled as saturated ramps. To solve this problem, delay calculations with the Ceff (**C**oupled gate **eff**ective capacitance) concept is widely used to take into the RC shielding effect of an interconnect (see J. Qian, S. Pullela, and L.T. Pileggi, "Modeling the effective capacitance for the RC Interconnect of CMOS gates," IEEE Trans. On Computer-Aided Design, vol. 13 no. 12, pp. 1526 -1534, Dec, 1994).

[0033] Fig. 2 sketches the concepts underlying the steps to determine statistical delay. Fig 3 provides pseudocode for the inventive approach diagrammed in Fig 2; Fig 4 depicts the steps of the approach as in Fig 2 and Fig 3 in a flow chart. Initially, a statistical π circuit load model is constructed from the statistical interconnect information. The statistical π circuit load model is used to calculate the statistical Thevenin model through using the inventive equilibrium point equations; the equations include the sensitivities over input slope, cell process parameters and π load. Fig 2a (400): represents a total circuit; logic circuit 402; a first waveform 404; an interconnect (RC) 406; a second waveform 408. Fig 2b (410) (and see Fig 3a). The steps are shown in Fig 4: statistical driving circuit calculation 80 including the sub-steps of calculating the statistical compact interconnect load 82; calculating the

nominal effective capacitance through an equilibrium equation 84; and calculating the statistical driving Thevenin/Norton circuit 86.

[0034] Once the Thevenin model is parameterized, the interconnect 406 is then attached to the linear gate model (see Fig 2b) and a statistical linear circuit evaluation is performed to calculate the statistical fanout delay and slope (see Fig 2c (412)) (and see Fig 3b). The steps are shown in Fig 4, statistical delay and transition calculation 90 and include the substeps of: calculating statistical transfer function to fanout pins 92; calculating statistical voltage waveforms at fanout pins 94; and calculating statistical delay and transition from waveforms 96.

Equivalent statistical driver model calculation

[0035] The preferred embodiment of the invention as regards delay calculation includes the steps as set forth herein. Initially, a statistical Thevenin model is constructed from statistical Effective Capacitance evaluation. Then a nominal Ceff evaluation is performed to construct an equivalent Thevenin model. (A detailed nominal Ceff evaluation process can be found in Mustafa Celik, Lawrence Pileggi and Altan Odabasioglu, "IC Interconnect Analysis", Kluwer Academic Publishers, 2002 (incorporated by reference as if fully set forth herein)).

[0036] At this point, to aid the reader, the derivation is omitted and the resulting equation shown - the final average current expression for both π load and Ceff load from our modified nominal Ceff calculation. An equivalent Thevenin model can be computed by iteratively matching these two equations. As is shown in equations (1) and (2), to avoid unstable numerical computation, the inventive method improves the nominal Ceff evaluation by expressing the average current in turns of time constant.

$$i_{\pi} = \frac{\beta}{\Delta}(1 + \frac{k_{\tau 1} \cdot \tau_1}{\Delta}(e^{-\frac{\Delta}{\tau_1}} - 1) + \frac{k_{\tau 2} \cdot \tau_2}{\Delta}(e^{-\frac{\Delta}{\tau_2}} - 1)) \quad (1)$$

$$i_{ceff} = \frac{c_{eff}}{\Delta}(1 + \frac{\tau}{\Delta}(e^{-\frac{\Delta}{\tau}} - 1)) \quad (2)$$

[0037] Once the nominal Thevenin model is available, one can start to compute its sensitivity with respect to different circuit element and process parameters. To simplify the computation, we rewrite the Ceff expression in a general form as shown in equation (3) where $S(si, w, Ceff)$ and $T(si, w, Ceff)$ are output slew and time constant that are directly queried from cell table during Ceff iteration. Among all the variables in equation (3), only input slew (s_i) and π load ($\pi = c_1, c_2, r_{pi}$) are original variables. Considering process variation, we also introduce a new variable - **w** - which represents variational cell process parameters.

$$Ceff(si, \pi, w) = F(\pi, Ceff, S(si, w, Ceff), T(si, w, Ceff)) \quad (3)$$

[0038] Note that this equation (3) should always be satisfied. Thus its derivatives with respect to every original variable should be equal to zero. Using the satisfied equation, we can calculate the sensitivities of Ceff to input slew, π load and cell process variables: $dCeff/dsi$, $dCeff/dw$ and $dCeff/d\pi$.

[0039] Once statistical Ceff is available, the sensitivity of Thevenin model with respect to different variables can be easily computed by applying the chain rule.

Statistical waveform propagation and statistical delay and transition calculation

[0040] Once the statistical Thevenin model is available, an interconnect can be attached, and fanout delay and transition can then be calculated through statistical fanout moment. As in the previous steps (*see* Fig 3a), a nominal fanout delay evaluation is performed before sensitivity computations. Equation (4) shows the

formula of fanout waveform with two-pole approximation:

$$v(t)=\begin{cases}\frac{k_1}{\Delta\cdot p_1^2}(e^{p_1 t}-1-p_1 t)+\frac{k_2}{\Delta\cdot p_2^2}(e^{p_2 t}-1-p_2 t) & (t\le\Delta)\\ \frac{k_1}{\Delta\cdot p_1^2}(e^{p_1 t}-e^{p_1(t-\Delta)}-p_1\Delta)+\frac{k_2}{\Delta\cdot p_2^2}(e^{p_2 t}-e^{p_2(t-\Delta)}-p_2\Delta) & (t>\Delta)\end{cases} \quad (4)$$

[0041] From equation (4), we can calculate the sensitivity of the output waveform with respect to poles and zeros; the chain rule is then used to calculate the sensitivity for the Thevenin circuit and the interconnect load. Once waveform sensitivity has been thus determined, using the condition that $v(t_d)\equiv v_d$ and v_d is a fixed value, we can compute the timing sensitivity for a different fixed voltage point:

$$\frac{\partial t_d}{\partial x}=-\left(\frac{\partial v(t_d)}{\partial x}\right)\Big/\left(\frac{\partial v(t_d)}{\partial t_d}\right) \quad (5)$$

Statistical Noise and Crosstalk Delay Calculation

[0042] The invention provides a novel method for statistical noise analysis and crosstalk delay calculation (*see* Fig 1, 306). The method naturally combines aggressor timing window with noise waveform to reduce pessimism. It also takes into account the process variations from both aggressor and victim net driving cell. Fig 6 presents pseudocode expressing the main steps for statistical noise and crosstalk delay calculations according to the preferred embodiment. Fig 7 is a flow chart showing the steps for statistical noise calculation.

[0043] When the aggressor net is switching, its driving cell can be modeled as a Thevenin linear circuit. And the transfer function from aggressor driver pin to victim fanout pin can be calculated using moment-based methods. If we assume the transition time of the aggressor voltage source is Δ, and the transfer function is

modeled as a two-pole function where p1, p2, k1, k2 are corresponding poles and residues, the fanout noise waveform can be calculated using the following equations:

$$v(t)=\begin{cases}\frac{k_1}{\Delta\cdot p_1}(e^{p_1 t}-1)+\frac{k_2}{\Delta\cdot p_2}(e^{p_2 t}-1) & (t\le\Delta)\\ \frac{k_1}{\Delta\cdot p_1}(e^{p_1 t}-e^{p_1(t-\Delta)})+\frac{k_2}{\Delta\cdot p_2}(e^{p_2 t}-e^{p_2(t-\Delta)}) & (t>\Delta)\end{cases} \quad (6)$$

[0044] Noise waveform calculated in equation (6) has several useful features. First, noise waveform starts from zero (v(0) = 0) and end up with zero (v(∞) = 0). Second, there is one and only one peak on the waveform, and the voltage before- peak and after-peak decreases monotonically. Once the nominal waveform is calculated, it is straightforward to calculate the statistical waveform $dv(t)/dw$ by applying the chain rule on equation (6).

[0045] Equation (6) gives the statistical noise waveform at victim net when aggressor net switches at time t = 0. However, in static timing analysis, the exact switching time at a timing node is not known: only the earliest/latest arrival time is available. The aggressor cell/net input pin can switch at any time in this period between the earliest and the latest time available. In order to create the "worst case" noise scenario, we can combine the noise waveform with the arrival timing window to create a noise envelope.

[0046] A single noise envelope (*see* Fig 5a, 606) from a noise waveform 602 and a timing window 604 represents the worst case noise peak from a single aggressor. In general, there are multiple aggressors in a coupled system. To calculate the total noise effect on a victim from all aggressors, we combine all the noise envelopes.

[0047] There are two basic operations for noise envelope combination: Max and Sum.

As shown in Fig 5b, the Max 612 operation takes the bigger value of the envelope over the total time interval, while the Sum 626 operation adds two envelopes 622, 624 together to create a new envelope 628. The Sum operation is used to combine noise envelopes that come from all the aggressor nets and drivers. The Max operation is used to combine noise envelopes that come from all the input pins of each aggressor driver. Statistical noise calculation according to the present invention appears as a flow chart in Fig 7.

[0048] Referring to Fig 7, the steps for statistical noise calculation 900 include the substeps of:

a) Calculating statistical noise waveform and envelope for a given input pin of a given aggressor cell 905;

b) Repeating Step a for all input pins of the aggressor cell 910;

c) Calculating the statistical Max of the envelopes from all input pins of a given aggressor cell 915;

d) Repeating Step c for all aggressors cells 920;

e) Calculating the statistical Sum of noise envelopes from all aggressor cells 925.

[0049] Under process and environmental variations, noise waveforms and noise envelopes become statistical. To calculate the statistical noise waveform, the same "Max" and "Sum" concepts can be used. However, with process variations, these Max and Sum operations have to work on random variables instead of deterministic values.

[0050] Assume normal random variables x and y can be expressed as linear function of a set of independent random variables (p_1, p_2 ... p_n), e.g. $x = x_0+x_1 \cdot p_1+x_2 \cdot p_2+\ldots x_n \cdot p_n$ and $y = y_0+y_1 \cdot p_1+y_2 \cdot p_2+\ldots x_n \cdot p_n$. The Sum operation is

straightforward, $s = (x+y) = (x_0+y_0) + (x_1+y_1)p_1 + \ldots + (x_n+y_n)p_n$. For Max operation $z = \text{Max}(x, y)$, analytical formulas exist so that variable z can also be approximated by the same set of random variables $z = z_0+z_1 \cdot p_1+z_2 \cdot p_2+\ldots z_n \cdot p_n$. The parameters z_0 and z_i can be calculated from equation (7), where $\varphi(\bullet)$ and $\Phi(\bullet)$ are the probability density function (PDF) and the cumulative distribution function (CDF) of normal random variables, $a=\text{sqrt}(\sigma_x^2+\sigma_y^2-2\sigma_x\sigma_y\rho_{xy})$ and $\alpha=(\mu_x-\mu_y)/a$.

$$\begin{aligned} z_0 &= \mu_z = x_0\Phi(\alpha) + y_0\Phi(-\alpha) + a\varphi(\alpha) \\ z_i &= \rho_{z,p_i} = x_i\Phi(\alpha) + y_i\Phi(-\alpha) \end{aligned} \qquad (7)$$

[0051] The invention teaches using the statistical Sum and Max operations so as to calculate a final statistical noise waveform from individual noise waveforms. The invention teaches applying statistical Max and Sum operations to statistical noise waveform and envelope calculations. Referring again to Fig 7, the step of statistical crosstalk delay calculation 930 includes the sub-steps of:

Calculating the statistical output waveform as the statistical Sum of the statistical fanout waveform from victim cell (from the statistical delay calculation) and statistical noise waveform from all aggressor cells 935; and

Calculating crosstalk delay from the statistical waveform using the equation

$$td_i = -\frac{v_i(td) + n_i(td)}{\partial v(td)/\partial td + \partial v(td)/\partial td} \qquad (8)$$

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[0052] Crosstalk delay is a function of both noise waveform and original fanout waveform. Once available, total statistical noise waveform and statistical fanout waveform can be combined to calculate statistical crosstalk delay as a linear function of different process variables.

Theorem 1: Given victim fanout voltage waveform $v(t)=v_0(t)+v_1(t)\cdot p_1+v_2(t)\cdot p_2+\ldots v_i(t)\cdot p_i\ldots$ and noise waveform at the same fanout $n(t)=n_0(t)+n_1(t)\cdot p_1+n_2(t)\cdot p_2+\ldots n_i(t)\cdot p_i\ldots$, where $(p_1, p_2 \ldots)$ are a set of independent normal random variables, the statistical crosstalk delay td at that fanout can be calculated as $td=td_0+td_1\cdot p_1+td_2\cdot p_2+\ldots td_i\cdot p_i\ldots$ and

$$td_i = -\frac{v_i(td)+n_i(td)}{\partial v(td)/\partial td + \partial v(td)/\partial td} \qquad (9)$$

[0053] Theorem 1 can be proved by combining the statistical transition waveform and noise waveform and applying the chain rule. Because the transition waveform and the noise waveform both include statistical information, using Equation (9) we can easily calculate statistical crosstalk delay distributions.

[0054] As can easily be appreciated by those of skill in the relevant art, the system and method may be implemented via software – computer readable media- or in any configuration enabling the delivery of instructions for practicing the invention to any central processing unit of any suitable computing device. Moreover, an apparatus for performing the invention as well as a product resulting from the invention are within the scope of the teaching and claims.

[0055] The present invention is not limited to given embodiments or examples; the attached set of claims in light of the drawings and specification define possible further embodiments for a person skilled in the art.

Claims:

1. A method for determining statistical delay in static timing analysis of integrated circuits, the method comprising the step of :

a) calculating the statistical driving circuit 80 including the sub-steps of

1. calculating the statistical compact interconnect load 82;
2. using the results of sub-step 1, calculating the nominal effective capacitance through an equilibrium equation 84; and
3. using the results of sub-steps 1 and 2, calculating the statistical driving Thevenin/Norton circuit 86; and

b) calculating the statistical delay and transition 90 including the substeps of:

4. calculating statistical transfer function to fanout pins 92 using the statistical interconnect information;
5. calculating statistical voltage waveforms at fanout pins 94 using the statistical transfer function of substep 4 ; and
6. calculating, using the results of step 5 – the statistical voltage waveforms at the fanout pins - , the statistical delay and transition from the statistical voltage waveforms 96

the results of which determine the statistical delay useful in timing analysis of integrated circuits.

2. A method for statistical noise calculation for a plurality of logic cells, where each victim cell is surrounded by aggressor cells, comprising the steps of:

a) calculating statistical noise waveform and statistical noise envelope for an input pin of a given aggressor cell 905;

b) repeating Step a for all input pins of a given aggressor cell 910;

c) calculating the statistical Max of the noise envelopes from all input pins of a given aggressor cell 915;

d) repeating Step c for all aggressor cells 920;

e) calculating the statistical Sum of the noise envelopes from all aggressor cells, where the statistical noise for the plurality of logic cells is the Sum of all statistical noise from all aggressor cells.

3. A method for crosstalk delay calculation for a plurality of logic cells where one cell is a victim cell and the other cells are aggressor cells, comprising the steps of:

a) calculating statistical output waveform as the statistical Sum of the statistical fanout waveform from the victim cell and statistical noise waveform from all aggressor cells 935; and

b) calculating crosstalk delay from statistical output waveform of Step a, using the equation 940 $td_i = -\frac{v_i(td) + n_i(td)}{\partial v(td)/\partial td + \partial v(td)/\partial td}$ where td = time delay, v = voltage and n=noise

4. A computer readable medium containing an executable program having instructions to direct a central processing unit to determine the statistical delay of a plurality of interconnected logic cells, where the program comprises instructions to direct the computer to :

a) calculate the statistical driving circuit 80 by:

1. calculating the statistical compact interconnect load 82;
2. calculating the nominal effective capacitance through an equilibrium equation 84; and

3. calculating the statistical driving Thevenin/Norton circuit 86;

b) calculate statistical delay and transition 90 by::

1. calculating the statistical transfer function to fanout pins 92;
2. calculating the statistical voltage waveforms at fanout pins 94; and
3. calculating statistical delay and transition from waveforms 96.

5. The computer readable medium of claim 4 wherein the program further comprises instruction to direct the central processing unit to calculate statistical noise, and wherein at least one of the interconnected logic cells is a victim cell and the remainder are aggressor cells, by:

a) calculating the statistical noise waveform and noise envelope for a given input pin of a given aggressor cell 910;

b) repeating Step a for all input pins of a given aggressor cell 910;

c) calculating the statistical Max of the noise envelopes from all input pins of a given aggressor cell 915;

d) repeating Step c for all aggressor cells 920;

e) calculating the statistical Sum of the noise envelopes from all aggressor cells. 915

6. The computer readable medium of claim 5 wherein the program further comprises instruction to direct the central processing unit to calculate cross-talk delay, and wherein at least one of the interconnected logic cells is a victim cell and the remainder are aggressor cells, by:

a) calculating statistical output waveform as the statistical Sum of the statistical fanout waveform from the victim cell and statistical noise waveform from all aggressor cells 935; and

b) calculating crosstalk delay from statistical output waveform of Step a, using the equation 940 $td_i = -\frac{v_i(td) + n_i(td)}{\partial v(td)/\partial td + \partial v(td)/\partial td}$ where td = time delay, v = voltage and n=noise.

7. An apparatus for performing timing analysis for a plurality of logic cells (cells) where such cells include at least one victim and one aggressor, said apparatus comprising:
a statistical delay calculation logic 302 having a non-linear input waveform and a receiver capacitance input and logic to determine statistical delay based on the non-linear input waveform input and the receiver capacitance input.

8. An apparatus as in claim 7 further comprising:
a statistical noise calculation logic 304 considering non-linear victim driver resistance model and multiple timing windows.

9. An apparatus as in claim 8 further comprising:
a statistical crosstalk delay calculation logic 306 combining non-cross-talk statistical delay and statistical noise information.

10. A system for determining timing in an electrical circuit comprising:
means for statistical delay calculation 302 considering non-linear input waveform and receiver capacitance;
means for statistical noise calculation 304 considering non-linear victim driver resistance model and multiple timing windows; and
means for statistical crosstalk delay calculation 306 combining non-cross-talk statistical delay and statistical noise information.

11. A computer memory storing instructions to cause a computer to perform a method, said method comprising the steps of:

a) calculating the statistical driving circuit 80 including the sub-steps of

1. calculating the statistical compact interconnect load 82;
2. calculating the nominal effective capacitance through an equilibrium equation 84; and
3. calculating the statistical driving Thevenin/Norton circuit 86;

b) calculating the statistical delay and transition 90 including the substeps of:

1. calculating the statistical transfer function to fanout pins 92;
2. calculating the statistical voltage waveforms at fanout pins 94; and
3. calculating statistical delay and transition from the waveforms 96.

12. A computer memory storing instructions as in claim 11, said method further including the steps of :

a) calculating the statistical noise waveform and the statistical noise envelope for a given input pin of a given aggressor cell 905;

b) repeating Step a for all input pins of the aggressor cell 910;

c) calculating the statistical Max of the noise envelopes from all input pins of a given aggressor cell 915;

d) repeating Step c for all aggressor cells 920; and

e) calculating the statistical Sum of the noise envelopes from all aggressor cells.

13. A computer memory storing instructions as in claim 12, said method further including the steps of: calculating cross talk delay 930 via the sub-steps of:

a) calculating statistical output waveform as the statistical Sum of the statistical fanout waveform from the victim cell (where such statistical fanout from the victim cell is calculated in a statistical delay calculation) and the statistical noise waveform 935; and

b) calculating crosstalk delay from the statistical output waveform of Step a by using the equation 940. $td_i = -\frac{v_i(td) + n_i(td)}{\partial v(td)/\partial td + \partial v(td)/\partial td}$ .where td=time delay, v-voltage and n=noise.

14. A computer output product produced by the process of analyzing timing of an electrical circuit, the process comprising the steps of:

a) calculating the statistical driving circuit 80 by:

1. calculating the statistical compact interconnect load 82;
2. calculating the nominal effective capacitance through an equilibrium equation 84; and
3. calculating the statistical driving Thevenin/Norton circuit 86; and

b) calculating the statistical delay and transition 90 by:

1. calculating the statistical transfer function to fanout pins 92;
2. calculating the statistical voltage waveforms at fanout pins 94; and
3. calculating statistical delay and transition from the waveforms 96.

15. A computer output product produced by the process of analyzing timing of an electrical circuit as in claim 14, said process further including the steps of :

a) calculating statistical noise waveform and statistical noise envelope for a given input pin of a given aggressor cell 910;

b) repeating Step a for all input pins of the aggressor cell 910;

c) calculating the statistical Max of the noise envelopes from all input pins of a given aggressor cell 915;

d) repeating Step c for all aggressor cells 920; and

e) calculating the statistical Sum of the noise envelopes from all aggressor cells.

16. A computer output product produced by the process of analyzing timing of an electrical circuit as in claim 15, said process further comprising the calculation of cross talk delay 930 by:

a) calculating the statistical output waveform as the statistical Sum of the statistical fanout waveform of the victim cell (the value of the statistical fanout of the victim cell used is from claim 14 step b substep 2) and statistical noise waveform 935; and

b) calculating crosstalk delay from statistical waveform using the equation $td_i = -\frac{v_i(td) + n_i(td)}{\partial v(td)/\partial td + \partial v(td)/\partial td}$ where td=time delay; v=voltage, n=noise.

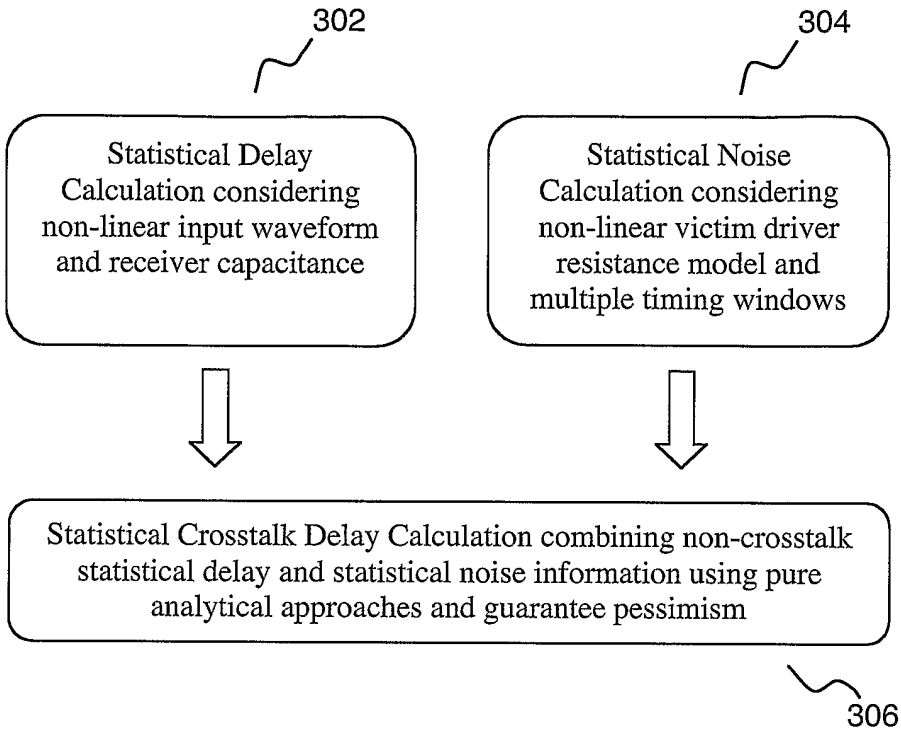

302
304
Statistical Delay Calculation considering non-linear input waveform and receiver capacitance
Statistical Noise Calculation considering non-linear victim driver resistance model and multiple timing windows
Statistical Crosstalk Delay Calculation combining non-crosstalk statistical delay and statistical noise information using pure analytical approaches and guarantee pessimism
306

Fig. 1

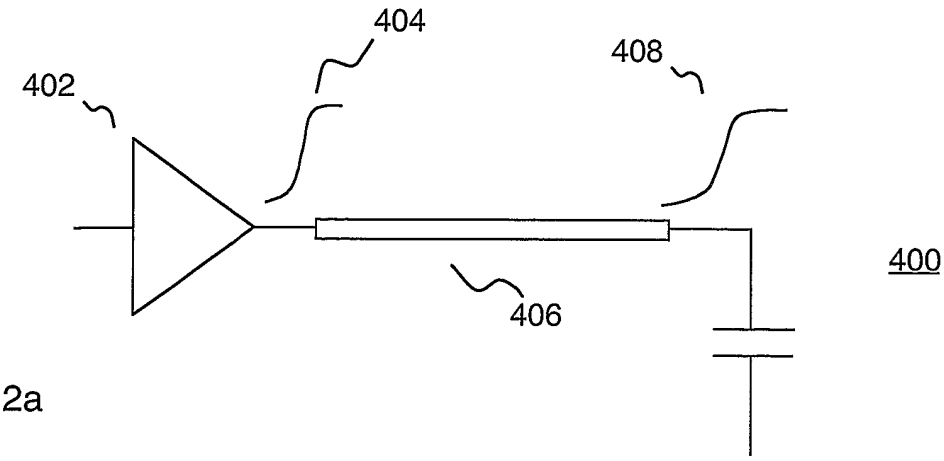


Fig. 2a

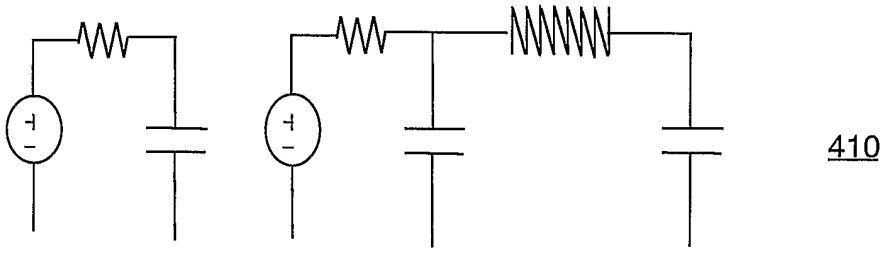


Fig.2b

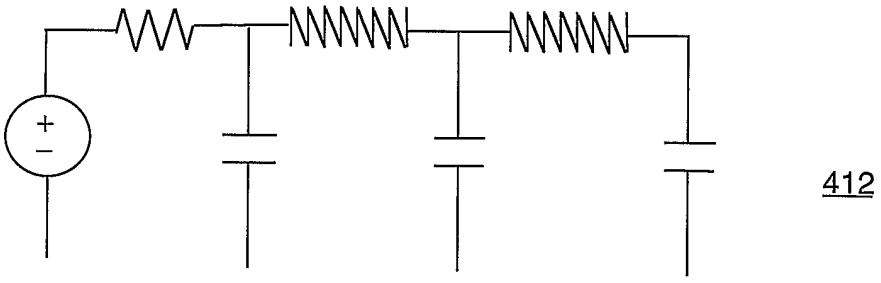


Fig. 2c

Fig 2

```
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
For each logic cell in the design {
   Load statistical cell information from library
   Load statistical interconnection information from extractor
   For each arc in the logic cell {
      Calculate statistical compact interconnect loading circuit {
         Collect statistical interconnection information {
            // R and C are functions of interconnect variations
            R = f(wire_width, thickness, ild, via_resistance, ...)
            C = g(wire_width, thickness, ild, via_resistance, ...)
         }
      }
      Construct equilibrium equation through effect capacitance iteration.
      Calculate statistical driving circuit model for the cell {
         // Each element of statistical driving (Thevenin / Norton) circuit
         // is expressed as functions input transition variation, cell variations
         // and interconnect elements and loading capacitance of the fanout
         // cells
         Drivering_Circuit = f ( input_transition, input_tail,
                                 cell_variation,
                                 interconnect_element,
                                 dynamic_capacitance_of_loading_cells )
      }                                                                    3a

      For each Fanout Pin of the Net {
          Calculate statistical transition function to fanout pin
          Calculate statistical waveform to fanout pin
          Calculate statistical delay and transition from waveform {
              // Using the delay definitions to build equilibrium equation
              v = v(t(w), w)
              dt/dw = dt/dv * dv/dw
          }
      }
   }
}                                                                          3b
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
```

Fig. 3

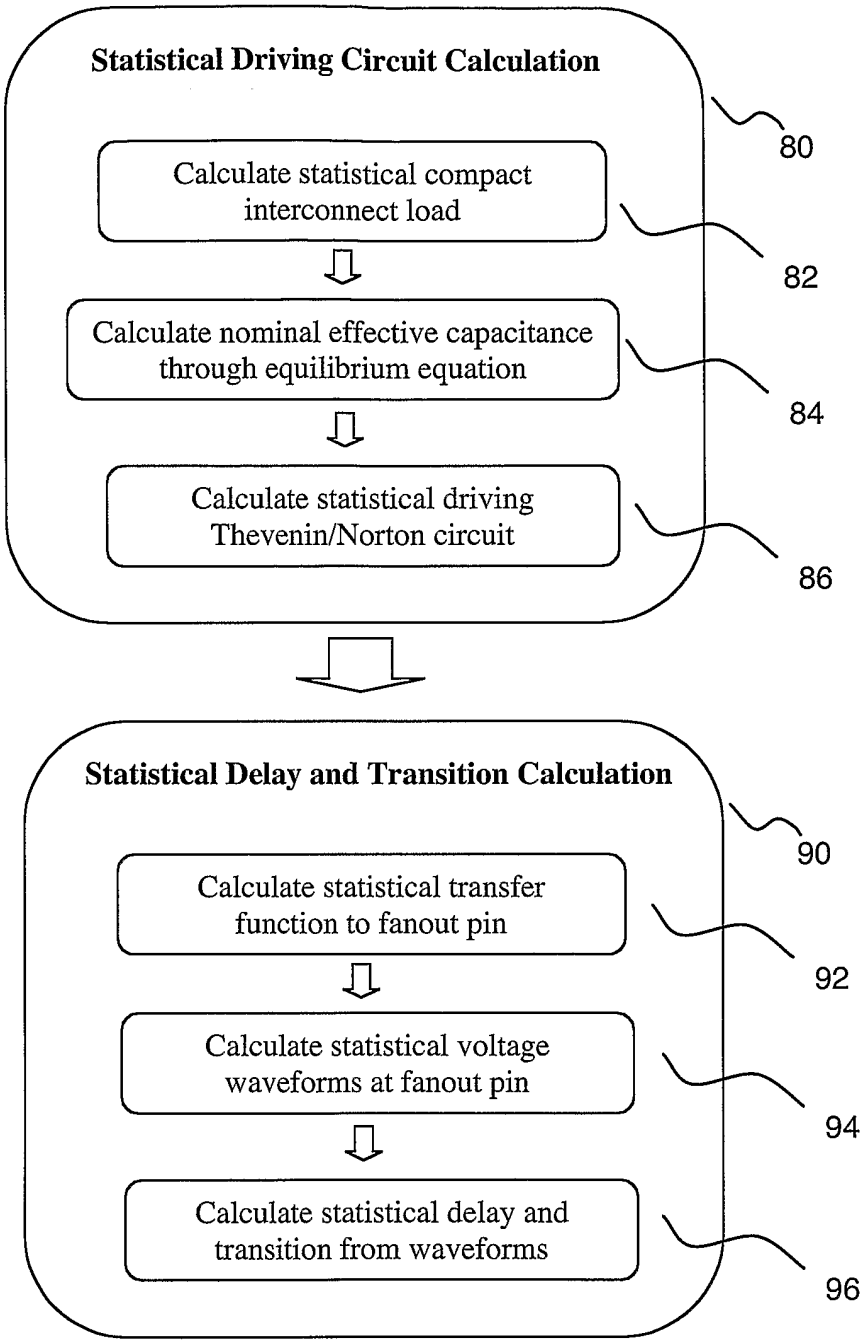

Statistical Driving Circuit Calculation
Calculate statistical compact interconnect load
Calculate nominal effective capacitance through equilibrium equation
Calculate statistical driving Thevenin/Norton circuit
80
82
84
86
Statistical Delay and Transition Calculation
Calculate statistical transfer function to fanout pin
Calculate statistical voltage waveforms at fanout pin
Calculate statistical delay and transition from waveforms
90
92
94
96

Fig. 4

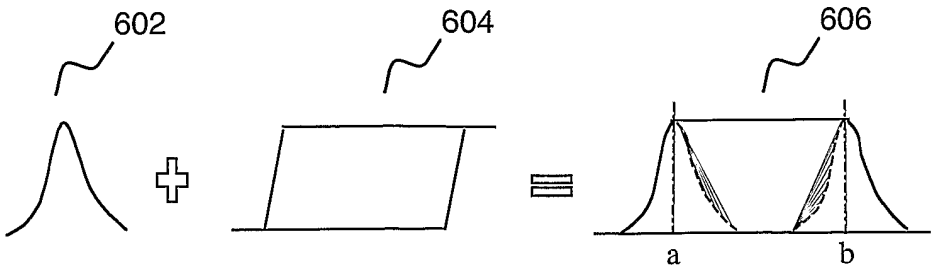


Fig. 5a

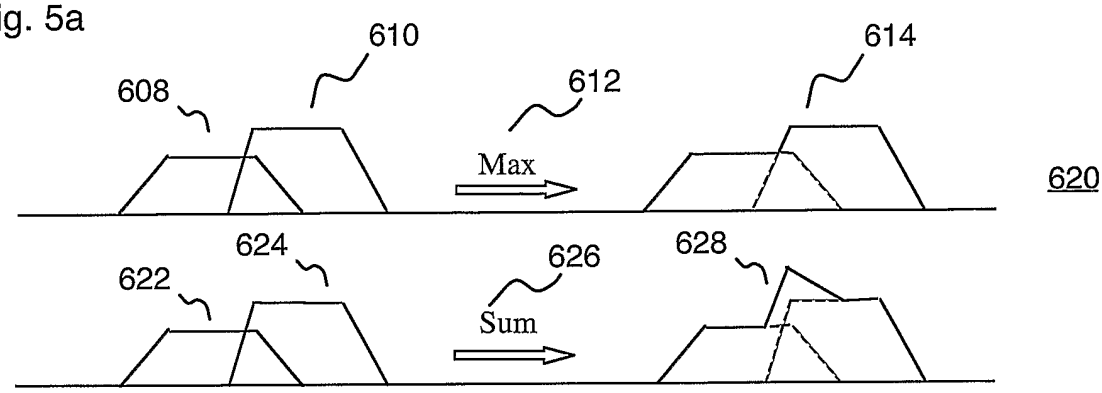


Fig. 5b

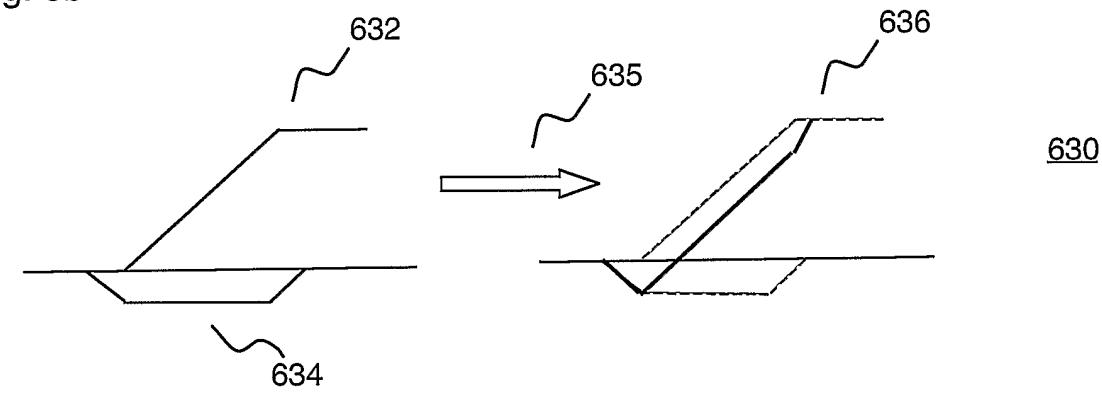


Fig. 5c

Fig. 5

For each cell in the design
  For each aggressor of the cell {
    For each aggressor cell input {
      Calculate the statistical noise waveform from a given aggressor cell input
      Calculate the statistical noise envelope from a given aggressor cell input
    }
    // To keep the pessimism, we take the worst case scenario of all possible input
    // from a given aggressors. Here we apply statistical max operation on the
    // waveforms.
    //
    //
    //
    //
    //
    Calculate statistical MAX of the envelopes from all inputs of a given aggressor cell
  }

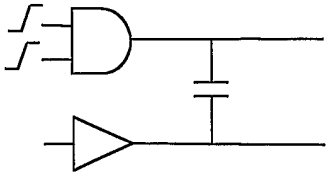
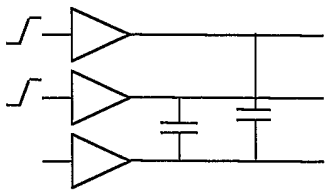


Fig. 6a

// To calculate total effects of statistical noise on victim, we need to add up all
// the noise effect from different aggressor nets.
//
//
//
//
//
//
Calculate statistical SUM of all envelopes from different aggressors



// Now we have statistical noise envelopes, we can use that information to calculate
// statistical crosstalk delay using equilibrium equations that combine transition and
// noise waveform.
Calculate statistical output waveform with noise effect.
Calculate statistical crosstalk delay.

$$td_i = -\frac{v_i(td) + n_i(td)}{\partial v(td)/\partial td + \partial v(td)/\partial td}$$

// Note that to consider non-linear victim driver effect, we can updated each noise
// waveform based on updated output waveform and repeat above procedures.
}

Fig. 6b

Fig. 6

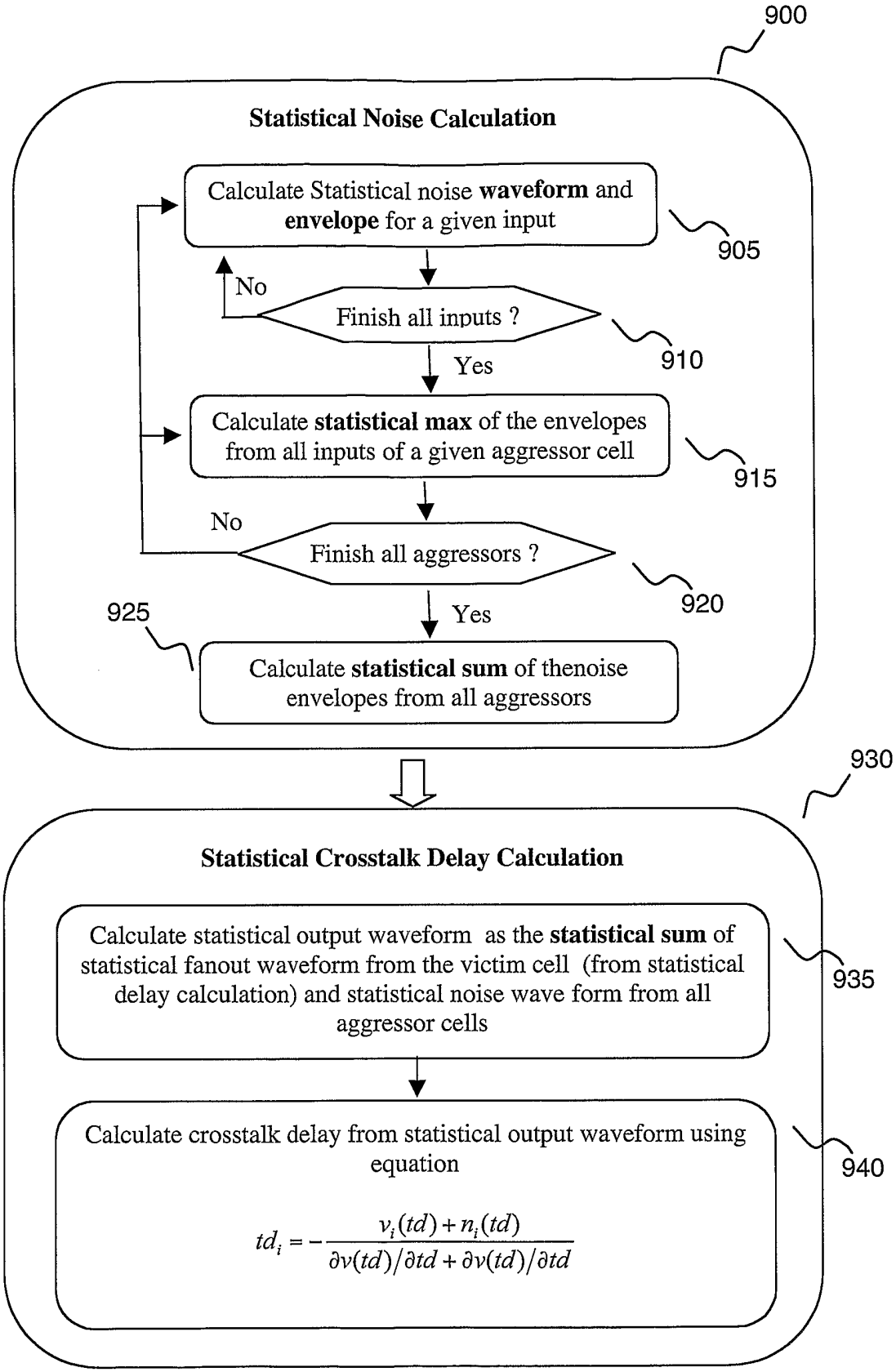

900
Statistical Noise Calculation
Calculate Statistical noise **waveform** and **envelope** for a given input
905
No
Finish all inputs ?
910
Yes
Calculate **statistical max** of the envelopes from all inputs of a given aggressor cell
915
No
Finish all aggressors ?
920
925
Yes
Calculate **statistical sum** of thenoise envelopes from all aggressors
930
Statistical Crosstalk Delay Calculation
Calculate statistical output waveform as the **statistical sum** of statistical fanout waveform from the victim cell (from statistical delay calculation) and statistical noise wave form from all aggressor cells
935
Calculate crosstalk delay from statistical output waveform using equation
940
$td_i = -\frac{v_i(td) + n_i(td)}{\partial v(td)/\partial td + \partial v(td)/\partial td}$

Fig. 7

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference MC O3182006	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US06/09634	International filing date (*day/month/year*) 17 March 2006 (17.03.2006)	(Earliest) Priority Date (*day/month/year*) 18 March 2005 (18.03.2005)
Applicant CELIK, MUSTAFA		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☒ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the Report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed.
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. _____
      ☐ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☒ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US06/09634

A. CLASSIFICATION OF SUBJECT MATTER
IPC: **G06F 9/45**(2006.01);**G06F 17/50**(2006.01)

USPC: 716/4,5,6;703/1,2,3,13
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 716/4,5,6; 703/1,2,3,13

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 6,496,960 B1 (Kashyap et al.) 17 December 2002 (17.12.2002), Figure 4 US 6,405,348 B1 (Fallah-Tehrani et al.) 11 June 2002 (11.06.2002), Figures 2, 3, 6, 7, and 9	1,4,11,14 ---------- 2,3,5-10,12,13,15,16
X	US 6,405,348 B1 (Fallah-Tehrani et al.) 11 June 2002 (11.06.2002), Figures 2, 3, 6, 7, and 9	2,3, 7-10
X	US 6,496,960 B1 (Kashyap et al.) 17 December 2002 (17.12.2002), Figure 4	1,4,11,14

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
26 May 2006 (26.05.2006)

Date of mailing of the international search report
18 JUL 2006

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Form PCT/ISA/210 (second sheet) (April 2005)