(54) Title: SYSTEM FOR PRODUCING A SYSTEM CLOCK AND TEMPERATURE GRADIENT DETECTION SYSTEM
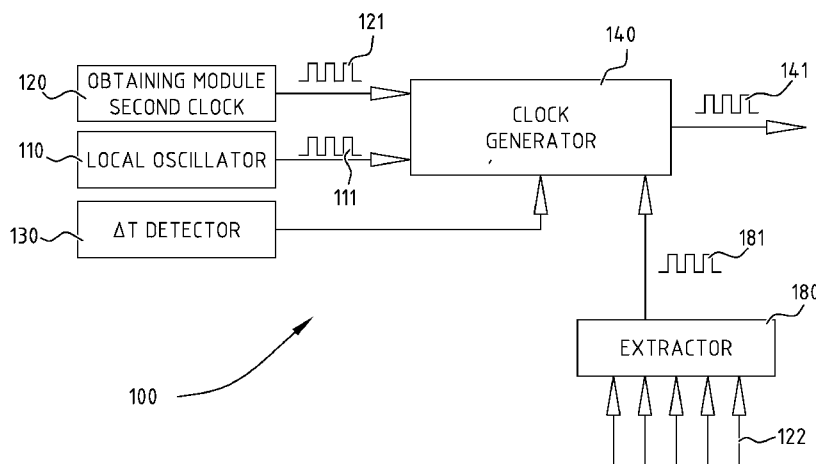
FIG. 1

(57) Abstract: System for producing a system clock signal comprising a local oscillator configured to generate a first clock signal; a temperature detector configured to detect a temperature change above a critical value in an area including the local oscillator; an obtaining module configured to obtain a second clock signal; a clock generator configured to generate the system clock signal in a first manner, using the first clock signal, in a normal mode when the temperature detector does not detect a temperature change above the critical value, and in a second manner different from the first manner, using the second clock signal, in a reverse hold-over mode when the temperature detector has detected a temperature change above the critical value.

**System for producing a system clock and temperature gradient
detection system**

Technical field

5   Embodiments of the invention relate to the field of systems
and methods for producing a system clock. Further
embodiments of the invention relate to the field of
temperature gradient detection systems and methods.

10 Background

Time synchronization or clock distribution in a timing
dependent system or network, e.g. a telecommunications
network, is usually subject to very strict specifications
for frequency stability, e.g. as specified in ITU-T

15 recommendations G.803, G.812, G.813, G.823, G.824, G.8262
and/or many others. The nodes in a (telecommunication)
network often receive timing information from an external,
network wide reference. This can be a dedicated clock signal
with very stable frequency, or it can be a data clock

20 extracted from the incoming data communication links. This
clock information is compared with the output clock signal
from a local reference oscillator to determine the error-
offset of this local reference oscillator. The local
reference clock signal, corrected by the determined error-

25 offset, is then used to generate the desired frequencies
required by the transmitted communication links, and to
maintain a system clock signal during periods of failure of
the external reference clock signal (hold-over). This
mechanism implies that the frequency stability of the system

30 clock is tightly locked to the frequency stability of its
local oscillator, even in the presence of an external
reference clock signal. However, the output frequency of a
typically used local oscillator is typically sensitive to

temperature variations, which threaten the required stability. Although there exist oscillators such as Rubidium or atomic clocks which are more or less insensitive to temperature variations, those clocks are generally too

5   expensive and/or too big in size to be used e.g. in nodes of communication networks.

Summary

An object of embodiments of the invention is to provide a

10   system for generating a system clock which is more stable than in prior art systems, and can cope with temperature variations.

According to embodiments of the invention, the system

15   comprises a local oscillator, an obtaining module, a temperature detector, and a clock generator. The local oscillator is configured to generate a first clock signal. The obtaining module is configured to obtain a second clock signal. The temperature detector is configured to detect a

20   temperature change above a critical value in an area including the local oscillator. The clock generator is configured to generate the system clock signal in a first manner, using the first clock signal, in a normal mode when the temperature detector does not detect a temperature

25   change above the critical value, and in a second manner different from the first manner, using the second clock signal, in a reverse hold-over mode after the temperature detector has detected a temperature change above the critical value.

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The obtaining module may be an extractor configured to extract a second clock signal from at least one external signal received at the system, but could e.g. also be a

module for receiving a second clock signal from an area near the system, which area is not influenced by the temperature change.

5   Using such embodiments, in the presence of too steep temperature changes, it can be avoided that the resulting accuracy of the system clock signal deviates from the accuracy of the nominal frequency defined by a selected external reference clock, beyond the allowed tolerance, such
10   that the system can comply with the required specifications, and in particular with e.g. specifications relating to ITU-T recommendations concerned with time keeping, or backhauling applications of wireless communications onto the core networks.
15

Embodiments of the invention are based on the insight that there are two problems to be addressed: a timely detection of temperature gradients in timing related parts of the system; and a proper reaction to such temperature gradients
20   that cannot be compensated in timing related parts of the system.

The local oscillator may be an oven controlled crystal oscillator (OCXO), a temperature compensated crystal
25   oscillator (TCXO), or any other suitable oscillator. An oven controlled oscillator or temperature crystal oscillator has an enhanced thermal inertia, as a local reference oscillator, depending on the required stability of the system. These OCXO and TCXO provide accurate and stable
30   frequency outputs over a wide temperature range if the rate at which the environmental temperature changes is low, e.g. below 1°C per minute. However, in some fault conditions, e.g. in case of fan failure or replacement of a fan tray, or

in outside units, a temperature gradient much steeper than the 1°C per minute may occur. Opening doors of the cabinets containing the telecommunications equipment may be another source of higher temperature gradients. In embodiments of

5   the invention problems with steep temperature gradients are avoided by switching to a reverse hold-over mode when such a gradient is detected.

10   According to a preferred embodiment the local oscillator is configured to generate the first clock signal with a first frequency having a first temperature dependence, and the temperature detector comprises a further local oscillator adapted to generate a further clock signal with a second

15   frequency having a second temperature dependence which is significantly higher than the first temperature dependence. The temperature detector may then further comprise a comparator for comparing the first clock signal with the further clock signal in order to detect a temperature change

20   above a critical value. The comparator is preferably a phase comparator. The further local oscillator may be an oscillator, with a lower thermal inertia compared to the local oscillator, e.g. a cheap crystal oscillator.

25   According to a preferred embodiment, the clock generator is configured to generate the system clock signal in the first manner using the first clock signal as a master clock signal and a third clock signal for determining an error-offset value to be applied to the master clock signal to produce

30   the system clock signal. The third clock signal may be the same as the second clock signal and is typically obtained by providing an extractor configured to extract a third clock signal from at least one external signal received at the

system. The clock generator is then preferably configured to
store the error-offset value when switching from the normal
mode to the reverse hold-over mode, and to use this stored
error offset value for generating the system clock signal
5   when switching back from the reverse hold-over mode to the
normal mode.

According to an embodiment of the invention, protection
against a high temperature gradient, which may be detected
10   by the means described above, or by another means to detect
temperature changes, and which in either case affects the
short term accuracy of the local oscillator, is to
temporarily use a second clock signal directly extracted out
of the best external reference, instead of the first clock
15   signal, corrected by error-offset values as discussed above.
This condition where the local oscillator is not used for a
short period of time, but where one of the external
references is directly used to generate the system clock
corresponds with the reverse hold-over mode.
20

The clock generator may comprise a digital PLL to generate
the system clock signal using an intermediate clock signal
as a master clock signal and the second or third clock
signal for determining an error-offset value to be applied
25   to the master clock signal to produce the system clock
signal, wherein the intermediate clock signal is generated
in the first manner or in the second manner, depending on
whether the clock generator operates in the normal or
reverse hold-over mode. An example of such an embodiment is
30   disclosed in figure 3.

The clock generator may comprise a PLL in series with a
multiplexor, which are coupled between the output of the

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extractor and the master clock input of the digital PLL. The
multiplexor has preferably a first input coupled to the
local oscillator and a second input coupled to the output of
the PLL, and is configured to select the first input in the
normal mode, and to select the second input in the reverse
hold-over mode. The PLL is preferably provided with a
feedback loop with a feedback divider, said feedback loop
being adapted to have a divider value which is dependent on
the phase difference between the first clock signal and the
output of the PLL in the normal mode, said feedback loop
being further adapted to maintain said divider value
constant when switching from the normal to the reverse hold-
over mode.

According to an alternative embodiment the clock generator
comprises a digital PLL to generate the system clock signal
in the first manner using the first clock signal as a master
clock signal and the second clock signal for determining a
error-offset value to be applied to the master clock signal
to produce the system clock signal generated in the first
manner; and a switch-over module to switch between the
system clock signal generated in the first and second
manner. An example of such an embodiment is illustrated in
figure 2. The switch-over module may be a hitless switch-
over module comprising a PLL.

The system may comprise an internal clock synchronization
sub-system which is constantly monitoring its external
references to determine the quality, and validity of each
reference, in order to find and select the best one. This
may be based, amongst other means, on monitoring the
frequency stability of the external reference.

According to another aspect of the invention there is
provided a system for detecting a temperature change in an
environment comprising a first oscillator. The system
comprises the first oscillator which is configured to
5   generate a first clock signal having a first frequency which
changes in function of the temperature, and a second
oscillator adapted to generate a second clock signal with a
second frequency which changes faster with the temperature
compared to the first frequency. Further the system
10   comprises a comparator for comparing the first clock signal
with the second clock signal in order to detect a
temperature change. The first oscillator may e.g. be an oven
controlled crystal oscillator or a temperature compensated
crystal oscillator. The comparator is preferably a phase
15   comparator. The second oscillator may be an oscillator with
a lower thermal inertia compared to the first oscillator,
and may e.g. be a cheap crystal oscillator without any
temperature compensation.

20   According to an embodiment of the invention, sudden steep
temperature gradients are detected using a very cheap, not
at all temperature compensated second oscillator besides a
more robust, less temperature sensitive regular first
oscillator which forms the heart of the internal timing sub-
25   system, and may be corrected by an external reference clock
signal. A TCXO (Temperature Compensated Crystal Oscillator)
or OCXO (Oven Controlled Crystal Oscillator) is typically
used as the first oscillator with low temperature
sensitivity. This extra cheap second oscillator will react
30   very quickly to temperature changes, before the regular
first oscillator will. Comparing the output signal of both
will allow detecting and signaling such temperature changes,
before they start affecting the regular first oscillator.

8

Brief description of the figures

The accompanying drawings are used to illustrate presently
preferred non-limiting exemplary embodiments of systems and
5   methods of the present invention. The above and other
advantages of the features and objects of the invention will
become more apparent and the invention will be better
understood from the following detailed description when read
in conjunction with the accompanying drawings, in which:

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Figure 1 illustrates schematically a first embodiment of a
system of the invention;
Figure 2 is a schematic diagram of a second embodiment of a
system of the invention; and
15   Figure 3 is a schematic diagram of a third embodiment of a
system of the invention.

Figure 1 illustrates an embodiment of a system 100 for
producing a system clock signal according to the invention.
20   The system 100 comprises a local oscillator 110 configured
to generate a first clock signal 111. The local oscillator
is e.g. an oven controlled crystal oscillator or a
temperature compensated crystal oscillator. Further, the
system comprises an obtaining module 120 which is configured
25   to obtain a second clock signal 121. Also there is provided
an extractor 180 to extract a third clock signal 181 from at
least one external signal 122 received at the system 100.
Note that the second clock signal could be the same as the
third clock signal, in which case the obtaining module 120
30   and the extractor 180 are the same module, see also the
exemplary embodiments of figures 2 and 3 discussed below.
The extractor may be configured to extract from a number of
external signals 122 a quality of a clock signal included in

the external signal. Using this quality, the extractor may
extract the best external signal and decide to use the clock
signal of this best external signal as the third clock
signal 181.

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Further, the system 100 comprises a temperature detector
which is configured to detect a temperature change above a
critical value in an area including the local oscillator
110. When no significant temperature change is detected the

10   system operates in a normal mode, and upon detecting a
significant temperature variation the system switches to a
reverse hold-over mode. The detector 130 may be further
adapted to decide to remain in the reverse hold-over mode
for a minimum period of time in which period the systems

15   needs to be stable, i.e. in which period no further
significant temperature variations may be detected, before
the system may switch back to the normal mode. The
temperature detector 130 provides a detection signal to a
clock generator 140 to indicate whether a temperature change

20   above the critical value has been detected, i.e. whether to
change from the normal to the reverse hold-over mode.

The clock generator 140 is provided with the first clock
signal 111 from the local oscillator 110 and with the second

25   clock signal 121 from the extractor 120. Using this first
and second clock signal, the clock generator 140 generates a
system clock signal 141. The clock generator 140 is adapted
to generate the system clock signal 141 in a first manner
when no temperature change above the critical value is

30   detected, and in a second manner when a temperature change
above the critical value is detected. According to the first
manner, the first clock signal 111 is used to generate the
system clock 141, wherein the second clock signal 121 may be

used to correct the first clock signal 111. According to the
second manner, the second clock signal 121 is used to
generate the system clock signal 141.

5   Figure 2 illustrates a more detailed second embodiment of a
system 200 of the invention. The system 200 comprises a
local oscillator 210, e.g. running at 10 MHz, an extractor
220 for extracting a second clock signal from an external
signal, a temperature detector 230, and a clock generator
10 240 for generating a system clock. The second clock signal
may e.g. be running at 100 MHz, while the system clock
signal could be running at 200 MHz.

The temperature detector 230 comprises a further local
15 oscillator 231 having a low thermal inertia compared to the
local oscillator 210. The output of the local oscillator 210
and of the further oscillator 231 are fed into a phase
comparator 232. The local oscillator 210 and the further
oscillator 231 are placed in the same thermal environment
20 250. When the temperature in this local environment 250
changes, because of the lower thermal inertia of the further
oscillator 231, the frequency of the signal generated by the
further oscillator 231 will change faster compared to the
local oscillator 210. The phase comparator 231 evaluates the
25 difference in phase between the signal from the local
oscillator 210 and from the further oscillator 231 in
function of the time. When the slope of the phase difference
in function of the time changes, this is indicative of a
temperature change in the thermal environment 250. As
30 illustrated in figure 2, from the output of the phase
comparator 231, the window comparator 233 can determine
whether the temperature change in the thermal environment
250 is higher than a critical value. This result is

communicated to the clock generator 240. The local

oscillator 210 may be protected against temperature changes

to some extent, while the further oscillator 230 may be a

standard cheap crystal oscillator which is not protected

5   against temperature changes. A frequency difference is

constantly being monitored using the phase comparator 232,

and when this frequency difference suddenly changes, this is

an indication that a temperature gradient is present. The

amount of the sudden frequency change is a measure of the

10   temperature gradient and allows assessment of whether the

frequency of the first clock signal will be affected by the

temperature change or not. The skilled person will

understand that instead of using a crystal oscillator any

other suitable oscillator may be used.

15

The clock generator 240 comprises an optional processing

block 244 which is configured for multiplying or dividing

the frequency of the second clock signal 221 with a

predetermined factor and/or for cleaning jitter in the

20   second clock signal 221. In the example of having a second

clock signal 221 of 100 MHz and a system clock 241 of 200

MHz, a multiplier "2" will be used. Further, the clock

generator 240 comprises a digital PLL 242 which uses the

first clock signal 211 as a master clock signal or base

25   clock. This master clock signal is multiplied with a

correction factor which is determined using the second clock

signal 221 derived from the one or more external references.

The output of the digital PLL 242 is fed into a hitless

switchover block 242 which performs a hitless switchover.

30   The hitless switchover block 243 uses the output of the

temperature detector 230 to determine how to set a

multiplexer 245. When no critical temperature change is

detected, the output of the DPLL 242 is passed by the

multiplexer 245 to a PLL 246, and the system clock will be
equal to the output of the DPLL 242. When a critical
temperature change is detected, the multiplexer switches,
and allows the output of the processing block 244 to be fed

5   in the PLL 246. The PLL 246 will ensure that when a
switching of the multiplexer 245 takes place, the transition
from the output signal of the DPLL 242 to the output of the
processing block 244 en vice versa happens smoothly by
adjusting the phase. The hitless switchover block 242 may be

10 further provided with a button to perform a manual
switchover of the multiplexer 245. In that way, when a
critical temperature change is expected, e.g. because of
maintenance operations to the cabinet, it can be decided to
use the second clock signal 221 from the external references

15 instead of the first clock signal 211 from the local
oscillator 210.

Figure 3 illustrates a third embodiment of a system 300 of
the invention. The system 300 comprises a local oscillator

20 310, an extractor 320, a temperature detector 330, and a
clock generator 340. The temperature detector 330 is
identical to the temperature detector 230 described above
with reference to figure 2, and hence a detailed description
thereof has been omitted. As in the embodiment of figure 2,

25 the temperature detector 330 comprises an oscillator 331
having a low thermal inertia compared to the local
oscillator 310, a phase comparator 332, and a window
comparator 333.

30 The clock generator 340 comprises a multiplexer 345 which
will allow the first clock signal 311 of the local
oscillator 310 to pass as the master clock signal 371 to the
input of a digital PLL 342, when no critical temperature

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change has been detected by the temperature detector 330.
The clock generator 340 further comprises a processing block
344 which is adapted to ensure that the second clock signal
321 derived from one or more external reference signals 322

5   is in phase with the first clock signal 311. Further, the
processing block 344 may be adapted to multiply or divide
the second clock signal 321 with a suitable factor. This
processed second clock signal is fed into the multiplexor
345, and will be selected by the multiplexor 345 when the

10   detected temperature change is above a critical value. Also,
when detecting the critical change the settings of the
feedback loop of processing block 344 will be frozen, see
further, so that the first clock signal no longer influences
the processed second clock signal. In that way the master

15   clock signal that is fed in the DPLL 342 will be either the
first clock signal 311 or the processed second clock signal
321' depending on whether a critical temperature change has
been detected. When the temperature has become stable again,
the multiplexor may switch back to the first clock signal.

20   To ensure a smooth transition back, a delay may be
introduced, see block 369, so that the switching is done
when there is no phase difference between the first clock
signal 311 and the processed second clock signal 321', which
will be detected by the phase comparator 368. The DPLL 342

25   corrects the master clock signal 371, being either the first
clock signal 311 or the processed second clock signal 321'
depending on whether a critical temperature change has been
detected, with a correction factor which is determined
using the second clock signal 321 derived from the one or

30   more external references 322.

The processing block 344 comprises a reference divider 361,
a phase comparator 362, a loop filter 363 having a high

bandwidth, a VCO 364, an output divider 365 and a feedback
divider 366. The reference divider 361 and the output
divider 365 are typically configured at fixed values. In
normal operation, i.e. when no critical temperature is

5   detected, the feedback divider 366 is configured with a
value which is dependent on the phase difference between the
first clock signal 311 and the output 321' of the PLL 344,
using phase comparator 368 and averaging filter 367. In that
way the PLL's output 321' can be brought to be in phase with

10   the first clock signal 311. This will allow a so-called
hitless switch-over in a temperature gradient is detected.
Further, when a temperature gradient is detected, the
parameters of the averaging filter 367 are frozen until the
temperature is again stable.

15

In this third embodiment, at the entrance of the DPLL 342,
the first clock signal 311 from the local oscillator 310 is
replaced with a clock 321' of the same frequency and phase,
but derived directly from the selected external reference

20   clock, through a VCO 364 with high bandwidth. The oscillator
in this VCO 364 will also be suffering from the temperature
effects that invalidate the local oscillator 310 as local
reference, but the impact of this on the VCO output will be
neutralized by virtue of the high bandwidth commodity of the

25   loop filter 363, which will make it track accurately the
stable external reference clock 321, despite changes in the
control voltage to frequency characteristic of the VCO 364.
This third embodiment may provide an even better system
clock behavior, as the system clock remains generated by the

30   DPLL 342 in both situations, only using a different input
base clock 371 for each situation.

A skilled person will notice that processing block 344 is actually a DPLL which uses the second clock signal 321 as a master clock to produce the processed second signal 321' which is in frequency and phase identical to the first clock

5   signal 311 produced by the local oscillator 310 for as long as no harmful temperature gradient was detected. Therefore processing block 344 may be replaced by any other known DPLL with the similar functionality.

10   Where in the embodiments disclosed above reference is made to a divider or a multiplier, the skilled person will understand that this divider/multiplier may be a divide/multiply with "1", and that a divider may be a multiplier and vice versa.

15

The above discussed extractor and clock generator modules may be implemented using hardware and/or software components as will be apparent to the skilled person.

20   For all illustrated embodiments, it is typically assumed that the probability of simultaneous occurrence of unacceptable deviations of the selected external reference clock, as well as changes in the local system temperature, is very low, and below the required availability or up-time

25   for the system. Under this condition, the described embodiments will protect against each of both types of failure, whereas prior art embodiments only protect against deviations in the selected external reference clock, and require a stable local oscillator clock at all times.

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Timing dependent systems containing conventional temperature sensors and switches, have the following disadvantage compared to embodiments of the present invention. Such

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sensors and switches are intended for regulating its
cooling, and for protection (preventive power down) of the
equipment against overheating. These sensors are of little
use for detecting the kind of temperature variations that
5   may impair the internal timing logic of such systems in
time, and hence for protecting against such variations. The
temperature gradient detection of preferred embodiments of
the invention only requires one low cost crystal oscillator
and a very small additional silicon area for implementing
10   the phase comparator and window comparator, and can report
temperature gradients before they affect the local
oscillator.

Whilst the principles of the invention have been set out
15   above in connection with specific embodiments, it is to be
understood that this description is merely made by way of
example and not as a limitation of the scope of protection
which is determined by the appended claims.

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Claims

1. System for producing a system clock signal comprising:
- a local oscillator configured to generate a first clock
5   signal;

- a temperature detector configured to detect a temperature
change above a critical value in an area including the local
oscillator;
10   - an obtaining module configured to obtain a second clock
signal;
- a clock generator configured to generate the system clock
signal
          - in a first manner, using the first clock signal, in a
15   normal mode when the temperature detector does not
          detect a temperature change above the critical value,
          and
          - in a second manner different from the first manner,
          using the second clock signal, in a reverse hold-over
20   mode when the temperature detector has detected a
          temperature change above the critical value.

2. System of claim 1, wherein the obtaining module is
configured to obtain the second clock signal from at least
25   one external signal received at the system, so that the
second clock signal is not influenced by temperature change.

3. System of claim 1 or 2, wherein the local oscillator is
an oven controlled crystal oscillator or a temperature
30   compensated crystal oscillator.

4. System of any of the previous claims, wherein the local
oscillator is configured to generate the first clock signal

with a first temperature dependence, and the temperature
detector comprises a further local oscillator adapted to
generate a further clock signal with a second temperature
dependence which is significantly higher than the first

5   temperature dependence; and
wherein the temperature detector further comprises a
comparator for comparing the first clock signal with the
further clock signal in order to detect a temperature change
above the critical value.

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5. System of claim 4, wherein the comparator is a phase
comparator.

15   6. System of any of the previous claims, further comprising:
an extractor configured to extract a third clock signal from
at least one external signal received at the system;
wherein the clock generator is configured to generate the
system clock signal in the first manner using the first

20   clock signal as a master clock signal and the third clock
signal for determining an error offset value to be applied
to the master clock signal to produce the system clock
signal.

25   7. System of claim 6, wherein the clock generator is
configured to store the error offset value when switching
from the normal mode to the reverse hold over mode, and to
use this stored error offset value for generating the system
clock signal when switching back from the reverse hold over

30   mode to the normal mode.

8. System of claim 6, wherein the clock generator comprises
a digital PLL to generate the system clock signal using an

intermediate clock signal as a master clock signal and the
second or the third clock signal for determining a
correction factor to be applied to the master clock signal
to produce the system clock signal, wherein the intermediate

5   clock signal is generated in the first manner or in the
second manner, depending on whether the clock generator
operates in the normal or reverse hold over mode.

9. System of claim 8, wherein the clock generator comprises

10   a PLL in series with a multiplexor, which are coupled
between the output of the extractor and the digital PLL,
said multiplexor having a first input coupled to the local
oscillator and a second input coupled to the output of the
PLL, and being configured to select the first input in the

15   normal mode, and to select the second input in the reverse
hold over mode; and
a feedback loop with a feedback divider for said PLL, said
feedback loop being adapted to have a divider value which is
dependent on the phase difference between the first clock

20   signal and the output of the PLL in the normal mode, said
feedback loop being further adapted to maintain said divider
value constant when switching from the normal to the reverse
hold over mode.

25   10. System of any of the claims 1-8, wherein the clock
generator comprises a digital PLL to generate the system
clock signal in the first manner using the first clock
signal as a master clock signal and the second clock signal
for determining a correction factor to be applied to the

30   master clock signal to produce the system clock signal
generated in the first manner; and a switch-over module
(242) to switch between the system clock signal generated in
the first and second manner.

11. System of claim 10, wherein the switch-over module is a hitless switch-over module.

12. System for detecting a temperature change in an environment comprising

a first oscillator, said system comprising said first oscillator which is configured to generate a first clock signal having a first frequency which changes in function of the temperature, and

a second oscillator adapted to generate a second clock signal with a second frequency which changes faster with the temperature compared to the first frequency; and

a comparator for comparing the first clock signal with the second clock signal in order to detect a temperature change.

13. System of claim 12, wherein the first oscillator is an oven controlled crystal oscillator or a temperature compensated crystal oscillator.

14. System of claim 12 or 13, wherein the comparator is a phase comparator.

15. System of claim 14, further comprising a window comparator adapted to evaluate a change in the rate at which the phase difference determined by the phase comparator, increments or decrements.

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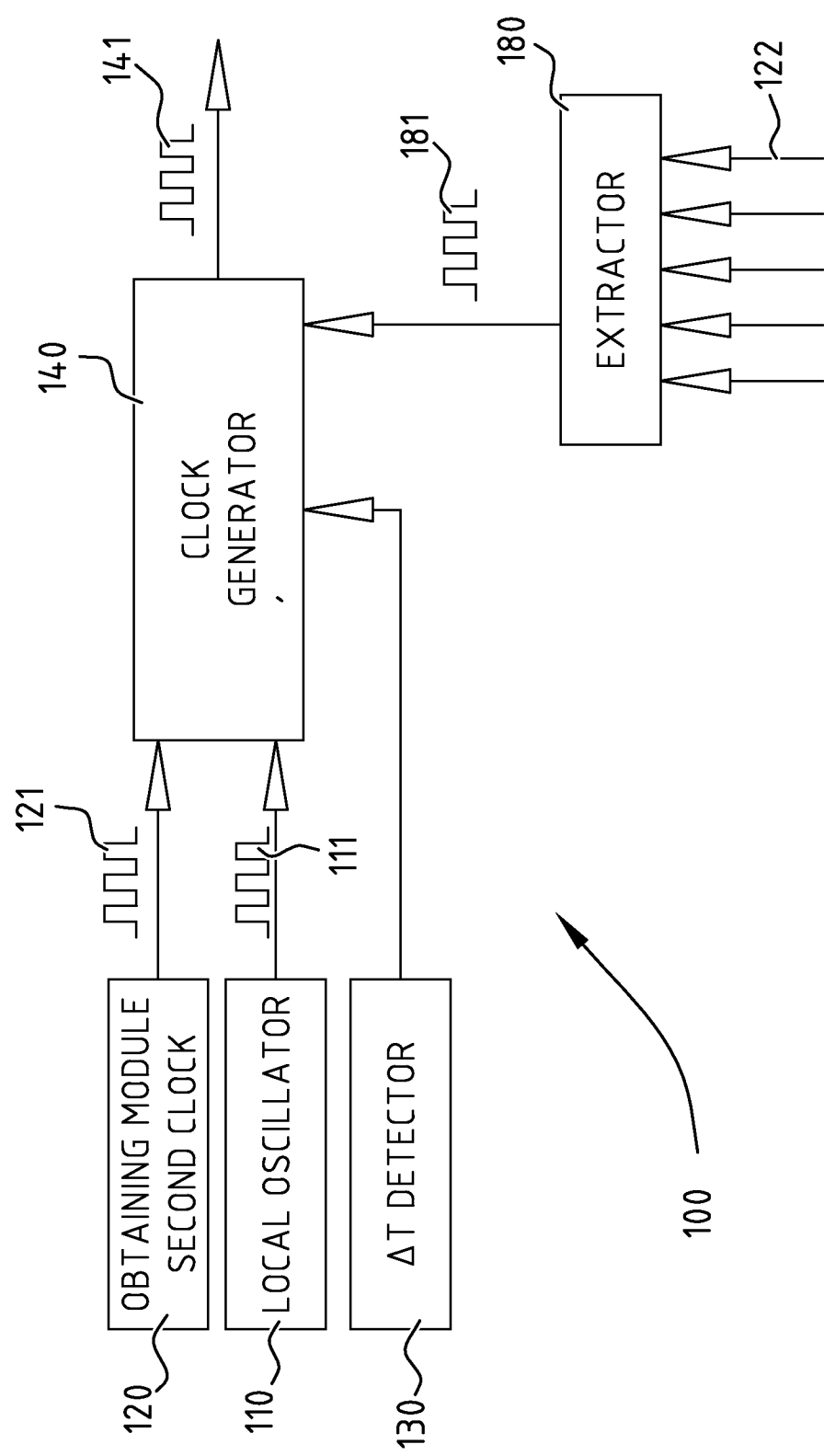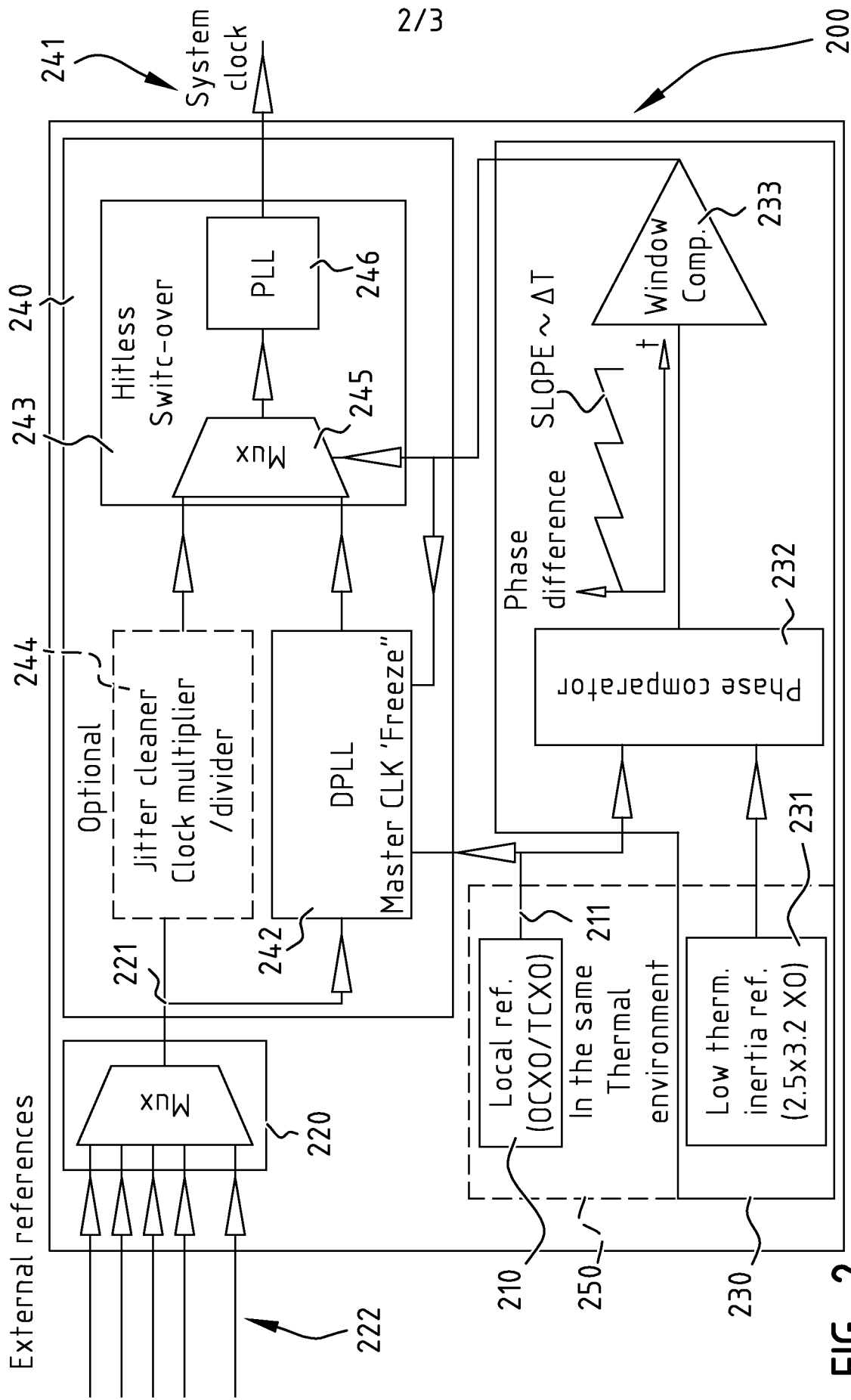

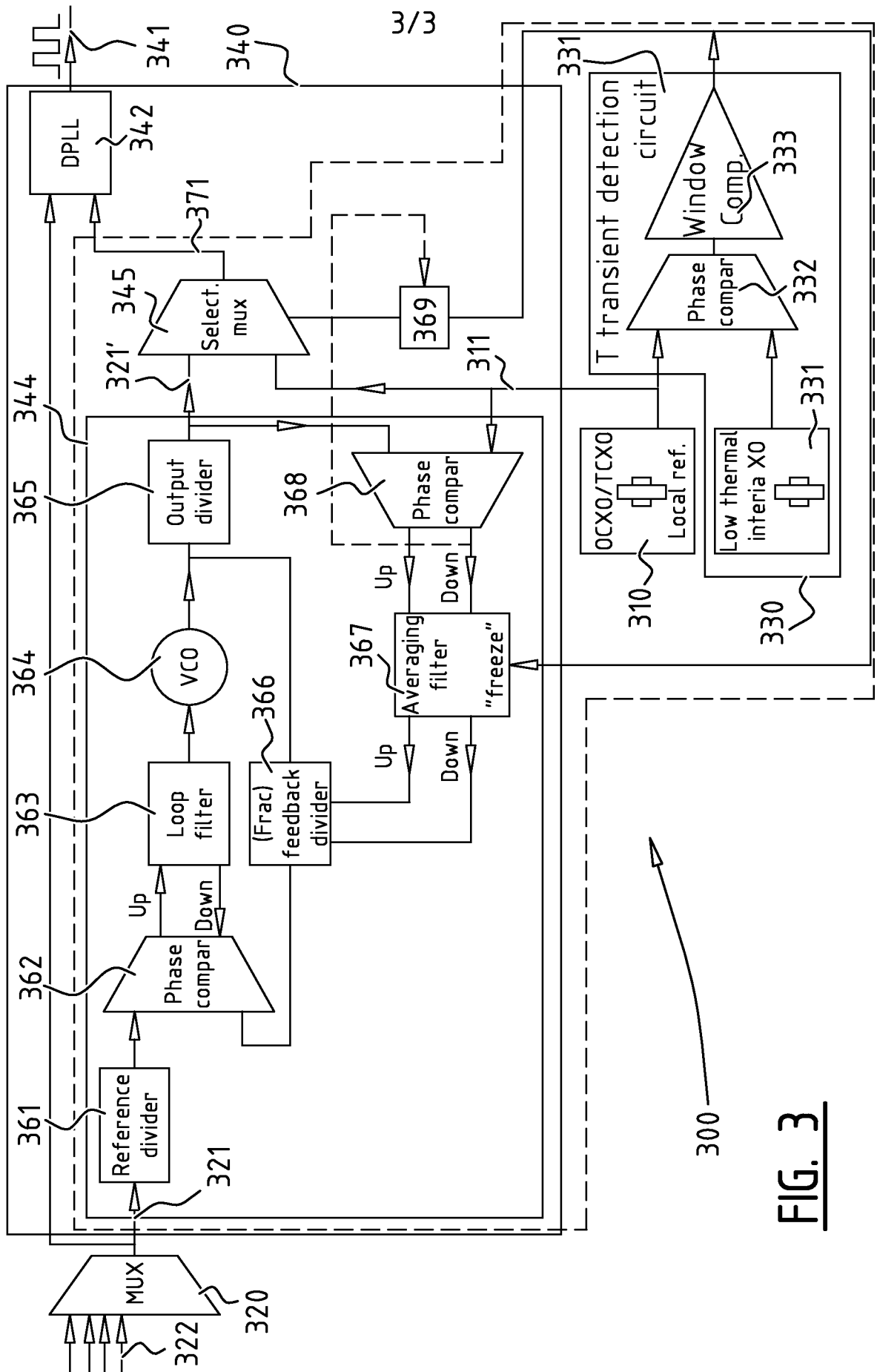<u>FIG. 1</u>

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FIG. 2

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FIG. 3

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03L1/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7 764 133 B1 (NICHOLLS CHARLES [CA]) 27 July 2010 (2010-07-27)	12-15
A	column 8, line 35 - column 9, line 28; figure 4 column 9, line 57 - column 10, line 4 -----	1-11
A	WO 2011/086976 A1 (FURUNO ELECTRIC CO [JP]; KOWADA SHINYA [JP]) 21 July 2011 (2011-07-21) abstract; figure 1 & EP 2 525 494 A1 (FURUNO ELECTRIC CO [JP]) 21 November 2012 (2012-11-21) -----	1-15
A	US 6 711 230 B1 (NICHOLLS CHARLES [CA] ET AL) 23 March 2004 (2004-03-23) column 1, line 1 - column 3, line 34; figure 2 ----- -/--	1-15

[X]	Further documents are listed in the continuation of Box C.	[X]	See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

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Date of the actual completion of the international search	Date of mailing of the international search report
2 October 2013	10/10/2013

Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Peeters, Mark

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