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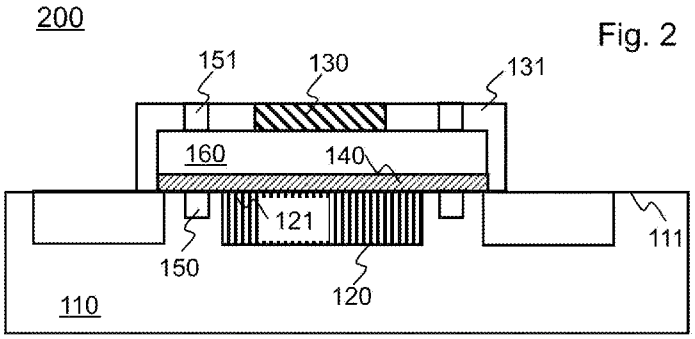

Fig. 2

(57) Abstract: A micro structure (100,200,300) comprising a substrate (110) having a top surface (111); a first electrode (120) with a horizontal orientation parallel to the top surface (111) of the substrate (110), wherein the first electrode (120) is embedded within the substrate (110) so that a top surface (121) of the first electrode (120) coincides with the top surface (111) of the substrate (110); a dielectric layer (140) arranged on the top surface (121) of the first electrode (120); and a second electrode (130) arranged above the dielectric layer (140).

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CAPACITIVE MICRO STRUCTURE

TECHNICAL FIELD

[0001] The present application generally relates to micro structures, fabrication techniques and to a semiconductor apparatus. In particular, but not exclusively, the present application relates to microelectromechanical system (MEMS) structures, integrated passive devices (IPD), switched capacitors, metal-insulator-metal (MIM) capacitors and microelectromechanical system (MEMS) switches.

BACKGROUND

[0002] This section illustrates useful background information without admission of any technique described herein being representative of the state of the art.

[0003] Components fabricated with the technologies of microelectromechanical systems (MEMS) are being incorporated in an increasing number of consumer applications including, but not limited to, automotive electronics, medical equipment, smart phones, hard disk drives, computer peripherals, and wireless devices. MEMS technology is directed at forming miniaturized electromechanical devices and structures using micro-fabrication techniques. MEMS devices have typically some form of mechanical functionality that is typically in the form of a least one moving structure. Structures may be formed on a suitable substrate by a series of processing steps involving thin film depositions that are photolithographically masked and etched. MEMS mechanical elements, sensors, and actuators may be integrated on a common substrate with complementary metal-oxide-semiconductor (CMOS) devices, for example.

[0004] Integrated passive devices (IPD) technology is a way for realizing high quality factor (Q) passives in low loss substrates. Combining most of passive components to IPD and then integrating IPD based module to sub-system enables high performance, high integration density and lower assembly cost. Especially RF front-end modules and components requiring high-Q inductors are beneficial to integrate to IPD such as baluns, couplers, filters, LC resonators and matching circuits

[0005] In known solutions, micro structures, such as microelectromechanical system (MEMS) metallizations are grown on top of wafers. This limits thickness of a bottom electrode typically to less than 2 μm. Known solutions also have resistive

losses.

[0006] It is the aim of the current invention to provide a method, structure and apparatus that mitigates for example the above problems of the state of the art.

SUMMARY

[0007] Various aspects of examples of the invention are set out in the claims.

[0008] According to a first example aspect of the present invention, there is provided a micro structure comprising:

a substrate having a top surface;

a first electrode with a horizontal orientation parallel to the top surface of the substrate, wherein the first electrode is embedded within the substrate so that a top surface of the first electrode coincides with the top surface of the substrate;

a dielectric layer arranged on the top surface of the first electrode; and

a second electrode arranged above the dielectric layer.

[0009] In an embodiment, the top surface of the first electrode is polished.

[0010] In an embodiment, thickness of the first electrode is more than 5 μm.

[0011] In an embodiment, the micro structure comprises a microelectromechanical system (MEMS) switch, and further comprises:

a structural layer having a beam structure in which both ends thereof are fixed to the substrate, and the structural layer comprises the second electrode provided on a surface of the structural layer facing the substrate.

[0012] In an embodiment, the micro structure further comprises:

a lower drive electrode provided below the structural layer and an upper drive electrode provided on the surface of the structural layer facing the substrate, wherein when a potential difference is arranged between the upper drive electrode and the lower drive electrode, the structural layer is attracted towards the substrate by an electrostatic attractive force, so that the second electrode operating as an upper switch electrode and the first electrode operating as a lower switch electrode come in contact with each other.

[0013] In an embodiment, the micro structure comprises a metal-insulator-metal (MIM) capacitor, wherein

the second electrode is arranged on a top surface of the dielectric layer.

[0014] In an embodiment, a first horizontal end of the top surface of the first electrode is left uncovered by the dielectric layer and the dielectric layer extends

over a second horizontal end of the top surface of the first electrode.

[0015] In an embodiment, a first horizontal end of the top surface of the dielectric layer is left uncovered by the second electrode and the second electrode extends to a second horizontal end of the top surface of the dielectric layer.

[0016] In an embodiment, the micro structure further comprises a connecting element arranged on the substrate and configured to provide at least one of the following:

a first connecting element configured to provide connection to the first horizontal end of the top surface of the first electrode; and

a second connecting element configured to provide connection to a second horizontal end of the second electrode adjacent to the second horizontal end of the top surface of the of the dielectric layer.

[0017] According to a second example aspect of the present invention, there is provided a method of forming a micro structure, the method comprises:

providing a substrate having a top surface;

forming a first electrode with a horizontal orientation parallel to the top surface of the substrate, wherein the first electrode is embedded within the substrate so that a top surface of the first electrode coincides with the top surface of the substrate;

forming a dielectric layer on the top surface of the first electrode; and

forming a second electrode above the dielectric layer.

[0018] According to a third example aspect of the present invention, there is provided a semiconductor apparatus comprising the micro structure according to the first aspect.

[0019] In an embodiment, the semiconductor apparatus comprises an integrated passive device (IPD).

[0020] In an embodiment, the semiconductor apparatus comprises a passivation layer arranged between the silicon substrate layer and a first metal layer.

[0021] In an embodiment, the semiconductor apparatus comprises at least one barrier layer extending on a surface of at least one metal layer of at least one electrode.

[0022] In an embodiment, the dielectric layer comprises an Atomic Layer Deposition (ALD) grown aluminum oxide layer.

[0023] In an embodiment, the dielectric layer comprises a plasma enhanced

chemical vapor deposition (PECVD) layer.

[0024] Different non-binding example aspects and embodiments of the present invention have been illustrated in the foregoing. The embodiments in the foregoing are used merely to explain selected aspects or steps that may be utilized in implementations of the present invention. Some embodiments may be presented only with reference to certain example aspects of the invention. It should be appreciated that corresponding embodiments may apply to other example aspects as well.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] For a more complete understanding of example embodiments of the present invention, reference is now made to the following descriptions taken in connection with the accompanying drawings in which:

[0026] Fig. 1 illustrates profile/side view of a portion of a micro structure according to an embodiment of the invention;

[0027] Fig. 2 illustrates a micro structure of a MEMS switch according to an embodiment of the invention;

[0028] Fig. 3 illustrates a micro structure of a MIM capacitor according to an embodiment of the invention; and

[0029] Fig. 4 shows a flow chart of a method according to an embodiment of the invention.

DETAILED DESCRIPTON OF THE DRAWINGS

[0030] In embodiments, it is disclosed micro structures, such as microelectromechanical system (MEMS) switches, metal-insulator-metal (MIM) capacitors or passive components and circuits realized using inductors and capacitors. The integrated passive device (IPD) technology can also be used as an integration platform for multi-chip modules technology with hybrid integrated active circuits, for example.

[0031] The micro structure technology or integrated passive device (IPD) technology can be manufactured to any substrate that is suitable for thin film processing in clean rooms. Fused silica, quartz or high resistivity silicon are typically used for RF applications due to their good RF properties.

[0032] The micro structure or integrated passive device (IPD) layers can also be

post processed to active device wafers such as CMOS, SiGe or GaAs in order to have high Q passives and re-distribution layers (RDL).

[0033] The present invention and its potential advantages are understood by referring to Figs. 1 through 4 of the drawings. In this document, like reference signs denote like parts or steps.

[0034] Fig. 1 illustrates profile/side view of a portion of a micro structure 100 according to an embodiment of the invention.

[0035] In an embodiment, die (not shown) may be coupled on top of the micro structure 100. Furthermore, a circuit board (not shown) may be coupled on top or below of the micro structure 100. A solder ball may be utilized for coupling.

[0036] The micro structure 100 comprises a substrate 110 having a top surface 111, a first electrode 120 with a horizontal orientation parallel to the top surface 111 of the substrate 110, wherein the first electrode 120 is embedded within the substrate 110 so that a top surface 121 of the first electrode 120 coincides with the top surface 111 of the substrate 110.

[0037] In an embodiment, the top surface 121 of the first electrode 120 is polished or planarized to result with smooth top surface.

[0038] Vertical thickness of the first electrode 120 may be more than 5 μm, even more than 10 μm.

[0039] Fig. 2 illustrates a micro structure 200 of a microelectromechanical system (MEMS) switch according to an embodiment of the invention.

[0040] In an embodiment, the micro structure 200 of the microelectromechanical system (MEMS) switch comprises a substrate 110 having a top surface 111, a first electrode 120 with a horizontal orientation parallel to the top surface 111 of the substrate 110, wherein the first electrode 120 is embedded within the substrate 110 so that a top surface 121 of the first electrode 120 coincides with the top surface 111 of the substrate 110.

[0041] The micro structure 200 further comprises a dielectric layer 140 arranged on the top surface 121 of the first electrode 120, and a second electrode 130 arranged above the dielectric layer 140.

[0042] In an embodiment, the micro structure 200 further comprises a structural layer 131 that has a beam structure in which both ends thereof are fixed to the substrate 110, and the structural layer 131 comprises the second electrode 130 provided on a surface of the structural layer 131 facing the substrate 110.

[0043] In an embodiment, the micro structure 200 may further comprise at least one lower drive electrode 150 provided below the structural layer 131 and at least one upper drive electrode 151 provided on the surface of the structural layer 131 facing the substrate 110. Thus, when a potential difference is arranged between the upper drive electrode 151 and the lower drive electrode 150, the structural layer 131 is attracted towards the substrate 110 by an electrostatic attractive force, so that the second electrode 130 operating as an upper switch electrode and the first electrode 120 operating as a lower switch electrode come in contact with each other.

[0044] In an embodiment, the drive electrodes 150,151 may be integrated with first and second electrodes 120,130 or the first and the second electrodes 120,130 may be used to provide bias voltage for the potential difference.

[0045] Embodiments of the invention enable a new type of a MEMS switch device that has thicker bottom electrode than prior known systems. This lowers the loss of the MEMS switch technology and increases the quality factor (Q) when the technology is used as switch capacitor technology. The top surface 121 of the electrode 120 metallization may be polished/planarized resulting in smooth top surface. This is important especially for MEMS components because the structural layer 131 of embodiments does not have any steps as in prior known methods. In prior known methods, if thick metals (>1 μm) are deposited on the surface of a wafer, this causes steps to the structural layer of the MEMS component and thus potentially causes problems later on. RF power handling is also improved significantly because of thick metallizations for bottom electrode especially.

[0046] Thus, higher quality factor (Q) is achieved meaning lower resistive losses together with easier post processing compared to prior known methods. Furthermore, there are no step coverage problems in the dielectric layer 140 and no steps in the structural layer 131 because of the smooth bottom electrode 120. This results in higher voltage and power handling.

[0047] In general, MEMS RF switches have performance advantages over traditional semiconductor switches. For instance, the MEMS RF switch provides extremely low insertion loss when the switch is on, and exhibits a high attenuation level when the switch is off. In contrast to semiconductor switches, the MEMS RF switch features very low power consumption and a high frequency level (approximately 70 GHz).

[0048] In an embodiment, the MEMS RF switch has a MIM

(Metal/Insulator/Metal) structure, that is, an insulator/dielectric layer 140 is sandwiched between two electrodes 120,130. Therefore, when a bias voltage is applied to the MEMS RF switch (e.g. over drive electrodes 150,151 or the electrodes 120,130), the switch acts as a capacitor, allowing an AC signal to pass therethrough.

[0049] In an embodiment, Fig. 2 shows a cross-sectional view of a MEMS RF switch 200. The MEMS RF switch 300 includes a substrate 110, a first electrode 120, an insulator (dielectric layer) 140, and a second electrode 130. Particularly, the MEMS RF switch in Fig. 2 has a structural layer 131 where the second electrode 130 is arranged. Also, an air gap 160 exists between the second electrode 130 and the insulator 140.

[0050] When a bias voltage (over drive electrodes or main electrodes) is applied, at least one electrode may be thermally expanded and shifts in the direction of the insulator 140, thereby making contact with the insulator 140. As such, the first electrode 120, the insulator 140 and the second electrode 130 act as a capacitor together, and the RF switch 200 is turned on, which in turn allows an RF signal to pass therethrough at a predetermined frequency band. However, if the bias voltage is not applied, the second electrode 130 is separated from the insulator 140. As a result, the RF switch 200 is turned off and cannot allow the RF signal to pass therethrough.

[0051] In an embodiment, when the bias voltage is applied, a second bias electrode 130,151 is charged positively resulting in a buildup of positive (+) charges, and a first bias electrode 120,150 is charged negatively resulting in a buildup of (-) charges. Meanwhile, the charge on the insulator 140 may be maintained at 0, independent of the application of a bias voltage. In practice, however, charge buildup often occurs to the insulator 140. Thus, the detected charge on the insulator 140 is not always 0.

[0052] Fig. 3 illustrates a micro structure 300 of a MIM capacitor according to an embodiment of the invention.

[0053] In an embodiment, the micro structure 300 of the MIM capacitor comprises a substrate 110 having a top surface 111, a first electrode 120 with a horizontal orientation parallel to the top surface 111 of the substrate 110, wherein the first electrode 120 is embedded within the substrate 110 so that a top surface 121 of the first electrode 120 coincides with the top surface 111 of the substrate 110.

[0054] The micro structure 300 further comprises a dielectric layer 140 arranged

on the top surface 121 of the first electrode 120 and a second electrode 130 arranged on a top surface of the dielectric layer 140.

[0055] In an embodiment, a first horizontal end of the top surface 121 of the first electrode 120 is left uncovered by the dielectric layer 140 and the dielectric layer 140 extends over a second horizontal end of the top surface 121 of the first electrode 120, as shown in Fig. 3.

[0056] Furthermore, a first horizontal end of the top surface of the dielectric layer 140 may be left uncovered by the second electrode 130 and the second electrode 130 may extend to a second horizontal end of the top surface of the dielectric layer 140.

[0057] In an embodiment, the micro structure 300 may further comprise at least one connecting element 151,152 arranged on the substrate 110.

[0058] A first connecting element 151 may be configured to provide connection to the first horizontal end of the top surface 121 of the first electrode 120, for example. The first connecting element 151 may be a connecting pad, for example.

[0059] A second connecting element 152 may be configured to provide connection to a second horizontal end of the second electrode 130 adjacent to the second horizontal end of the top surface of the dielectric layer 140, for example. The second connecting element 151 may also be a connecting pad, for example. The second connecting element 152 may be comprised by the second electrode 130 and form a single element 130.

[0060] The first connecting element 151 and the second connecting element 152 may be arranged in opposite horizontal ends of the top surface of the dielectric layer 140.

[0061] In known systems, the thickness of the bottom electrode of MIM capacitor is typically between 0,1 μm and 1 μm. This limits the quality factor (Q) of MIM-capacitors because of the resistive losses.

[0062] Embodiments for the MIM capacitor enable thicker (5-10 μm) bottom electrode 120. The thick bottom electrode 120 is fabricated into the substrate 110 and planarized afterwards. This allows smooth surface 121 for the next processing steps. A dielectric layer 140 is grown after the metal layer of the first electrode 120 is provided. The dielectric layer 140 can be patterned if needed. On top of dielectric layer 140, a metal layer the second electrode 130 is grown.

[0063] This multi-purpose technology is suitable for a plurality of RF applications

and frequencies from Very High Frequency (VHF) to millimeter waves. The semiconductor apparatus 300 may further comprise thin film resistors, and IPD components between different metal layers, for example.

[0064] In an embodiment, at least one barrier layer may extending on a surface of at least one metal layer of electrodes 120,130 may be formed.

[0065] The barrier layer may comprise a low-pressure chemical vapor deposition nitride (LPCVD SiN) or a plasma enhanced chemical vapor deposition nitride (PECVD SiN).

[0066] The dielectric layer 140 may comprise an Atomic Layer Deposition (ALD) grown aluminum oxide layer or a plasma enhanced chemical vapor deposition (PECVD) layer, such as tetraethylorthosilicate (TEOS), for example. The substrate may comprise a silicon substrate layer 110.

[0067] In an embodiment, connecting elements 310,311 may comprise conductive pads that may be used to interconnect to at least one metal layer. Connection to an integrated passive device (IPD) of a semiconductor apparatus may also be arranged. The metal layer pads 310,311 of the semiconductor apparatus may be coupled to integrated passive device (IPD) terminals, for example.

[0068] The dielectric layer 140 may affect to the RF performance of the micro structure 300.

[0069] In an embodiment, different insulator deposition methods may be used to result different RF performances. RF performance may be optimized, for example, with a thin oxide layer 140 with minimal static charge.

[0070] In an embodiment, high resistive silicon substrates 110 may be used. Such high resistivity silicon substrates 110 with novel passivation layer(s) do not necessarily behave the same way as standard silicon wafers.

[0071] The thickness and material type of a dielectric layer 140 in contact with the micro structure substrate 110 has an effect to the performance of the micro structure 300. Especially RF performance is affected. The substrate 110 may comprise a glass or a silicon substrate in some implementations.

[0072] In an embodiment, a copper metal layer may be provided for high quality factor transmission lines and passive components, for example. Metal layers may be separated by a polyimide layer 140 and different metal layer elements of the same metal layer may be separated by a second polyimide material. As a further step, flip chip bumps may be deposited to allow component assembly to modules.

[0073] In an embodiment, SiO2 may be used as a dielectric material 140 but other materials are also available if higher capacitance densities are needed. For example, Ta2O5, HfO or ZrO2 have permittivity of 25, 16 and 20.

[0074] For IPD devices, resistance of the thin film resistor layer can be chosen according to application. For example, resistance of the standard process thin film resistors is good for matched RF terminations and resistor for resistive Wilkinson power dividers. Applications such as RF MEMS biasing circuits need resistance values preferably above 500 ohm.

[0075] Embodiments of the invention enable a new type of a MIM capacitor that has thicker bottom electrode than prior known systems. This lowers the resistive loss of the MIM capacitor technology and increases the quality factor when the technology is used. The top surface 121 of the electrode 120 metallization may be polished/planarized resulting in smooth top surface. This is important especially for MIM components because the dielectric layer 140 then has no step coverage problems as in prior known systems. In prior known methods, if thick metals (>1 μm) are deposited on the surface of a wafer, this causes steps to the dielectric layer 140 to embed the first electrode 120. The MIM capacitor of the embodiments has also higher breakdown voltage compared to the traditional MIM capacitors due to the polished and smooth surface. RF power handling is also improved significantly because of thick metallizations for bottom electrode 120 especially.

[0076] Thus, higher quality factor (Q) is achieved meaning lower resistive losses together with easier post processing compared to prior known methods. Furthermore, there are no step coverage problems in the dielectric layer 140 because of the smooth bottom electrode 120. This results in higher voltage and power handling.

[0077] Fig. 4 shows a flow chart of a method according to an embodiment of the invention.

[0078] A method of forming a micro structure 100,200,300 (see e.g. Figs. 1-3) is started in step 410. In step 420, a silicon substrate 110 having a top surface 111 is provided. In step 430, a first electrode 120 is formed with a horizontal orientation parallel to the top surface 111 of the substrate 110, wherein the first electrode 120 is embedded within the substrate 110 so that a top surface 121 of the first electrode 120 coincides with the top surface 111 of the substrate 110. In step 440, a top surface of the first electrode 120 is polished/polarized. In step 450, a dielectric layer

140 is formed on the top surface 121 of the first electrode 120. In step 460, a second electrode 130 is formed above the dielectric layer 140. In step 470, the method ends.

[0079] In an embodiment, a passivating layer comprises aluminium oxide and is formed on a surface of a silicon substrate to protect from effects caused by chemical interaction between the passivating layer and a conducting electrode by fabricating a barrier layer between the passivating layer and the conducting electrode.

[0080] A barrier layer comprising titanium and oxygen, tantalum and oxygen, zirconium and oxygen, hafnium and oxygen, or a combination of any of these, or a combination of any of these with aluminium and oxygen, on the passivating layer may be deposited by exposing the passivating layer in a reaction space to alternately repeated surface reactions of two or more different precursors, wherein at least one of the precursors is a precursor for oxygen, and forming the conducting electrode on the barrier layer deposited on the passivating layer by making a layer comprising aluminium paste on the barrier layer.

[0081] The reaction space may be subsequently pumped down to a pressure suitable for forming the passivating layer comprising aluminium oxide. The reaction space can be pumped down to the suitable pressure using e.g. a mechanical vacuum pump or, in the case of atmospheric pressure ALD systems and/or processes, gas flows can be set to protect the deposition zone from the atmosphere. The silicon substrate may be also heated to a temperature suitable for forming the passivating layer, the conductive layer or the dielectric layer by the used method. The silicon substrate can be introduced to the reaction space through e.g. an airtight load-lock system or simply through a loading hatch. The silicon substrate can be heated by e.g. resistive heating elements that also heat the entire reaction space.

[0082] After the silicon substrate and the reaction space have reached the targeted temperature and other conditions suitable for deposition, the silicon surface can be conditioned such that the deposited material may be essentially directly deposited on the silicon surface. This conditioning of the silicon surface on which the layer is to be deposited can include chemical purification of the surface of the silicon film from impurities and/or oxidation. Especially removal of oxide is beneficial when the silicon surface has been imported into the reaction space via an oxidizing environment, e.g. when transporting the exposed silicon surface from one deposition tool to another. The details of the process for removing impurities and/or oxide from the surface of the silicon film will be obvious to the skilled person in view of this

specification. In some embodiments of the invention the conditioning can be done ex-situ, i.e. outside the tool suitable for ALD-type processes.

[0083] After the silicon substrate has been conditioned, an alternate exposure of the deposition surface to different precursor chemicals may be started, to form a further layer directly on the silicon substrate. Each exposure of the deposition surface to a precursor results in the formation of additional deposit on the deposition surface, as a result of adsorption reactions of the corresponding precursor with the deposition surface.

[0084] A typical reactor suitable for ALD-type deposition comprises a system for introducing carrier gas, such as nitrogen or argon into the reaction space such that the reaction space can be purged from surplus chemical and reaction by-products before introducing the next precursor chemical into the reaction space. This feature together with the controlled dosing of vaporized precursors enables alternately exposing the substrate surface to precursors without significant intermixing of different precursors in the reaction space or in other parts of the reactor. In practice the flow of carrier gas is commonly continuous through the reaction space throughout the deposition process and only the various precursors are alternately introduced to the reaction space with the carrier gas.

[0085] Thickness of a further optional layer, e.g. a passivation layer, on the silicon substrate can be controlled by the number of exposures of the deposition surface to the different precursors. The thickness of the passivating layer is increased until a targeted thickness is reached, after which the at least one insulator layer is deposited.

[0086] Deposition of an insulator layer, e.g. a dielectric layer, in one embodiment of the invention, is carried out in an ALD-type process in the same deposition tool. In this case deposition of the insulator layer can begin simply by changing the precursor chemicals from those used for the deposition of the previous layer to those suitable for the deposition of the insulator layer.

[0087] In an embodiment, a bond wire package includes a micro structure 100,200,300 stacked on a die. The die may be disposed on a leadframe. The leadframe may be a pin grid array (PGA) package, a quad flat non-leaded (QFN) package or other package. The leadframe may comprise first pads and may be mounted on a PCB. An intermediate layer may be disposed between the micro structure 100,200,300 and the die and connect the micro structure 100,200,300 to

the die. Integrated passive devices (IPD) may also be arranged within the die.

[0088] The integrated passive device (IPD) includes an insulation layer or a second substrate, and the metallization layers. The insulation layer or the second substrate is disposed between the metallization layers. The insulation layer or the second substrate may include vias. The vias may be through glass vias (TGVs) or through silicon vias (TSVs). The vias may connect the first metallization layer and/or passive devices on the first metallization layer to the second metallization layer and/or passive devices on the second metallization layer. Each of the passive devices may be implemented on one or more layers of the integrated passive device (IPD).

[0089] Additional pads may be disposed on the micro structure 100,200,300. The pads may be connected to the first pads by bond wires. The pads may be connected to the metallization layer and/or passive devices in the metallization layer.

[0090] Without in any way limiting the scope, interpretation, or application of the claims appearing below, a technical effect of one or more of the example embodiments disclosed herein is improved RF power handling because of thick metallizations for bottom electrode especially. Another technical effect of one or more of the example embodiments disclosed herein is improved quality factor (Q). Another technical effect of one or more of the example embodiments disclosed herein is easier post processing compared to known methods. Another technical effect of one or more of the example embodiments disclosed herein is there are no step coverage problems in the dielectric layer and no steps in the structural layer because of the smooth bottom electrode. This results in higher voltage and power handling. Another technical effect of one or more of the example embodiments disclosed herein is an improved fabrication process of a micro structure. Another technical effect of one or more of the example embodiments disclosed herein is the provision of a reliable and compact semiconductor apparatus.

[0091] Although various aspects of the invention are set out in the independent claims, other aspects of the invention comprise other combinations of features from the described embodiments and/or the dependent claims with the features of the independent claims, and not solely the combinations explicitly set out in the claims.

[0092] It is also noted herein that while the foregoing describes example embodiments of the invention, these descriptions should not be viewed in a limiting sense. Rather, there are several variations and modifications that may be made

without departing from the scope of the present invention as defined in the appended claims.

CLAIMS

1. A micro structure (100,200,300) comprising:

a substrate (110) having a top surface (111);

a first electrode (120) with a horizontal orientation parallel to the top surface (111) of the substrate (110), wherein the first electrode (120) is embedded within the substrate (110) so that a top surface (121) of the first electrode (120) coincides with the top surface (111) of the substrate (110);

a dielectric layer (140) arranged on the top surface (121) of the first electrode (120); and

a second electrode (130) arranged above the dielectric layer (140).

2. The micro structure (100,200,300) of claim 1, wherein the top surface (121) of the first electrode (120) is polished.

3. The micro structure (100,200,300) of claim 1 or 2, wherein thickness of the first electrode (120) is more than 5 µm.

4. The micro structure (100,200) of any claim 1 to 3 comprising a microelectromechanical system (MEMS) switch, and further comprising:

a structural layer (131) having a beam structure in which both ends thereof are fixed to the substrate (110), and the structural layer (131) comprises the second electrode (130) provided on a surface of the structural layer (131) facing the substrate (110).

5. The micro structure (100,200) of claim 4, further comprising:

a lower drive electrode (150) provided below the structural layer (131) and an upper drive electrode (151) provided on the surface of the structural layer (131) facing the substrate (110), wherein when a potential difference is arranged between the upper drive electrode (151) and the lower drive electrode (150), the structural layer (131) is attracted towards the substrate (110) by an electrostatic attractive force, so that the second electrode (130) operating as an upper switch electrode and the first electrode (120) operating as a lower switch electrode come in contact with each other.

6. The micro structure (100,300) of any claim 1 to 3 comprising a metal-insulator-metal (MIM) capacitor, wherein

the second electrode (130) is arranged on a top surface of the dielectric layer (140).

7. The micro structure (100,300) of claim 6, wherein

a first horizontal end of the top surface (121) of the first electrode (120) is left uncovered by the dielectric layer (140) and the dielectric layer (140) extends over a second horizontal end of the top surface (121) of the first electrode (120).

8. The micro structure (100,300) of claim 7, wherein

a first horizontal end of the top surface of the dielectric layer (140) is left uncovered by the second electrode (130) and the second electrode (130) extends to a second horizontal end of the top surface of the dielectric layer (140).

9. The micro structure (100,300) of claim 8, further comprising:

a connecting element (310,311) arranged on the substrate (110) and configured to provide at least one of the following:

a first connecting element (310) configured to provide connection to the first horizontal end of the top surface (121) of the first electrode (120); and

a second connecting element (311) configured to provide connection to a second horizontal end of the second electrode (130) adjacent to the second horizontal end of the top surface of the of the dielectric layer (140).

10. A method of forming a micro structure (100,200,300), the method comprising:

providing a substrate (110) having a top surface (111);

forming a first electrode (120) with a horizontal orientation parallel to the top surface (111) of the substrate (110), wherein the first electrode (120) is embedded within the substrate (110) so that a top surface (121) of the first electrode (120) coincides with the top surface (111) of the substrate (110);

forming a dielectric layer (140) on the top surface (121) of the first electrode (120); and

forming a second electrode (130) above the dielectric layer (140).

11. A semiconductor apparatus comprising the micro structure (100, 200,300) of any claim 1 to 9.

12. The semiconductor apparatus of claim 11, further comprising an integrated passive device (IPD).

13. The semiconductor apparatus of claim 11 or 12, further comprising a passivation layer arranged between a silicon substrate layer and a first metal layer.

14. The semiconductor apparatus of any claim 11 to 13, further comprising at least one barrier layer extending on a surface of at least one metal layer of at least one electrode (120, 130).

15. The semiconductor apparatus of any claim 11 to 14, wherein the dielectric layer (140) comprises an Atomic Layer Deposition (ALD) grown aluminum oxide layer or a plasma enhanced chemical vapor deposition (PECVD) layer.

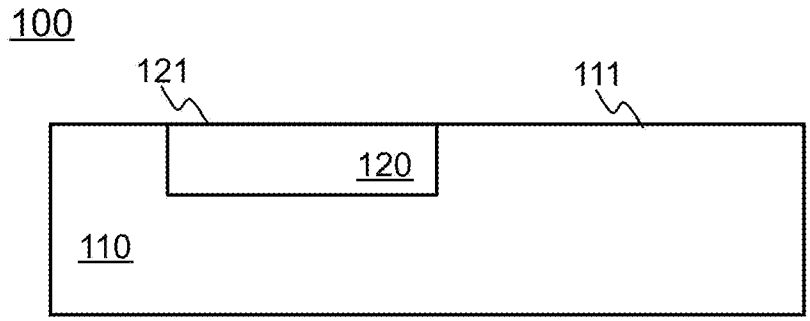

Fig. 1

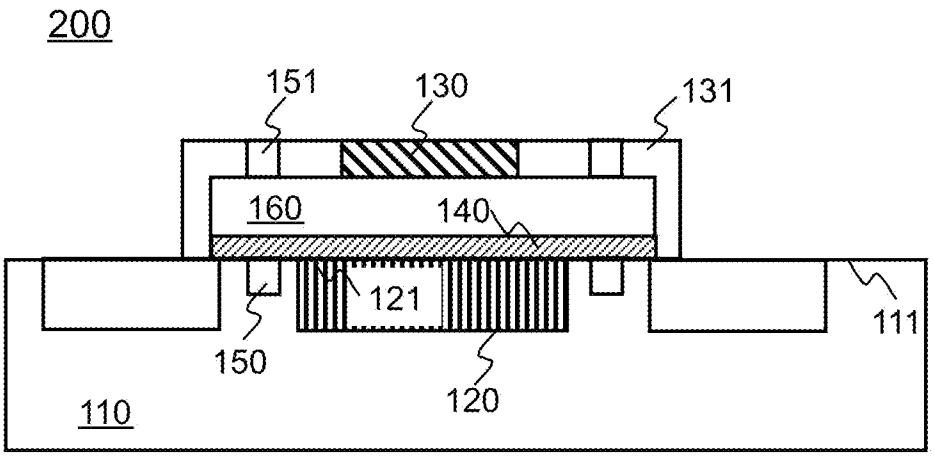

Fig. 2

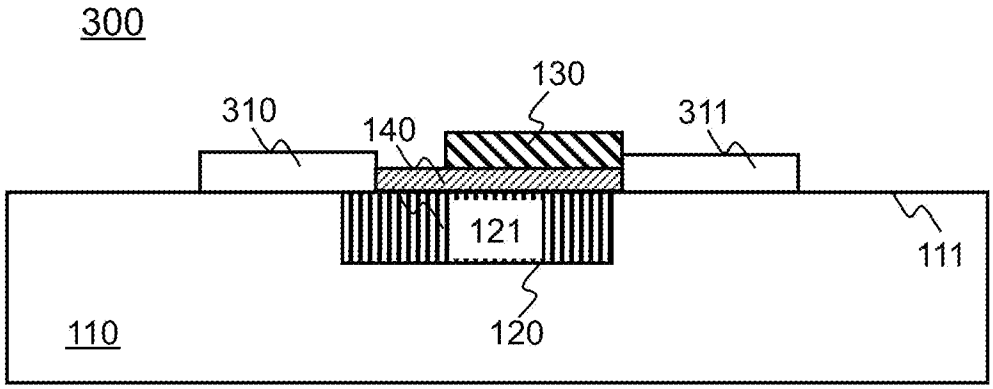
300
130
310
140
311
121
111
110
120

Fig. 3

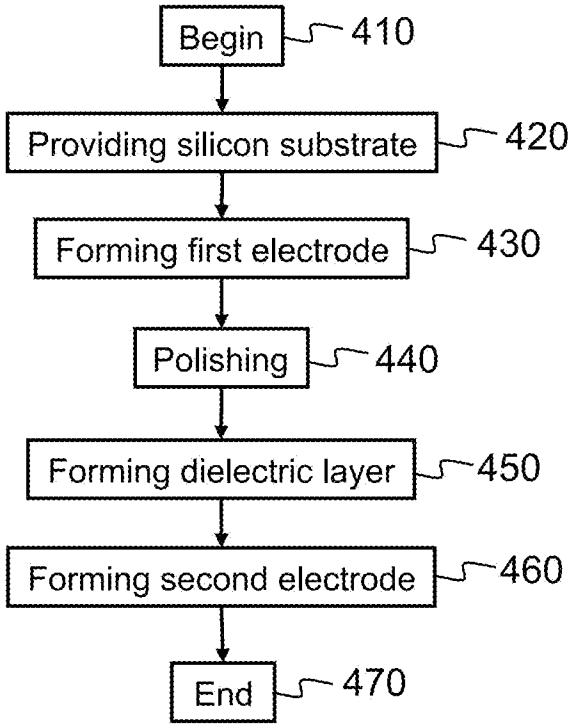
Begin
410
Providing silicon substrate
420
Forming first electrode
430
Polishing
440
Forming dielectric layer
450
Forming second electrode
460
End
470

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/FI2018/050467

A. CLASSIFICATION OF SUBJECT MATTER
INV. B81C1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
B81B B81C H01L H01G H01H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 180 976 B1 (ROY ARJUN KAR [US]) 30 January 2001 (2001-01-30) figures 1-12 column 6, line 21 - column 10, line 37 -----	1-3,6-15
X	US 2007/134835 A1 (FUKUDA HIROSHI [JP] ET AL) 14 June 2007 (2007-06-14) figures 1, 31-36 paragraph [0144] - paragraph [0145] -----	1-5

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 August 2018	24/08/2018

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/FI2018/050467

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 2007134835 A1	14-06-2007	CN 1979715 A	13-06-2007
		JP 2007157511 A	21-06-2007
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