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(54) SYSTEM HAVING MEMORY DEVICES OPERABLE IN A COMMON INTERFACE

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(57) **ABSTRACT**

DRAM and SRAM devices have a NAND interface mode (pins whose address and data are identical to one another are commonly used), directly being coupled to buses (an address/data bus and a control bus) of a NAND-type flash memory device that is connected to a microprocessor. Upon such a common interface mode, a DRAM device, an SRAM device, a NAND-type flash memory device, and a NOR-type flash memory device have the identical interface mode, and are independently (or individually) controlled by only one memory controller.

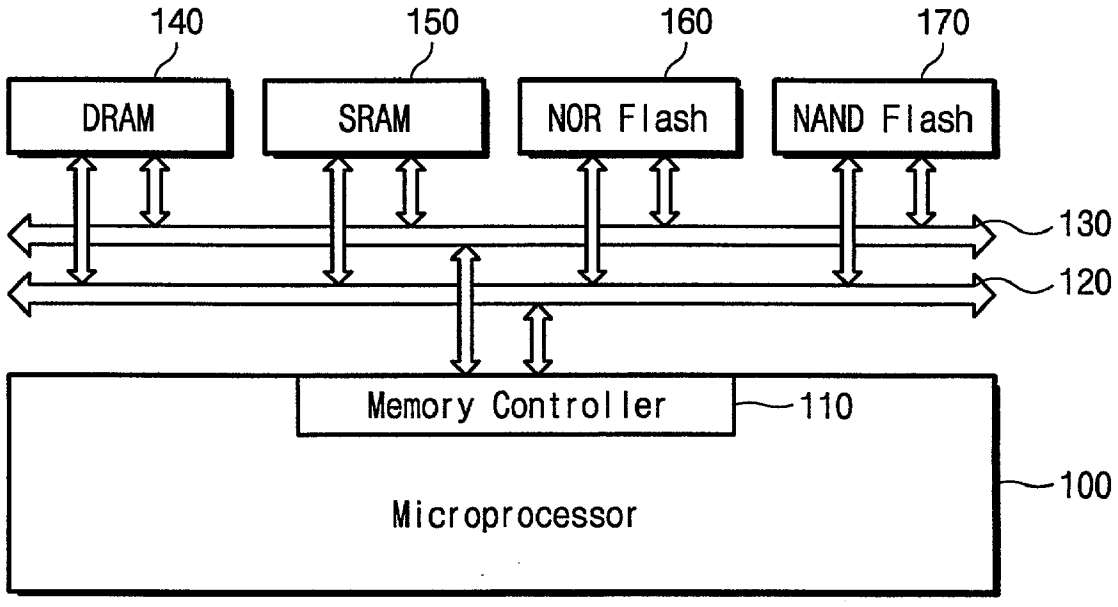


Fig. 1

(Prior Art)

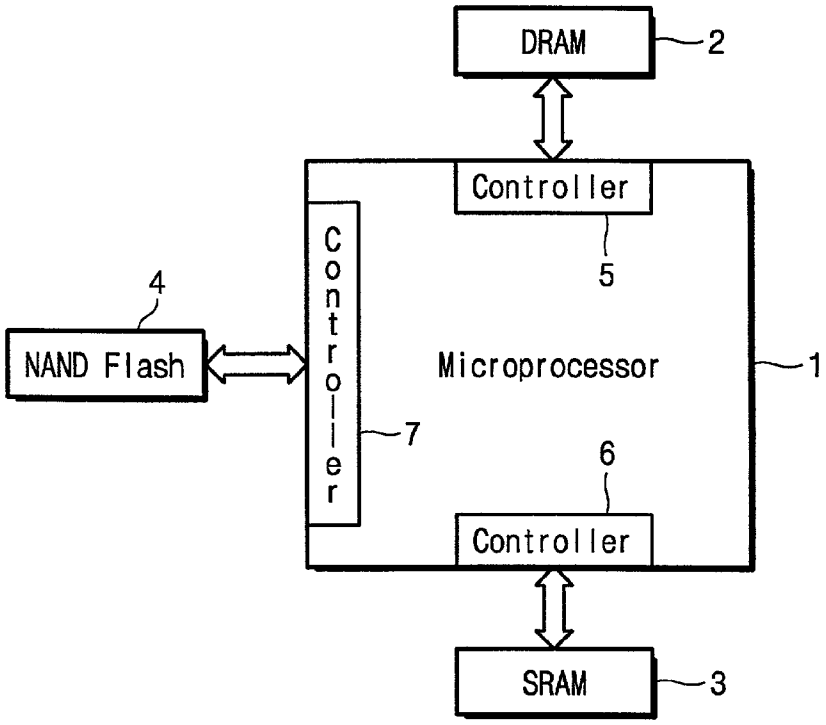


Fig. 2

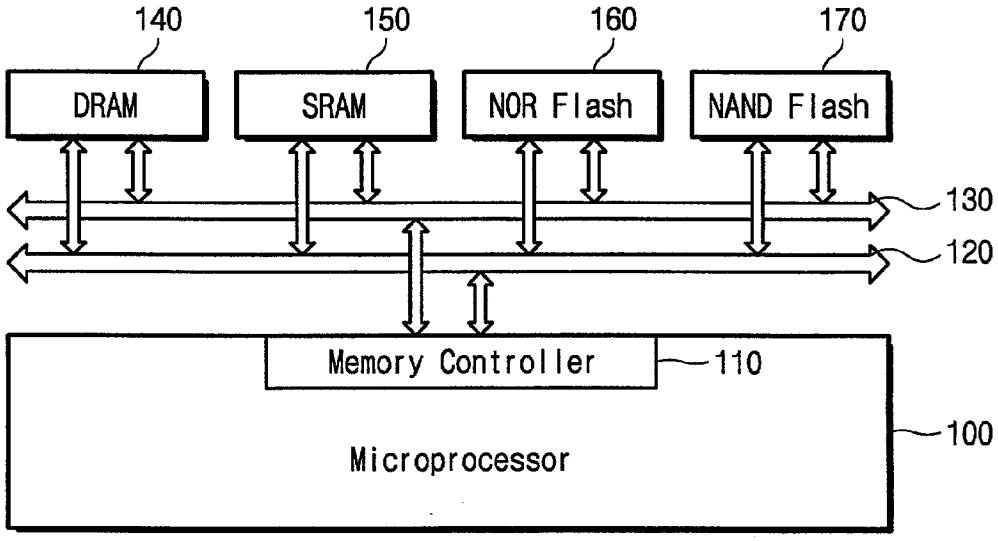
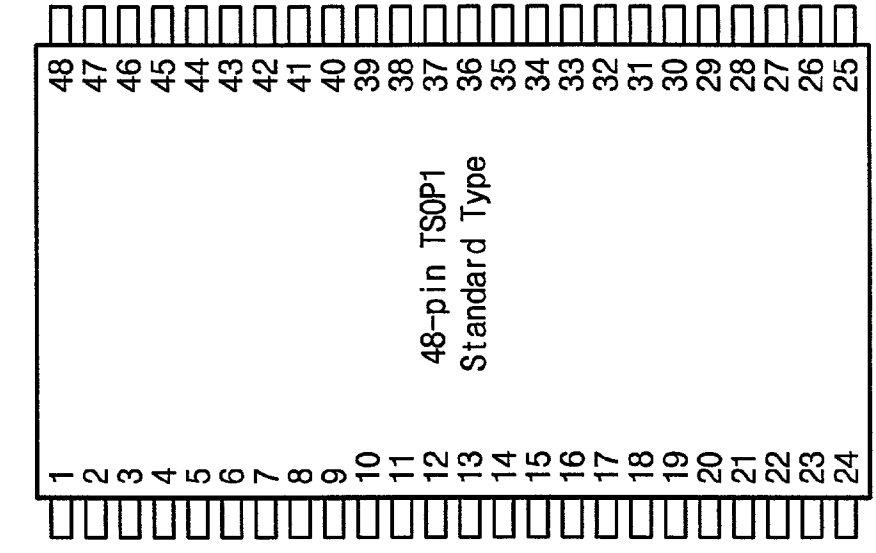


Fig. 3



128Mb NAND	16Mb DRAM	8Mb SRAM	8Mb NOR
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
I/O7	I/O7	I/O7	I/O7
I/O6	I/O6	I/O6	I/O6
I/O5	I/O5	I/O5	I/O5
I/O4	I/O4	I/O4	I/O4
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
VCC	VCC	VCC	VCC
VSS	VSS	VSS	VSS
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
I/O3	I/O3	I/O3	I/O3
I/O2	I/O2	I/O2	I/O2
I/O1	I/O1	I/O1	I/O1
I/O0	I/O0	I/O0	I/O0
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C

128Mb NAND	16Mb DRAM	8Mb SRAM	8Mb NOR
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
SE	RE	RE	SE
R/B	RE	RE	R/B
RE	CE	CE	RE
CE	CE	CE	CE
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
VCC	VCC	VCC	VCC
VSS	VSS	VSS	VSS
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
CLE	CLE	CLE	CLE
ALE	ALE	ALE	ALE
WE	WE	WE	WE
WP	N.C	N.C	WP
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C
N.C	N.C	N.C	N.C

Fig. 4

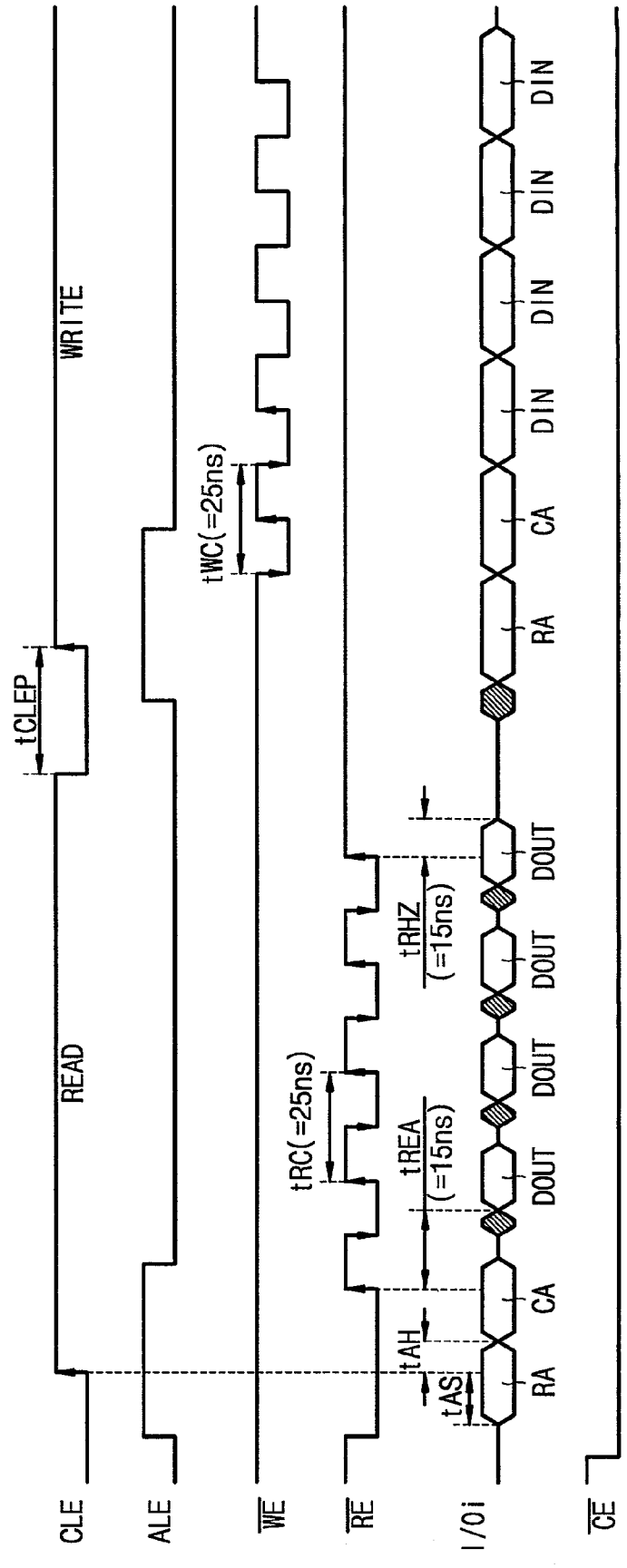

CLE
ALE
WE
RE
I/Oi
CE
READ
WRITE
tCLEP
tWC(=25ns)
tRC(=25ns)
tAH
tAS
tREA (=15ns)
tRHZ (=15ns)
RA
CA
DIN
DOUT

Fig. 5

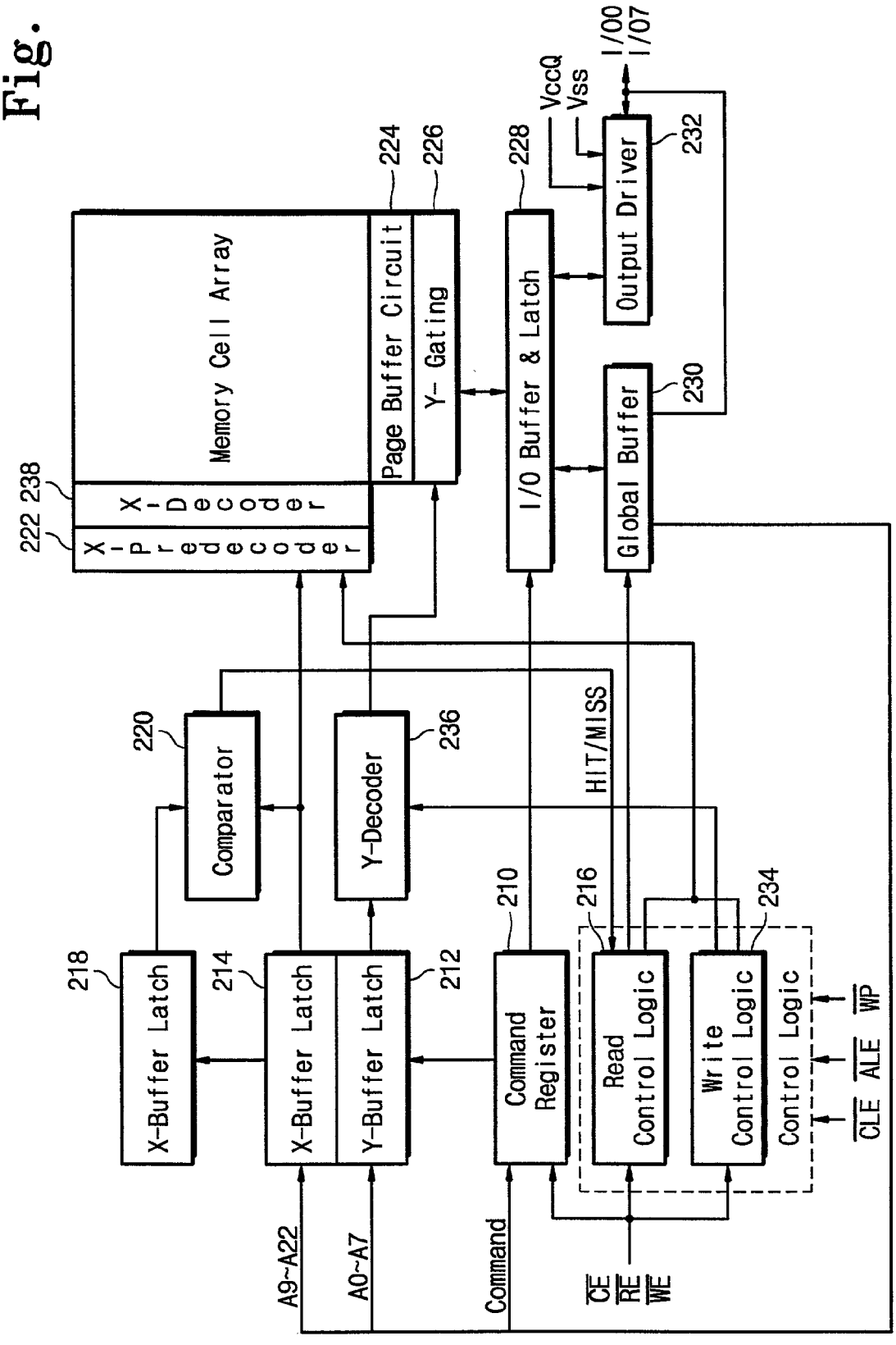

Memory Cell Array
Page Buffer Circuit
Y- Gating
I/O Buffer & Latch
Output Driver
Global Buffer
X-Predecoder
X-Decoder
Comparator
Y-Decoder
X-Buffer Latch
X-Buffer Latch
Y-Buffer Latch
Command Register
Read Control Logic
Write Control Logic
Control Logic
HIT/MISS
VccQ
Vss
I/O0
I/O7
222
238
220
236
218
214
212
210
216
234
224
226
228
232
230
A9~A22
A0~A7
Command
CE
RE
WE
CLE
ALE
WP

Fig. 6

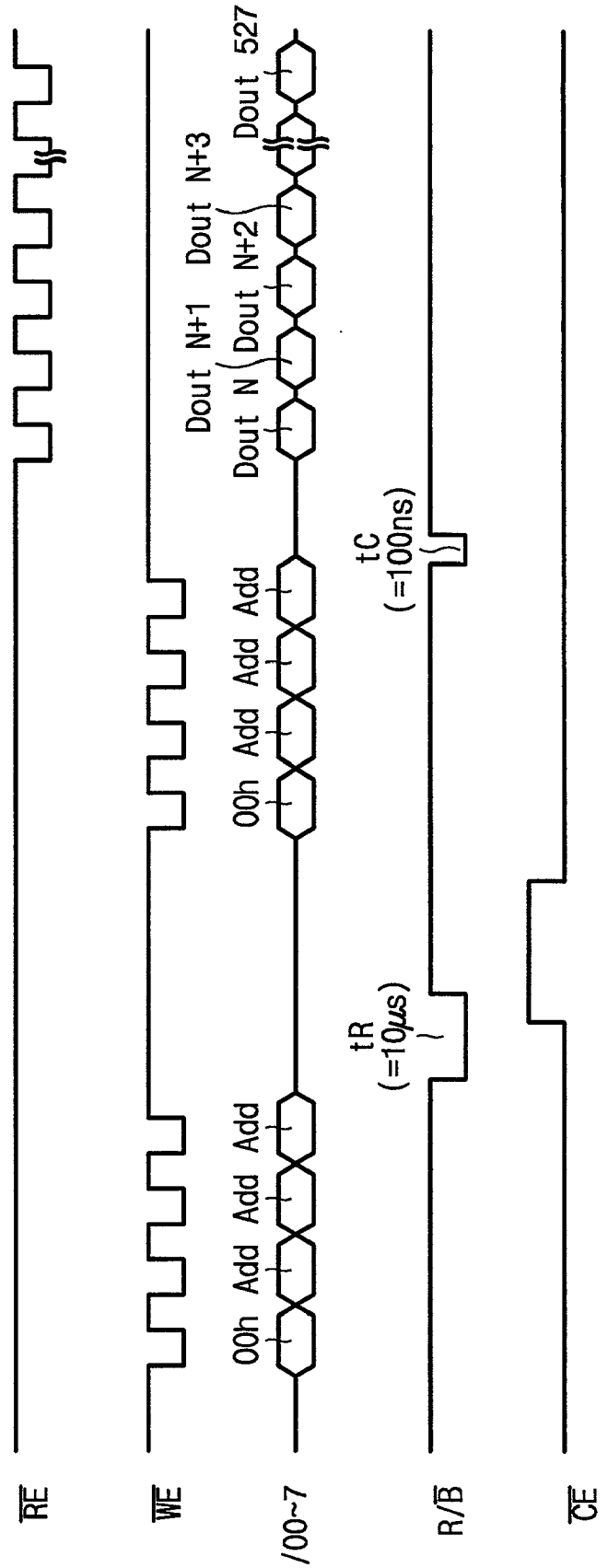

RE
WE
I/O0~7
R/B
CE
00h
Add
Add
Add
00h
Add
Add
Add
Dout N
Dout N+1
Dout N+2
Dout N+3
Dout 527
tR
(=10μs)
tC
(=100ns)

Fig. 7

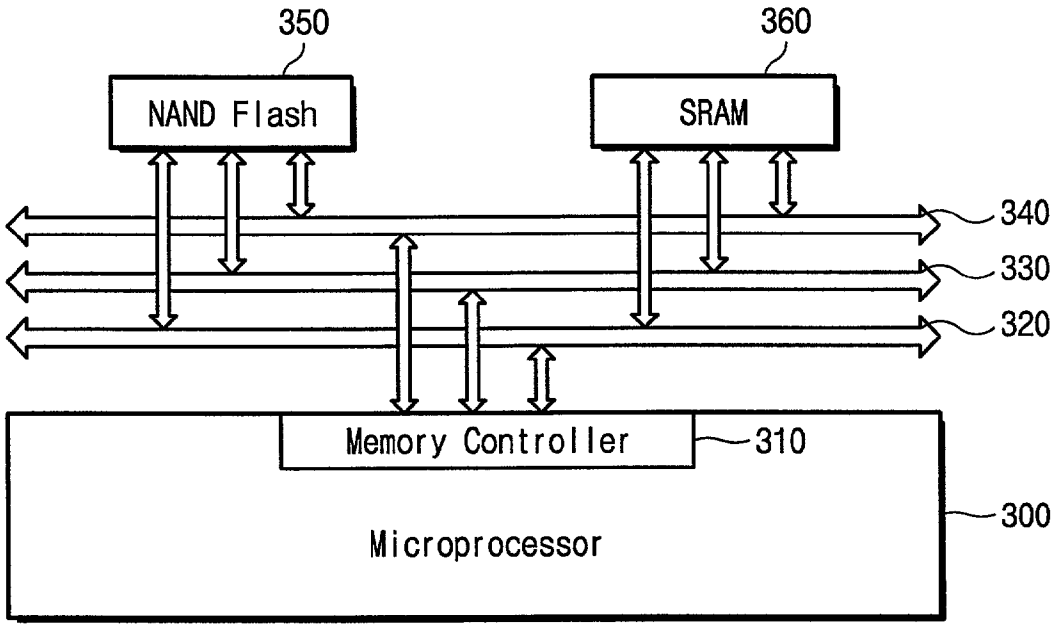

350
360
NAND Flash
SRAM
340
330
320
Memory Controller
310
300
Microprocessor

Fig. 8

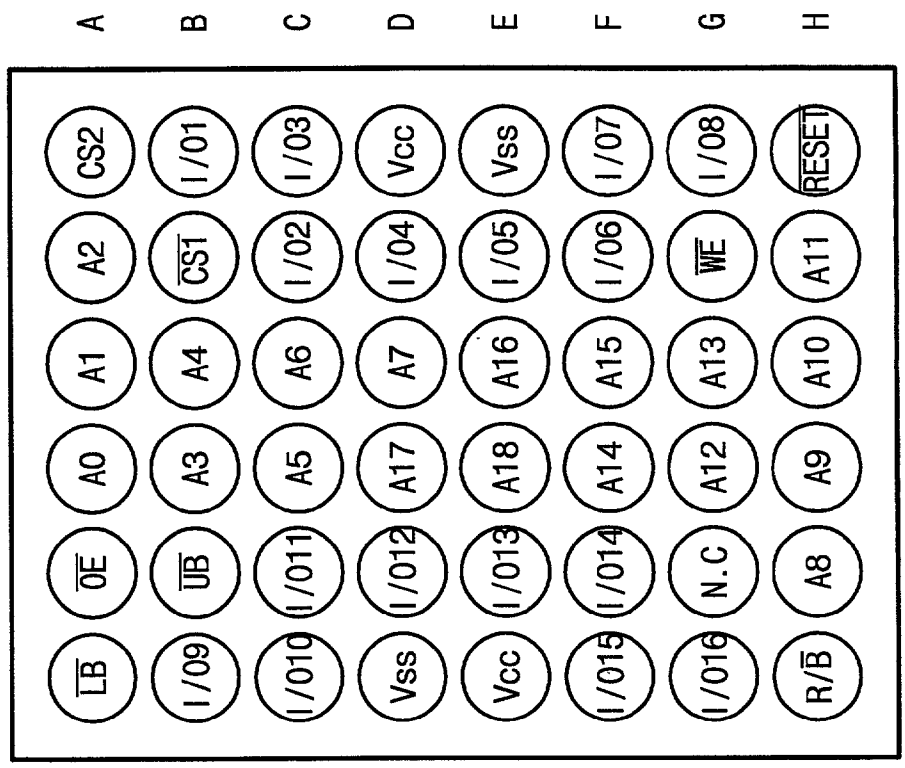

A B C D E F G H
1 2 3 4 5 6
LB OE A0 A1 A2 CS2
I/09 UB A3 A4 CS1 I/01
I/010 I/011 A5 A6 I/02 I/03
Vss I/012 N.C A7 I/04 Vcc
Vcc I/013 N.C A16 I/05 Vss
I/015 I/014 A14 A15 I/06 I/07
I/016 N.C A12 A13 WE I/08
N.C A8 A9 A10 A11 N.C
A B C D E F G H
1 2 3 4 5 6
LB OE A0 A1 A2 CS2
I/09 UB A3 A4 CS1 I/01
I/010 I/011 A5 A6 I/02 I/03
Vss I/012 A17 A7 I/04 Vcc
Vcc I/013 A18 A16 I/05 Vss
I/015 I/014 A14 A15 I/06 I/07
I/016 N.C A12 A13 WE I/08
R/B A8 A9 A10 A11 RESET

Fig. 9A

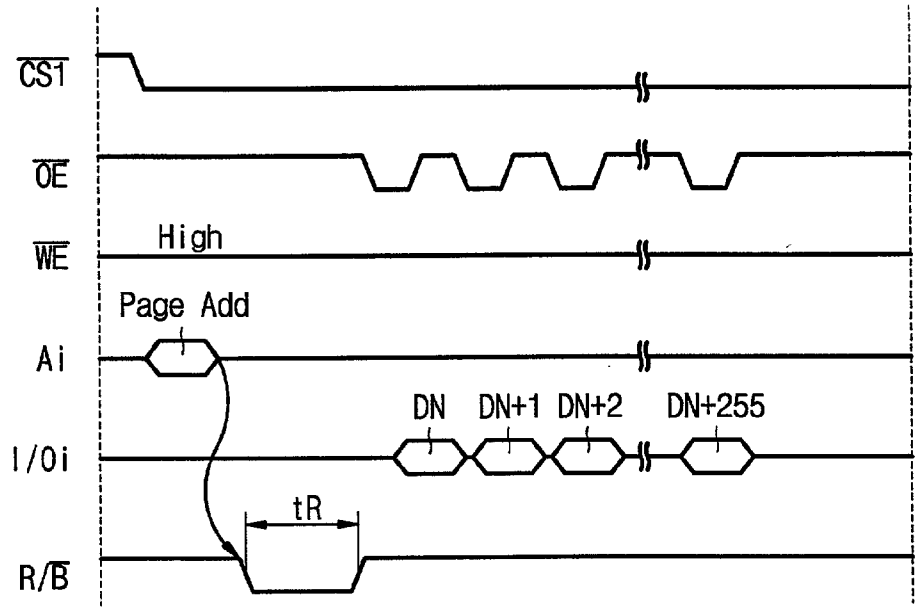

CS1
OE
WE
High
Page Add
Ai
DN
DN+1
DN+2
DN+255
I/Oi
tR
R/B

Fig. 9B

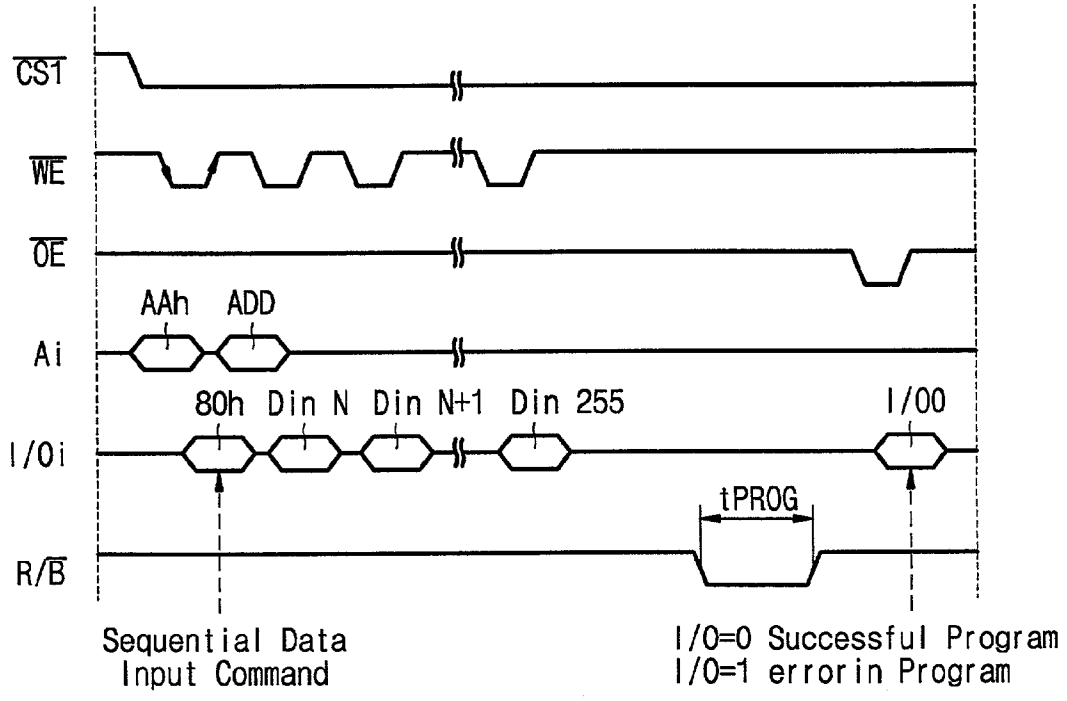
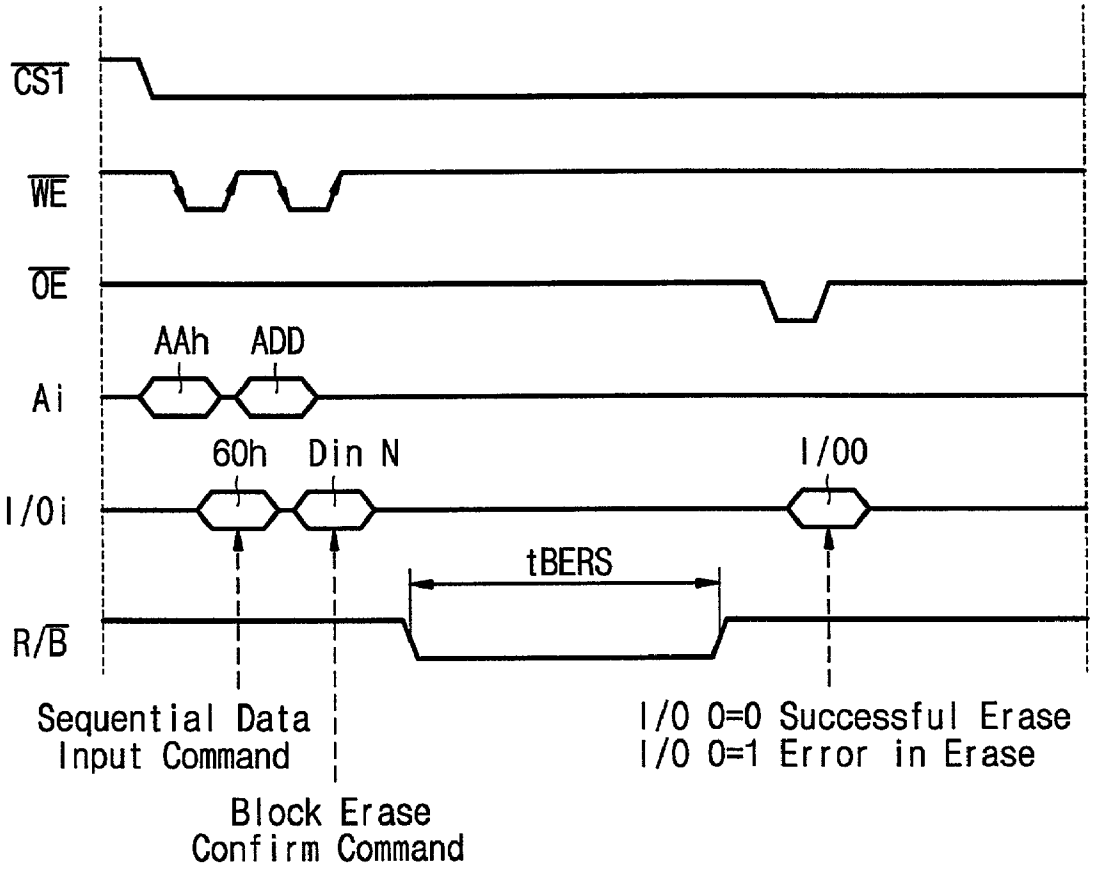

CS1
WE
OE
AAh
ADD
Ai
80h
Din N
Din N+1
Din 255
I/O0
I/Oi
tPROG
R/B
Sequential Data
Input Command
I/O=0 Successful Program
I/O=1 error in Program

Fig. 9C


CS1
WE
OE
AAh
ADD
Ai
60h
Din N
I/00
I/0i
tBERS
R/B
Sequential Data Input Command
Block Erase Confirm Command
I/0 0=0 Successful Erase
I/0 0=1 Error in Erase

SYSTEM HAVING MEMORY DEVICES OPERABLE IN A COMMON INTERFACE

[0001] This application relies for priority upon Korean Patent Application No. 2000-03708, filed on Jan. 26, 2000, the contents of which are herein incorporated by reference in their entirety.

FIELD OF THE INVENTION

[0002] The present invention relates to electric devices and, more particularly, to a system having memory devices operable in a common interface.

BACKGROUND OF THE INVENTION

[0003] Recently, various memory devices are employed in a computer- or microprocessor-based system. As storage elements within such a system, volatile semiconductor memory devices such as a dynamic random access memory device (DRAM) or a static random access memory device (SRAM), and non-volatile semiconductor memory device such as a NAND-type flash memory device and a NOR-type flash memory device are required therein. The volatile and non-volatile semiconductor memory devices are controlled by their corresponding memory controllers. Such a memory controller is disclosed in U.S. Pat. No. 5,684,978 entitled "SYNCHRONOUS DRAM CONTROLLER WITH MEMORY ACCESS COMMANDS TIMED FOR OPTIMIZED USE OF DATA BUS", and U.S. Pat. No. 5,893,136 entitled "MEMORY CONTROLLER FOR INDEPENDENT SUPPORTING SYNCHRONOUS AND ASYNCHRONOUS DRAM MEMORIES".

[0004] As well known in the art, DRAM and SRAM devices adopt an interface mode that address pins and data pins are separated from each other while a NAND-type flash memory device adopts an interface mode (i.e., "multiplexing interface mode") that address pins and data pins are commonly used. The above NAND-type flash memory device is disclosed in a data book "Flash Memories" published in Samsung Electronics Co., Ltd., March 1998. The above DRAM device is disclosed in a data book "MOS Memory" published by Samsung Electronics Co., Ltd., 1995. And, the above SRAM device is disclosed in a data book "SRAM/FIFO" published in Samsung Electronics Co., Ltd., April 1995.

[0005] A conventional system is schematically shown in **FIG. 1**. The system includes a microprocessor **1** (or a central processing unit, a baseband modem of a communication terminal, a codec, etc.), a DRAM device **2**, an SRAM device **3**, and a NAND-type flash memory device **4**. The microprocessor **1** includes memory controllers **5**, **6**, and **7** that control the DRAM device **2**, the SRAM device **3**, and the NAND-type flash memory device **4**, respectively. The memory controller **5** for the only DRAM device transfers address and control signals to the DRAM device **2** through a corresponding bus. The memory controller **6** for the only SRAM device transfers address and control signals to the SRAM device **3** through a corresponding bus. And, the memory controller **7** for the NAND-type flash memory device transfers address and control signals to the NAND-type flash memory device **4** through a corresponding bus.

[0006] Since memory devices used in a system have pin arrangements and interface modes that are different from each other, each memory controller for the only memory devices must be provided to the microcontroller **1**, as can be seen in **FIG. 1**. This causes increase in a size of the microcontroller **1** (or a central processing unit, a baseband modem of a communication terminal, a codec, etc.). Therefore, memory devices having pin arrangements and interface modes that are different from each other cannot be mounted with a chip-size package (CSP).

SUMMARY OF THE INVENTION

[0007] It is therefore an object of the present invention to provide a system having NAND interface DRAM, SRAM, and NOR-type flash memory devices which are commonly connected to one bus.

[0008] It is another object of the present invention to a NAN-type flash memory device having an SRAM interface mode.

[0009] It is further another object of the present invention to provide a NAND-type flash memory device capable of enhancing a bus use efficiency.

[0010] According to one aspect of the present invention, a semiconductor memory device includes a random access memory chip and a package having the random access memory chip. The package includes a plurality of pins for electrically connecting the random access memory chip to an external device. The plural pins provide memory functions commonly to a random access memory device and an electrically erasable and programmable non-volatile semiconductor memory device. Each of the pins is arranged at a position of a pin corresponding to the non-volatile semiconductor memory device.

[0011] The plural pins is composed of input/output pins for receiving address and data, power supply voltage pins, ground voltage pins, a read enable pin, a chip enable pin, a command latch enable pin, an address latch enable pin, and a write enable pin.

[0012] According to another aspect of the present invention, a semiconductor memory device includes an electrically erasable and programmable non-volatile semiconductor memory chip, and a package having the non-volatile semiconductor memory chip. The package includes a plurality of pins for electrically connecting the chip to an external device. The plural chips are composed of a first group of pins and a second group of pins. The pins of the first group provide memory functions commonly to a static random access memory device and an electrically erasable and programmable non-volatile semiconductor memory device. And, the pins of the first group are arranged at a position of a corresponding pin of the static random access memory device, respectively. The pins of the second group provide functions of unused non-volatile semiconductor memory device to the static random access memory. The pins of the second group are arranged at a position of an unused pin of the static random access memory, respectively.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] **FIG. 1** is a block diagram showing a system configuration in accordance with a prior art.

[0014] **FIG. 2** is a block diagram showing a system configuration in accordance with one embodiment of the present invention.

[0015] **FIG. 3** is a diagram showing pin arrangements of a DRAM, an SRAM, a NOR-type flash memory, and a NAND-type flash memory in accordance with the present invention.

[0016] **FIG. 4** is a timing diagram showing read and write operations of NAND interface DRAM and SRAM shown in **FIG. 2**.

[0017] **FIG. 5** is a block diagram showing a NAND-type flash memory device shown in **FIG. 2**.

[0018] **FIG. 6** is a timing diagram showing a read operation of a NAND-type flash memory device shown in **FIG. 5**.

[0019] **FIG. 7** is a block diagram showing a system configuration in accordance with another embodiment of the present invention.

[0020] **FIG. 8** is a diagram showing a ball pin arrangement of an SRAM and a NAND-type flash memory shown in **FIG. 7**.

[0021] **FIG. 9**A through **FIG. 9C** are timing views showing read/program/block erase operations of an SRAM interface NAND-type flash memory device shown in **FIG. 8**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0022] The present invention will now be described more fully hereinafter with reference to accompanying drawings wherein preferred embodiments of the invention are illustrated.

[0023] The present invention provides pin arrangements, structures, and a method of operating DRAM, SRAM, and NAND-type flash memory devices. The DRAM and SRAM devices have a NAND interface mode (pins whose address and data are identical to each other are used), being directly coupled to buses (an address/IO bus and a control bus) of a NAND-type flash memory device that is coupled to a microprocessor and a central processing unit or a multi-chip. Also, a NOR-type flash memory device has the NAND interface mode, being directly coupled to buses same as the NAND-type flash memory device. And, the NAND-type flash memory device an SRAM interface mode (an address pin and an input/output pin are separated from each other), being directly coupled to buses (e.g., an address bus, a data bus, and a control bus) same as the SRAM device. In brief, the DRAM, SRAM, NAND-type flash memory, and NOR-type flash memory devices have the identical interface mode, and are independently (or individually) controlled by only one memory controller. Pin arrangements, structures, and an operating method of memory devices having the identical interface mode are described in detail.

[0024] **FIG. 2** schematically shows a construction of a system in accordance with the present invention. A microprocessor **100** includes a memory controller **110** to which address/data bus **120** for transferring address and data and a control bus **130** for transferring a plurality of control signals (e.g., $\overline{CE}$, $\overline{RE}$, $\overline{WE}$, ALE, and CLE) are connected. A DRAM device **140**, an SRAM device **150**, a NOR-type flash memory device **160**, and a NAND-type flash memory device **170** are directly coupled to the buses **120** and **130**. That is, the memory devices have the identical interface mode. Specifically, the DRAM device **140**, the SRAM device **150**, and the NOR-type flash memory device **150** have the NAND interface mode, being directly coupled to the buses **120** and **130** same as the NAND-type flash memory device **160**.

[0025] **FIG. 3** illustrates pin arrangements of memory devices supporting the NAND interface mode. Pin arrangements of a 16 Mb DRAM device, an 8 Mb SRAM device, and an 8 Mb NOR-type flash memory device are compared with those of 128 Mb NAND-type flash memory 48-pin TSOP1 package products. A first group of pins providing memory functions to all memory devices are included in a DRAM device **140**, an SRAM device **150**, a NOR-type flash memory device **160**, and a NAND-type flash memory device **170**. The pins of the first group includes eight input/output pins I/**00**-I/**07**, two power supply voltage pin VCC, two ground voltage pins VSS, and five function pins, i.e., a chip enable pin $\overline{CE}$ for selecting a corresponding memory device, a read enable pin $\overline{RE}$, a write enable pin $\overline{WE}$, an address latch enable pin ALE, and a command latch enable pin CLE.

[0026] As shown in **FIG. 3, a** second group of three function pins are provided, which are included only in the NOR-type flash memory device **150** and the NAND-type flash memory device **160**. The pins of the second group are arranged, corresponding to non-connection (N.C) pins of the DRAM and SRAM devices **140** and **150**, commonly connecting all the memory devices to the identical buses. That is, a spare array enable pin $\overline{SE}$ is arranged, being located at each 6th pin (N.C) of the memory device **140** and **150**. A ready/$\overline{busy}$ pin R/$\overline{B}$ are arranged, being located at each 7th pin (N.C) of the memory device **140** and **150**. A write protect pin $\overline{WP}$ is arranged, being located at each 19th pin (N.C) of the memory device **140** and **150**. Out of 48 pins, 28 pins are non-connection (N.C) pins, as can be seen in **FIG. 3**.

[0027] An input of the spare array enable pin $\overline{SE}$ controls spare array selection that is provided to a corresponding flash memory device. An input of the write protect pin $\overline{WP}$ controls write/erase protect that may occur in power transition of $\overline{WP}$. When the input of $\overline{WP}$ is enabled, an internal high voltage generator (not shown) in a memory device is reset. An output of the ready/$\overline{busy}$ pin R/$\overline{B}$ indicates an operation state of a corresponding flash memory device. When the output of R/$\overline{B}$ is low, it is indicated that program, erase, and read operations of the flash memory device are proceeding. The memory devices **140**, **150**. **160**, and **170** have pin arrangements that are identical to one another, to be operable in the identical interface mode (specifically, an interface mode of a NAND-type flash memory device). Thus, all the memory devices **140**, **150**, **160**, and **170** are directly coupled to the identical buses (i.e., an address/IO bus and a control bus). Therefore, one memory controller is constructed in a microcontroller (or a baseband modem of a communication terminal or a multi-chip that a plurality of devices are constructed in one chip), controlling operations of all the memory devices **140**, **150**, **160**, and **170**. Further, since the memory devices **140**, **150**, **160**, and **170** have pin arrangements that are identical to one another, they can easily be constructed in a chip-size package.

[0028] **FIG. 4** illustrates a timing diagram for explaining read/write operations of DRAM and SRAM devices having the foregoing interface mode. Assuming that a chip enable signal $\overline{CE}$ for selecting a DRAM device **140** is enabled. Under the assumption, a read operation is described as follows. When a command latch enable signal CLE transi-

tions from low level to high level, a row address RA is provided to the DRAM device **140** through input/output pins I/Oi (i=**0-7**). Then, a column address CA is provided to the DRAM device **140** through I/Oi when a read enable signal $\overline{RE}$ transitions from low level to high level. After a predetermined access time tREA, data read-out from a memory cell array is synchronized with $\overline{RE}$ through I/Oi coupled to an address/data bus **120**, being transferred to a bus **120** coupled to a microprocessor **100**. The read operation is finished when CLE transitions from high level to low level.

[**0029**] Under the identical assumption, a read operation is described as follows. When the command latch enable signal CLE transitions from low level to high level again after a row precharge time tCLEP, a row address RA is provided through input/output pins I/Oi (i=**1-7**). A column address CA is then provided through I/Oi when $\overline{CE}$ transitions from low level to high level. And then, data DIN synchronized with a write enable signal $\overline{WE}$ inputs through data input/output pins I/Oi coupled to the bus **120**, and is stored in the memory cell array according to a late write mode that is known in the art.

[**0030**] In **FIG. 4**, comparing AC characteristic parameters of NAND interface DRAM and SRAM devices with those of conventional DRAM and SRAM devices, the comparison results are shown in the following tables.

TABLE 1

Conventional DRAM	tCAC	tHPC	tDOH	TRP
NI-DRAM	tREA	TRC(tWC)	tRHZ	TCLEP
Speed	15 ns	25(25) ns	15 ns	30 ns

(NI-DRAM: NAND interface DRAM)

[**0031**]

TABLE 2

Conventional SRAM	TACCB	tCLK	tOHZ	tAS/tAH	tACC2
NI-SRAM	TREA	TRC(tWC)	tRHZ	tAS/tAH	tACC
Speed	15 ns	25(25) ns	15 ns	20/0 ns	100 ns

(NI-SRAM: NAND interface SRAM)

[**0032**] Read/write operations of a NAND interface SRAM device according to the present invention are also based upon a timing view shown in **FIG. 4**, so that description thereof will be skipped. The read and write operations of the NAND interface DRAM/SRAM devices are classified using signals $\overline{RE}$ and $\overline{WE}$. For example, the read operation is carried out in moving the read enable signal $\overline{RE}$ while the write operation is carried out in moving the write enable signal $\overline{WE}$.

[**0033**] By the above description, it is known that the command latch enable pin CLS and the read enable pin $\overline{RE}$ substitute for a row address strobe pin $\overline{RAS}$ and a row address strobe pin $\overline{CAS}$ of the conventional DRAM device. Since address and data are provided through the identical input/output pins, collision between an output of read-out data by a first address and an input of a second address may occur in consecutive read operations. In order to overcome the collision, an address (i.e., burst address) for the consecutive read operations is provided into a NAND interface DRAM device. The burst address is created using a burst counter that is well known in the art, and is driven by the read enable signal $\overline{RE}$. A refresh operation of the NAND interface DRAM may be carried out using the command latch enable signal CLE and the read enable signal $\overline{RE}$. For example, an ROR refresh (/RAS only refresh) of a conventional DRAM device is carried out using CLE, and a CBR refresh (/CAS before /RAS refresh) is carried out using CLE and $\overline{RE}$.

[**0034**] In the NAND interface SRAM device, $\overline{RE}$ is used as a signal $\overline{ADV}$ for controlling creation of a burst address in a bust address counter of a conventional SRAM device, and as an output enable signal $\overline{OE}$. For example, when $\overline{ADV}$ is enabled, the burst address counter internally creates a series of burst addresses using an initial address. When $\overline{OE}$ retains low level, data read out from a memory cell array of a NAND interface SRAM device is outputted through data input/output pins I/Oi. The NAND interface SRAM device of this invention uses a second-inputted address out of addresses that are inputted in twice, as a burst address.

[**0035**] A NAND flash memory device of this invention is schematically shown in **FIG. 5**, and an operation timing diagram for describing a read operation is shown in **FIG. 6**. With reference to **FIG. 6**, the read operation will now be described more fully hereinafter.

[**0036**] Referring to **FIG. 5, a** command 00h, inputted through input/output pins I/Oi (i=**0-7**), to indicate a read operation, is transferred to a command register **210**. Consecutively, column addresses **A0-A7** and page (row) addresses **A8-A16** and **A17-A23** are latched to a Y-buffer latch **212** and an X-buffer latch **214**, respectively. Based upon control of a read control logic **216**, a ready/$\overline{busy}$ signal R/$\overline{B}$ retains low level for a predetermined time so as to carry out a practical read operation (i.e., data stored in memory cells of a selected row is latched to a page buffer circuit). A NAND-type flash memory device is unselected so as to carry out a read/write operation of other memory device (i.e., a chip enable signal $\overline{CE}$ corresponding to the NAND-type flash memory device transitions from low level to high level).

[**0037**] If the read/write operation of other memory device is completed and the chip enable signal $\overline{CE}$ for selecting the NAND-type flash memory device has a high-to-low transition, the command 00h, a column address, and a page address are transferred to a command register **210**, a Y-buffer latch **212**, and an X-buffer latch **214**, respectively. At this time, a previous page address latched to the X-buffer latch **214** is transferred to an X-buffer latch **218**. And, a comparator **220** compares whether the latched address to the X-buffer latches **214** and **218** are matched with each other, outputting a signal HIT/MISS as a comparison result. In response to, for example, a high-level signal HIT/MISS indicating that two addresses are matched with each other, a read control logic **216** controls a sensing operation associated with a currently inputted address (i.e., an address latched to the X-buffer latch **214**) not to be carried out. For example, an X-predecoder **222** is disabled by the read control logic **216**. **16**. The data, which is latched to a page buffer circuit **224** by a sensing operation that is previously carried out, is then transferred to a bus **120** through the input/output pins I/Oi by the control of the read control logic **216**.

[**0038**] In such a read operation, when a previously inputted page (row) address is matched with a currently inputted page (row) address, a practical read operation (specifically,

sensing operation) is not carried out. And, data (corresponding to a previously inputted page) latched to the page buffer circuit **224** is outputted to the outside, as data required to a current read operation. As shown in **FIG. 6, a** time tC (e.g., 100 ns) required in the current read operation is shorter than a time tR (e.g., 10 μs) required in a previous read operation. Therefore, other memory device can uses the identical buses (to which an SRAM, a DRAM, a NOR-type flash memory, and a NAND-type flash memory are coupled) for a shortened time. This leads to enhancement of bus use efficiency of memory devices that are established by a common interface mode.

[**0039**] A system configuration according to another embodiment is schematically shown in **FIG. 7**. A microprocessor **300** includes a memory controller **310** that generates a control signal for controlling an operation of a memory device and address signals. An address bus **320** for transferring an address, a data bus **330** for transferring data, and a control bus **340** for transferring control signals are connected to the memory controller **310**. A NAND-type flash memory device **350** and an SRAM device **360** are directly coupled to the buses **320**, **330**, and **340**. That is, each memory device has the identical interface mode. Specifically, each memory device has an SRAM interface mode (an address pin and a data pin are separated from each other), directly being coupled to the buses **320**, **330**, and **340** same as the SRAM device **360**. A ball pin arrangement satisfying such a situation is shown in **FIG. 8**.

[**0040**] Referring now to **FIG. 8, a** ball pin arrangement of a NAND-type flash memory device is compared with that of an SRAM 48-pin FBGA package product. A first group of pins providing common memory operations to both memory devices are included in a NAND-type flash memory device **350** and an SRAM device **360**. The pins of the first group are composed of address pins **A0-A16** for receiving an address, input/input pins I/O**1**-I/O**16** for receiving data, two power supply voltage pins VCC, two ground voltage pins VSS, and six function pins. The six function pins are composed of chip selection pins CS**2** and $\overline{\text{CS1}}$ for selecting a corresponding memory device, an output enable pin $\overline{\text{OE}}$, a write enable pin $\overline{\text{WE}}$, a pin $\overline{\text{LB}}$ for selecting data bits of a lower byte, and a pin $\overline{\text{UB}}$ for selecting data bits of an upper byte.

[**0041**] Referring to **FIG. 8** again, two function pins are provided which compose a second group of pins included only in the NAND-type flash memory device **350**. The pins of the second group are arranged, corresponding to non-connection (N.C) pins of an SRAM device. Thus, the memory devices **350** and **360** are commonly coupled to the address, data, and control buses. That is, a ready/$\overline{\text{busy}}$ pin R/$\overline{\text{B}}$ is arranged, being situated at a **1**H pin (N.C) of the SRAM device **360**. A hardware rest pin $\overline{\text{RESET}}$ is arranged, being situated at a **6**H pin (N.C) of the SRAM device **360**. And, the NAND-type flash memory device **350** further includes address pins A**17** and A**18** that are arranged, being situated at **3**D and **3**E pins of the SRAM device **360**, respectively. Remaining pins out of 48 pins are non-connection (N.C) pins.

[**0042**] The NAND-type flash memory device of this invention applies suitable command signals to input/output pins, carrying out page program, block erase, chip erase, and erase interrupt/refresh operations. For example, if a command signal "80h" (FF hexadecimal) is applied to an input/output pin, the NAND-type flash memory device senses the command and carries out a page program operation, as shown in the following [TABLE 3]. Similarly, command signals "FFh", "60h", and "BOh/DOh" enable the NAND-type flash memory device to carry out reset, block erase, and erase interrupt/refresh operations, respectively. If a command signal is not inputted, a read operation is carried out, as a default mode.

TABLE 3

	Command Set	
Mode of Operation	First Cycle	Second Cycle
Read	Address	
Reset	FFh	
Page Program	80 h	
Block Erase	60 h	DOh
Erase Interrupt/Refresh	BOh/DOh	

[**0043**] With reference to **FIG. 9**A through **FIG. 9**C, read/program/block erase operations of a NAND-type flash memory device having the foregoing common interface mode will be described more fully hereinafter.

[**0044**] As a chip selection signal $\overline{\text{CSI}}$ transitions from high level to low level, a NAND-type flash memory device is selected. Without an input of a command signal, a page address is then applied through address pins Ai, as shown in **FIG. 9A**. At this time, a ready/$\overline{\text{busy}}$ signal R/$\overline{\text{B}}$ transitions from high level to low level for a predetermined time tR that is taken to carry out a read operation of the NAND-type flash memory device. A conventional page buffer circuit senses and latches data from memory cells of a selected row for the reading time. The latched data is synchronized with an output enable signal $\overline{\text{OE}}$, being outputted to the outside (e.g., a memory controller coupled to a data bus) through input/output pins I/Oi.

[**0045**] Referring now to **FIG. 9**B, after a high-to-low transition of a chip selection circuit $\overline{\text{CSI}}$, a dummy address command AAh (provided to prevent an unwanted program operation caused by unspecific data), a serial data input command SOh, a column/row address ADD, and a series of data Din are sequentially inputted. A serial data input command 80h and data Din are inputted through input/output pins I/Oi in a low-to-high transition of a write enable signal $\overline{\text{WE}}$. And, the command AAh and address ADD are inputted through address pins Ai in a high-to-low transition of $\overline{\text{WE}}$. As a ready/$\overline{\text{busy}}$ signal R/$\overline{\text{B}}$ retains low level for a predetermined program time tPROG, a practical program operation is then carried out to memory cells. After the program operation, a signal outputted through an input/output pin I/OO is used as a flag signal that indicates program pass or program fail.

[**0046**] A block erase operation of a NAND-type flash memory device coupled to the same bus as an SRAM is similar to the program operation. Referring to **FIG. 9**C, on the basis of a falling edge of a write enable signal $\overline{\text{WE}}$, a dummy address command AAh (provided to prevent an unwanted program operation caused by unspecific data) and a block address are inputted. And, on the basis of a rising edge of $\overline{\text{WE}}$, a block erase setup command 60h and a command DOh to confirm a block erase operation are inputted. As a ready/$\overline{\text{busy}}$ signal R/$\overline{\text{B}}$ retains low level for a

predetermined erase time tBERS, the block erase operation is then carried out. After the block erase operation, a signal outputted through an input/output pin I/O**0** is used as a flag signal that indicates erase pass or erase fail.

[**0047**] As mentioned so far, memory devices provided to a system have pin arrangements that are identical to each other, being operable in the identical interface mode (e.g., an interface mode of a NAND-type flash memory device or an SRAM device). So all the memory devices are directly coupled to identical buses. As a result, one memory controller is constructed in a microprocessor (or a baseband modem of a communication terminal, a multi-chip that a plurality of devices are established in one chip, etc.), controlling operations of all the memory devices. Having the identical pin arrangement, the memory devices can easily be established in a chip-size package.

[**0048**] In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purpose of limitation, the scope of the invention being set forth in the following claims.

What is claimed is:

1. A semiconductor memory device comprising:

a random access memory chip; and

a package having the random access memory chip,

wherein the package includes a plurality of pins for electrically connecting the random access memory chip to an external device, and

wherein the plural pins provide memory functions commonly to a random access memory device and an electrically erasable and programmable non-volatile semiconductor memory device, each of the pins being arranged at a position of a pin corresponding to the non-volatile semiconductor memory device.

2. The device of claim 1, wherein the electrically erasable and programmable non-volatile semiconductor memory includes a NAND-type flash memory device.

3. The device of claim 2, wherein the random access memory device includes a dynamic random access memory device and a static random access memory device.

4. The device of claim 3, wherein the plural pins are composed of input/output pins for receiving address and data, power supply voltage pins, ground voltage pins, a read enable pin, a chip enable pin, a command latch enable pin, an address latch enable pin, and a write enable pin.

5. The device of claim 4, wherein the non-volatile semiconductor memory comprises:

a memory cell array having EEPROM cells in which rows and columns are arranged;

a first latch circuit for receiving a row address;

a row selection circuit for selecting at least one of the rows in response to a row address outputted from the first latch circuit;

a page buffer circuit for reading data stored in cells corresponding to the selected row, and latching the read-out data;

a second latch circuit for receiving and temporarily storing the latched row address to the first latch circuit;

a comparator for receiving row addresses each latched to the first and second latch circuits, and comparing whether the row addresses are matched with one another; and

a read control logic for controlling an operation of the row selection circuit according to an output signal of the comparator.

6. The device of claim 5 further comprising:

a column selection circuit for selecting a part of the columns in response to a row address; and

output means for outputting the latched data to the page buffer circuit corresponding to the selected columns.

7. The device of claim 6, wherein the read control logic disables the row selection circuit in response to a signal outputted from the comparator when the row addresses are matched with one another, so that the latched data to the page buffer circuit is outputted through the output means without a read operation by the page buffer circuit.

8. The device of claim 5, wherein the first and second latch circuits serve as shift registers.

9. A semiconductor memory device comprising:

an electrically erasable and programmable non-volatile semiconductor memory chip; and

a package having the non-volatile semiconductor memory chip,

wherein the package includes a plurality of pins for electrically connecting the chip to an external device,

wherein the plural chips are composed of a first group of pins and a second group of pins,

wherein the pins of the first group provide memory functions commonly to a static random access memory device and an electrically erasable and programmable non-volatile semiconductor memory device, the pins of the first group each being arranged at a position of a corresponding pin of the static random access memory device, and

wherein the pins of the second group provide functions of unused non-volatile semiconductor memory device to the static random access memory, the pins of the second group each being arranged at a position of an unused pin of the static random access memory.

10. The device of claim 10, wherein the electrically erasable and programmable non-volatile semiconductor memory device includes a NAND-type flash memory device.

11. The device of claim 9, wherein the pins of the first group are composed of address pins, input/output pins, power supply voltage pins, ground voltage pins, a chip selection pin, an output enable pin, and a write enable pin.

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