(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
16 February 2012 (16.02.2012)

PCT

(10) International Publication Number
WO 2012/019850 A1

(51) International Patent Classification:
H04B 10/158 (2006.01)

(21) International Application Number:
PCT/EP2011/061824

(22) International Filing Date:
12 July 2011 (12.07.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10305888.9 13 August 2010 (13.08.2010) EP

(71) Applicant *(for all designated States except US)*: **ALCATEL LUCENT** [FR/FR]; 3 avenue Octave Gréard, F-75007 Paris (FR).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **DUPUY, Jean-yves** [FR/FR]; C/o Alcatel Thales Iii - V Lab, Route de Nozay, F-91460 Marcoussis (FR). **JORGE, Filipe** [FR/FR]; C/o Alcatel Thales Iii - V Lab, Route de Nozay, F-91460 Marcoussis (FR). **KONCZYKOWSKA, Agnieszka** [FR/FR]; C/o Alcatel Thales Iii - V Lab, Route de Nozay, F-91460 Marcoussis (FR).

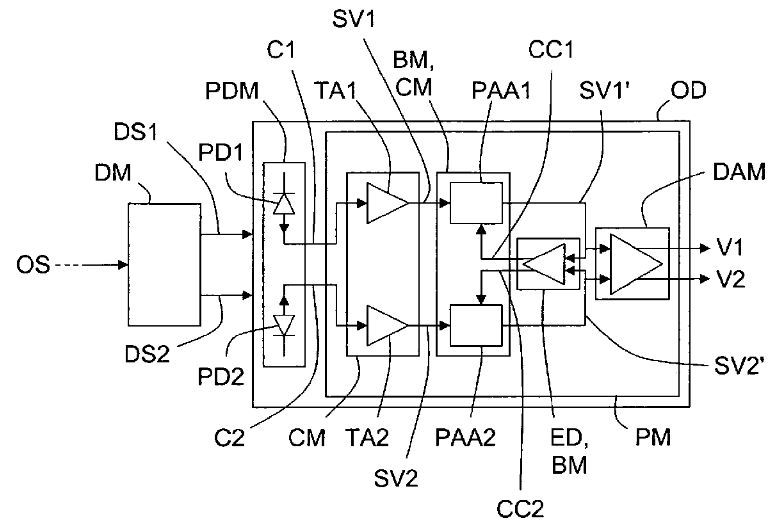
(74) Agent: **SHAMSAEI FAR, Hassan**; Alcatel-lucent International, 32 avenue Kléber, F-92707 Colombes (FR).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) **Title**: OPTOELECTRONIC DEVICE FOR DIFFERENTIAL PHOTORECEPTION, WITH AUTOMATIC COMPENSATION OF PHASE AND AMPLITUDE IMBALANCES



(57) **Abstract**: An optoelectronic device (OD) comprises a photodetection means (PDM) arranged for converting first and second complementary optical signals into first and second complementary currents, and a processing means (PM) arranged for processing these first and second complementary currents to output at least a first output voltage (V1). This processing means (PM) comprises i) a conversion means (CM) arranged for separately converting the first and second complementary currents into first and second operating voltages, ii) a balancing means (BM) arranged for balancing phase and amplitude of the first and second operating voltages, and iii) a differential amplification means (DAM) arranged for applying a subtraction function to the first and second operating voltages with balanced phase and amplitude to produce at least the first output voltage (V1), which is proportional to the difference between the first and second operating voltages with balanced phase and amplitude.

WO 2012/019850 A1

OPTOELECTRONIC DEVICE FOR DIFFERENTIAL PHOTORECEPTION, WITH AUTOMATIC COMPENSATION OF PHASE AND AMPLITUDE IMBALANCES

The present invention relates to optoelectronics, and in particular to optoelectronic devices that offer at least a photoreception function or constitute photoreceivers.

BACKGROUND ART

As it is known by a person skilled in the art, in some technical domains, such as optical communication, differential signaling can be an efficient way of carrying information data with a better immunity to a certain number of parasitic signals. The information data is recovered by realizing a subtraction of two complementary signals, that need to be kept well balanced in phase and amplitude until the subtraction is realized.

In the case of optical communications, these two complementary signals are typically generated by an optical component from one or several input optical signals. Then, an optoelectronic device may be used, which typically comprises a photodetection means arranged for converting the first and second complementary optical signals into first and second complementary currents, and a processing means typically arranged for processing the first and second complementary currents to output a voltage that is proportional to the difference between the first and second complementary currents. Optionally, instead of only one output voltage, two complementary output voltages can be generated, if a differential signaling at the output is further required.

SUMMARY

The above-mentioned optoelectronic devices may be of two types. A first type comprises the so called balanced photoreceivers, whose photodetection means typically comprises a balanced photodetector composed of two photodiodes which are connected in such a way that they output a single-ended current which is proportional to the difference between the two complementary input optical signals, and whose processing means comprises a trans-impedance amplifier, having an input connected to the two photodiodes' common output, and providing a single-ended output voltage, and optionally a complementary output voltage if a differential signaling at the output is further required.

A second type typically comprises the so called differential photoreceivers, whose photodetection means comprises two independent and identical photodiodes, and whose processing means comprises a differential trans-impedance amplifier having first and second inputs connected respectively to the outputs of the photodiodes and providing a single-ended output voltage which is proportional to the difference between the two complementary input currents, and optionally a second complementary output voltage if differential signaling at the output is further required.

However, the components that are combined to produce these optoelectronic devices and the fabrication processes of these components and optoelectronic devices often introduce imperfections causing imbalances between the two complementary signals before they are subtracted, thus degrading the reception performance.

Since typically no imbalance compensation can be realized by these optoelectronic devices, specific and demanding characteristics may be required for the components and fabrication processes involving the components in which differential signaling is used (for instance from the optical demodulator outputs that provide the two complementary optical signals to the photodetection means of the photoreceiver). This may lead to costly components and fabrication processes. Furthermore, whatever the quality of the components and fabrication processes, the optoelectronic devices may have remaining imperfections and possible characteristic shifts during their lifetime, and therefore the ultimate performance benefit that should bring the differential detection may become hard to achieve.

Some embodiments of this invention aim at enabling automatic compensation of amplitude and phase imbalances into optoelectronic devices comprising a photodetection means arranged for converting first and second complementary optical signals into first and second complementary currents, and a processing means arranged for processing the first and second complementary currents to output at least a first output voltage (and optionally a second complementary output voltage if a differential signaling at the output is further required).

For this purpose, the processing means of such optoelectronic devices may comprise:

- a conversion means arranged for separately converting the first and second complementary currents into first and second operating voltages,
- a balancing means arranged for balancing phase and amplitude of the first and second operating voltages, and
- a differential amplification means arranged for applying a subtraction function to the first and second operating voltages with balanced phase and amplitude to produce at least the first output voltage, said ouput voltage being proportional to a difference between the first and second operating voltages with balanced phase and amplitude (and optionally the second complementary output voltage).

The optoelectronic device according to the invention may include additional characteristics considered separately or combined, and notably:

- its conversion means may comprise first and second independent trans-impedance amplification means arranged for converting respectively the first and second complementary currents into the first and second operating voltages;
- its balancing means may comprise i) first and second independent phase and amplitude adjustment means arranged for adjusting respectively the phase and amplitude of the first and second operating voltages as a function of control signals (currents or voltages), and ii) a phase and amplitude error detector arranged for comparing the phases and amplitudes of the first and second operating voltages with balanced phase and amplitude, outputted by the first and second independent phase and amplitude adjustment means, to determine phase and amplitude

imbalances, and for producing the control signals (currents or voltages) representative of phase and amplitude adjustments to be carried out by the first and second independent phase and amplitude adjustment means to compensate for the determined phase and amplitude imbalances;

- ➢ each of the first and second independent phase and amplitude adjustment means may comprise a variable delay means arranged for adjusting the phase, and a variable gain means arranged for adjusting the amplitude;
- ➢ the phase and amplitude error detector may comprise a phase comparator comprising an XOR means arranged for applying an XOR logical function to the first and second operating voltages with balanced phase and amplitude, and an amplitude comparator comprising a peak detector and a differential amplifier arranged for comparing the amplitudes of the first and second operating voltages with balanced phase and amplitude;

- its photodetection means may comprise first and second independent photodiodes arranged for converting respectively the first and second complementary optical signals into the first and second complementary currents;
- it may constitute a differential photoreceiver.

BRIEF DESCRIPTION OF THE DRAWING

Other features and advantages of the invention will become apparent on examining the detailed specifications hereafter and the appended drawing, wherein the unique figure schematically and functionally illustrates an optical demodulator connected to an example of embodiment of an optoelectronic device according to embodiments of the invention.

The appended drawing may serve not only to complete the invention, but also to contribute to its definition, if need be.

DETAILED DESCRIPTION

Embodiments of the invention aim at providing an optoelectronic device OD capable of automatically compensating for amplitude and phase imbalances.

In the following description, it will be considered, as example, that the optoelectronic device OD is a differential photoreceiver. But, the optoelectronic device OD could be also a device offering several functions and notably photoreception.

As illustrated in the unique figure, an optoelectronic device OD, according to the invention, comprises at least a photodetection means PDM and a processing means PM.

The photodetection means PDM comprises first and second inputs which may be connected respectively to first and second outputs of an optical demodulator DM. The optical demodulator DM is arranged for demodulating each input optical signal it receives on its input to produce first DS1 and second DS2 optical complementary signals that it outputs onto its first and second outputs.

The photodetection means PDM may be arranged for converting the first DS1 and second DS2 complementary optical signals (respectively received on its first and second inputs) into first C1 and second C2 complementary currents.

For instance, and as illustrated in the unique figure, the photodetection means PDM may comprise first PD1 and second PD2 independent and (preferably) identical photodiodes PD1 and PD2. Herein, the term "independent" is to be understood to refer to the fact that the two photodiodes PD1 and PD2 are not coupled together.

These first PD1 and second PD2 photodiodes are arranged for converting respectively the first SD1 and second SD2 complementary optical signals into the first C1 and second C2 complementary currents.

The photodetection means PDM may further comprise further typical ancillary components, such as biasing and decoupling networks, which themselves may comprise capacitors and resistors.

The processing means PM may be an electronic circuit or an integrated component. It is arranged for processing the first C1 and second C2 complementary currents (outputted by the photodetection means PDM) to output at least a first output voltage V1, and optionally a second complementary output voltage V2 if a differential signaling at the output is further required.

For instance, the second output voltage V2, complementary to the first output voltage V1, is equal to the opposite of this first output voltage V1 (i.e. V2 = - V1).

More precisely, according to some embodiments of the invention and as illustrated in the unique figure, the processing means PM may comprise a conversion means CM, a balancing means BM and a differential amplification means DAM.

The conversion means CM may comprises first and second inputs that are respectively connected to the outputs of the photodetection means PDM to be fed respectively with the first C1 and second C2 complementary currents. It is arranged for separately converting the received first C1 and second C2 complementary currents into first SV1 and second SV2 operating voltages that it outputs respectively on first and second outputs. Herein, the terms "operating voltage" are to be understood to refer to voltage having values comprised into an interval which is adapted for a normal operation of the means that receive such voltage at respective input(s) thereof.

For instance, and as illustrated in the unique figure, the conversion means CM may comprise first TA1 and second TA2 independent and preferably identical trans-impedance amplification means which are arranged for converting respectively the first C1 and second C2 complementary currents into the first SV1 and second SV2 operating voltages. For instance, each trans-impedance amplification means TA1, TA2 is a single-ended trans-impedance amplifier.

The conversion means CM may comprise additional processing means downstream the two trans-impedance amplification means TA1 and TA2 to further optimize the signals, and notably a balancing means BM.

This balancing means BM comprises first and second inputs that are respectively connected to the first and second outputs of the conversion means CM to be fed respectively with the first SV1 and second SV2 operating voltages. It is arranged for balancing the phase and amplitude of these first

SV1 and second SV2 operating voltages.

For instance, and as illustrated in the unique figure, the balancing means BM may comprise first PAA1 and second PAA2 independent and preferably identical phase and amplitude adjustment means and a phase and amplitude error detector ED.

The first phase and amplitude adjustment means PAA1 has a first input connected to the first output of the conversion means CM to be fed with the first operating voltage SV1, and a second input connected to a first output of the phase and amplitude error detector ED to be fed with a first control signal (current or voltage) CC1. The second phase and amplitude adjustment means PAA2 has a first input connected to the second output of the conversion means CM to be fed with the second operating voltage SV2, and a second input connected to a second output of the phase and amplitude error detector ED to be fed with a second control signal (current or voltage) CC2.

These first PAA1 and second PAA2 phase and amplitude adjustment means are arranged for adjusting respectively the phase and amplitude of the first SV1 and second SV2 operating voltages as a function of the first CC1 and second CC2 control signals (currents or voltages) and comprise respectively outputs to output first SV1' and second SV2' operating voltages with adjusted phase and amplitude.

For instance, each of the first PAA1 and second PAA2 phase and amplitude adjustment means may comprise a variable delay means, which is arranged for adjusting the phase of the first SV1 or second SV2 operating voltage, and a variable gain means, which is arranged for adjusting the amplitude of the first SV1 or second SV2 operating voltage.

Herein the terms "variable delay means" are to be understood to refer to an electronic component that is capable of modifying the delay it introduces onto a signal as a function of a control signal (current or voltage). Such a variable delay means can be implemented by means of a so-called “selector” in charge of selecting among several delayed versions of the input signal depending on a control signal (current or voltage), for instance. Moreover, herein the terms "variable gain means" are to be understood to refer to an electronic component that is capable of modifying its gain as a function of a control signal (current or voltage). Such a variable gain means can be implemented by means of the well known Gilbert cell, for instance.

The phase and amplitude error detector ED comprises first and second inputs, connected respectively to the outputs of the first PAA1 and second PAA2 phase and amplitude adjustment means, and first and second outputs, connected respectively to the second inputs of the first PAA1 and second PAA2 phase and amplitude adjustment means. The phase and amplitude error detector ED is notably arranged for comparing the phases and amplitudes of the first SV1' and second SV2' operating voltages with balanced phase and amplitude, that are outputted respectively by the first and second outputs of the first PAA1 and second PAA2 phase and amplitude adjustment means, in order to determine possible phase and amplitude imbalances therebetween. The phase and amplitude error detector ED is also arranged for producing the first CC1 and second CC2 control signals (currents or voltages) that are intended respectively to control the operation of the first PAA1 and second PAA2 phase and amplitude adjustment means and which are representative of phase and amplitude adjustments to be carried out by these first PAA1 and second PAA2 phase and amplitude adjustment means to compensate for the determined phase and amplitude imbalances between the first SV1' and second SV2' operating voltages with balanced phase and amplitude they respectively output.

For instance, the phase and amplitude error detector ED may comprise a phase comparator and an amplitude comparator. Said phase comparator may comprise an XOR (exclusive OR) means arranged for applying an XOR logical function to the first SV1' and second SV2' operating voltages with balanced phase and amplitude. Herein the terms "XOR means" are to be understood to refer to an electronic component capable of outputting a signal representative of the result of a XOR logical function applied on two input signals. The phase comparator may further comprise some low pass filter(s) with some usual processing means after the XOR means in order to finally generate a suitable signal (voltage or current), that is proportional or at least representative in some way of the phase difference between the first SV1' and second SV2' operating voltages.

The amplitude comparator may comprise a peak detector and a differential amplifier arranged for comparing the respective amplitudes of the first SV1' and second SV2' operating voltages with balanced phase and amplitude. The amplitude comparator may comprise capacitor(s) and diode(s), to create a signal which is proportional or at least representative in some way of the amplitude of each first SV1' and second SV2' operating voltages, a differential amplifier for comparing said first SV1' and second SV2' operating voltages, and possibly further known processing means to generate a suitable amplitude error signal.

So, the balancing means BM acts as an automatic feedback loop capable of compensating for amplitude and phase imbalances between the first SV1 and second SV2 operating voltages.

The differential amplification means DAM comprises first and second inputs that are respectively connected to the first and second outputs of the balancing means BM (i.e. the ones of the first PAA1 and second PAA2 phase and amplitude adjustment means) to be fed respectively with the first SV1' and second SV2' operating voltages with balanced phase and amplitude.

This differential amplification means DAM is arranged for applying a subtraction function to the first SV1' and second SV2' operating voltages with balanced phase and amplitude in order to produce the first output voltage V1 that is proportional to the difference between the first SV1' and second SV2' operating voltages with balanced phase and amplitude, and optionally a second complementary output voltage V2 if a differential signaling at the output is further required.

The invention offers several advantages amongst which the following are in particular worth mentioning:

- simplification and cost reduction of differential detection,
- a powerful solution to efficiently implement differential detection without requiring a balanced photodetector,
- an improvement of the components and fabrication tolerances and therefore a cost reduction.

The invention is not limited to the embodiments of optoelectronic device described above, only as examples, but it encompasses all alternative embodiments which may be considered by one skilled in the art within the scope of the claims hereafter.

CLAIMS

1. Optoelectronic device (OD) comprising a photodetection means (PDM) arranged for converting first and second complementary optical signals into first and second complementary currents, and a processing means (PM) arranged for processing said first and second complementary currents to output at least a first output voltage (V1), wherein said processing means (PM) comprises i) a conversion means (CM) arranged for separately converting said first and second complementary currents into first and second operating voltages, ii) a balancing means (BM) arranged for balancing phase and amplitude of said first and second operating voltages, and iii) a differential amplification means (DAM) arranged for applying a subtraction function to said first and second operating voltages with balanced phase and amplitude to produce at least said first output voltage (V1), which is proportional to the difference between said first and second operating voltages with balanced phase and amplitude.

2. Optoelectronic device according to claim 1, wherein said conversion means (CM) comprises first (TA1) and second (TA2) independent trans-impedance amplification means arranged for converting respectively said first and second complementary currents into said first and second complementary operating voltages.

3. Optoelectronic device according to any one of claims 1 and 2, wherein said balancing means (BM) comprises i) first (PAA1) and second (PAA2) independent phase and amplitude adjustment means arranged for adjusting respectively the phase and amplitude of said first and second operating voltages as a function of control signals, and ii) a phase and amplitude error detector (ED) arranged for comparing the phases and amplitudes of said first and second operating voltages with balanced phase and amplitude, outputted by said first (PAA1) and second (PAA2) independent phase and amplitude adjustment means, to determine phase and amplitude imbalances, and for producing said control signals representative of phase and amplitude adjustments to be carried out by said first (PAA1) and second (PAA2) independent phase and amplitude adjustment means to compensate

for said determined phase and amplitude imbalances.

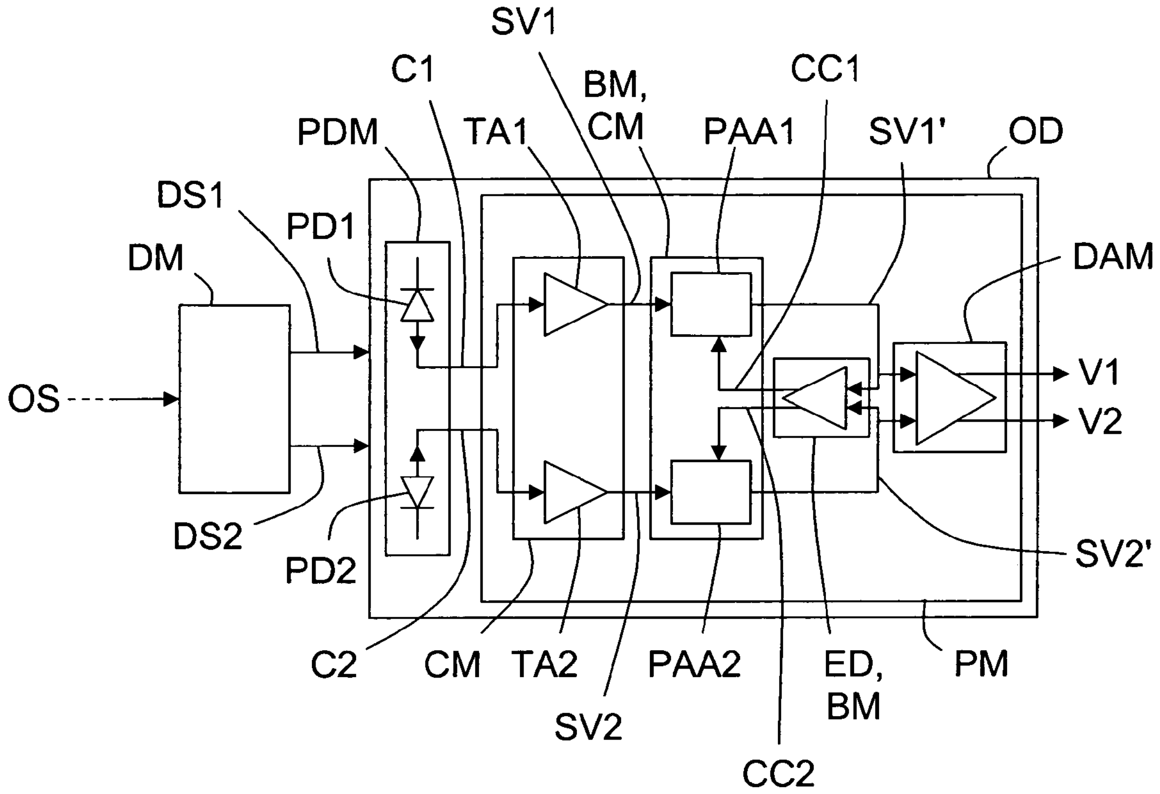
4. Optoelectronic device according to claim 3, wherein each of said first (PAA1) and second (PAA2) independent phase and amplitude adjustment means comprises a variable delay means arranged for adjusting said phase, and a variable gain means arranged for adjusting said amplitude.

5. Optoelectronic device according to one of claims 3 and 4, wherein said phase and amplitude error detector (ED) comprises a phase comparator comprising an XOR means arranged for applying an XOR logical function to said first and second operating voltages with balanced phase and amplitude, and an amplitude comparator comprising a peak detector and a differential amplifier arranged for comparing the amplitudes of said first and second operating voltages with balanced phase and amplitude.

6. Optoelectronic device according to any one of claims 1 to 5, wherein said photodetection means (PDM) comprises first (PD1) and second (PD2) independent photodiodes (PD1, PD2) arranged for converting respectively said first and second complementary optical signals into said first and second currents.

7. Optoelectronic device according to any one of claims 1 to 6, wherein said differential amplification means (DAM) is arranged for outputting a second output voltage (V2) which is complementary of said first output voltage (V1).

8. Optoelectronic device according to any one of claims 1 to 7, wherein it constitutes a differential photoreceiver.



Unique Figure

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2011/061824

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04B10/158
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007/047971 A1 (IKEUCHI TADASHI [JP]) 1 March 2007 (2007-03-01) figures 1,5 paragraph [0008] paragraphs [0037] - [0041] -----	1-8
A	US 2007/212081 A1 (TAKAHASHI HIDEYUKI [JP] ET AL) 13 September 2007 (2007-09-13) figure 1 paragraphs [0038] - [0040] -----	1-8
A	US 6 760 552 B1 (TAJIMA AKIO [JP] ET AL) 6 July 2004 (2004-07-06) figure 1 column 3, line 56 - column 4, line 20 -----	1-8
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 September 2011	27/09/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Petitit, Nicolas

2

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	A. UMBACH ET AL: "Integrated differential photoreceiver for 40 Gbit/s systems", CONFERENCE PROCEEDINGS. 2000 INTERNATIONAL CONFERENCE ON INDIUM PHOSPHIDE AND RELATED MATERIALS (CAT. NO.00CH37107), 1 January 2000 (2000-01-01), pages 321-324, XP55007510, DOI: 10.1109/ICIPRM.2000.850297 ISBN: 978-0-78-036320-5 the whole document -----	1-8

2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2011/061824

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007047971 A1	01-03-2007	JP 4440855 B2 JP 2007060442 A	24-03-2010 08-03-2007
US 2007212081 A1	13-09-2007	JP 2007243510 A	20-09-2007
US 6760552 B1	06-07-2004	EP 1041750 A2 JP 3655770 B2 JP 2000278222 A	04-10-2000 02-06-2005 06-10-2000