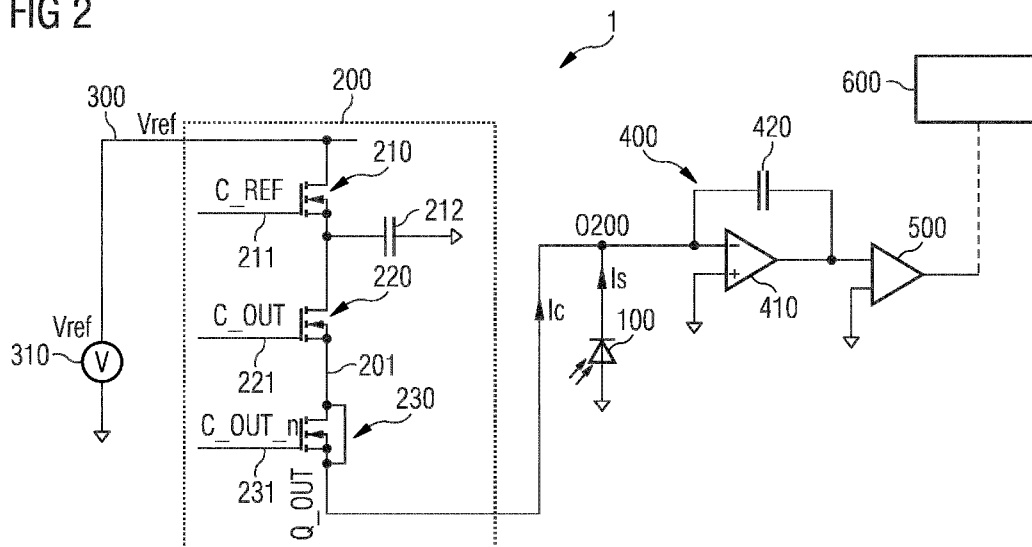




- |                                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p><b>(51) International Patent Classification:</b><br/>H03K 17/16 (2006.01) H03K 17/94 (2006.01)</p>         | <p><b>(74) Agent:</b> EPPING HERMANN FISCHER PATENTANWALTSGESELLSCHAFT MBH; Schloßschmidstr. 5, 80639 München (DE).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <p><b>(21) International Application Number:</b><br/>PCT/EP2018/081039</p>                                    | <p><b>(81) Designated States</b> (<i>unless otherwise indicated, for every kind of national protection available</i>): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.</p> |
| <p><b>(22) International Filing Date:</b><br/>13 November 2018 (13.11.2018)</p>                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <p><b>(25) Filing Language:</b> English</p>                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <p><b>(26) Publication Language:</b> English</p>                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <p><b>(30) Priority Data:</b><br/>17201931.7 15 November 2017 (15.11.2017) EP</p>                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <p><b>(71) Applicant:</b> AMS AG [AT/AT]; Schloss Premstätten, Tobelbader Str. 30, 8141 Premstätten (AT).</p> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <p><b>(72) Inventor:</b> LENHARD, Herbert; Peterstalstr. 5, 8042 Graz (AT).</p>                               | <p><b>(84) Designated States</b> (<i>unless otherwise indicated, for every kind of regional protection available</i>): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,</p>                                                                                                                                                                                                                                                                                                                                                                               |

**(54) Title:** SENSOR ARRANGEMENT TO SENSE AN EXTERNAL SIGNAL

FIG 2



**(57) Abstract:** A sensor arrangement to sense an external signal comprises a sensor (100) and a charge generator (200) to generate a compensation current ( $I_c$ ) to compensate the sensor current. A charge generator (200) comprises a first transistor (210) having a parasitic capacitor (212) and a first conductive path. The charge generator (200) comprises a second transistor (220) having a second conductive path being coupled in series to the first transistor (210) and coupled to the output node (O200) of the charge generator (200). The control circuit (600) is configured to control the conductivity of the respective first and second conductive path of the first and the second transistor (210, 220) of the charge generator (200) so that the sensor current is compensated by the compensation current ( $I_c$ ).

TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

**Published:**

- *with international search report (Art. 21(3))*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

## Description

### SENSOR ARRANGEMENT TO SENSE AN EXTERNAL SIGNAL

#### 5 Technical Field

The disclosure relates to a sensor arrangement to sense an external signal, wherein a charge is provided for a sensor interface to a sensor.

10

#### Background

A sensor arrangement may comprise a charge generator to generate a compensation charge/compensation current in a sensor interface. The charge generator generates the compensation charge/compensation current for example to compensate a sensor charge generated by a sensor, for example a photodiode, in a charge balance circuit topology. The charge generator can be designed with an SC (switched capacitor) circuit. The SC circuit may comprise a controllable switch to couple a capacitor to a reference voltage to load the capacitor in a first operation cycle and to discharge the capacitor in a second operation cycle. The compensation charge/compensation current is provided by discharging the capacitor. The capacitor is configured as a charge storage element to store the compensation charge.

A well-known problem in a conventional SC topology of the charge generator is the lower limit of the compensation charge generated owed to charge injection by switches coupling directly to charge storage elements. Each time a switching state of a controllable switch of the charge generator is changed, a disturbing charge is generated. The

disturbing charges may change the desired compensation charge which is necessary to compensate the sensor charge. The lower the compensation charge, the stronger the unwanted influence of the disturbing charge portions of switching elements of the charge generator in a sensor interface.

There is a desire to provide a sensor arrangement to sense an external signal, which allows to reduce the unwanted influence of disturbing charges caused by switching elements to a compensation charge to compensate a sensor charge of a sensor of the sensor arrangement.

#### Summary

A sensor arrangement to sense an external signal is specified in claim 1.

According to an embodiment, the sensor arrangement to sense an external signal comprises a sensor to provide a sensor charge/sensor current in dependence from the external signal. The sensor arrangement further comprises a charge generator to generate a compensation charge/compensation current to compensate the sensor charge/sensor current. The sensor arrangement further comprises an output node of the charge generator to provide the compensation charge/compensation current. The sensor is coupled to the output node of the charge generator to provide the sensor charge/sensor current of the sensor at the output node of the charge generator.

The sensor arrangement comprises a reference voltage line to provide a reference voltage. The sensor arrangement further comprises a control circuit to control the generation of the compensation charge/compensation current. The charge

generator comprises a first transistor having a parasitic capacitor and a first conductive path. The first transistor is connected to the reference voltage line. The charge generator comprises a second transistor having a second  
5 conductive path being coupled in series to the first transistor and coupled to the output node of the charge generator. The control circuit is configured to control the conductivity of the respective conductive path of the first and the second transistor of the charge generator so that the  
10 sensor charge/sensor current is compensated by the compensation charge/compensation current. "Compensation" means that the sensor current is equal or almost equal to the compensation current.

15 In order to circumvent the limitation regarding the lower limit of the compensation charge, the charge generator of the sensor arrangement uses the charge injection caused by the switching operation of the transistors of the charge generator itself to generate the compensation charge. In  
20 particular, the parasitic capacitor of the first transistor of the charge generator is used as a storage element to store a respective compensation charge portion during subsequent switching cycles of the first and the second transistor.

25 This means that the charge generator of the sensor arrangement does not use a device/capacitor provided especially for charge storing purposes. The sensor arrangement rather uses the parasitic capacitor of the first transistor to store a packet of charge that is to be  
30 transferred to the output node of the charge generator.

The first and the second transistor of the charge generator are alternately switched between a conductive and non-

conductive state. During a first operation state of the charge generator, the first transistor is operated in a conductive state so that the reference voltage line is conductively connected to the parasitic capacitor, and the parasitic capacitor is charged by the reference voltage. The second transistor is operated in the non-conductive state during the first operation state of the charge generator. During a subsequent second operation state of the charge generator, the first transistor is operated in the non-conductive state and the second transistor is operated in the conductive state so that the charge packet stored at the parasitic capacitor is discharged and transferred to the output node.

The switching of the second transistor between the conductive and non-conductive state causes the generation of a disturbing charge that influences the desired compensation charge/compensation current. In order to compensate the disturbing charge caused by the switching operations of the second transistor, the charge generator may comprise a compensation component. The compensation component is used to compensate a charge component generated by a parasitic capacitance of the second transistor. In particular, the compensation component is configured to compensate the AC-charge component generated by the gate-source capacitance of the second transistor of the charge generator. The compensation component may be configured as a transistor with drain and source terminals connected to each other so that a capacitor is realized.

The electrical properties of the first and second transistor and/or the compensation component of the charge generator depend on external parameters, for example the temperature or

manufacturing tolerances. In order to compensate temperature effects and process variations an additional reference loop/controllable reference voltage generator can be provided. The controllable reference voltage generator is  
5 configured to generate the reference voltage on the reference voltage line to control the amount of injected charge at the output node of the charge generator.

The controllable reference voltage generator comprises a  
10 charge monitor circuit to provide a monitor current to an output node of the charge monitor circuit. The controllable reference voltage generator further comprises a constant current source, for example a bandgap reference, which applies a reference current to the output node of the charge  
15 monitor circuit. The constant current source generates the reference current as a constant current.

The controllable reference voltage generator/reference loop further comprises a loop controller being arranged between  
20 the output node of the charge monitor circuit and the reference voltage line. The loop controller changes the reference voltage on the reference voltage line in dependence on a comparison of the monitor charge/monitor current of the charge monitor circuit and the reference current of the  
25 constant current source.

The controllable reference voltage generator is configured to adjust the reference voltage at the reference voltage line so that the monitor current equals the reference current at the  
30 output node of the charge monitor circuit. As a consequence of this, the compensation charge/compensation current generated by the charge generator will also be well-defined by the reference current of the constant current source. In

conclusion, the charge injected from the parasitic capacitor of the first transistor of the charge generator in dependence on the charging state of the parasitic capacitor is used as a compensation charge to compensate the sensor charge/sensor  
5 current, but in a well-controlled manner by using the reference loop/controllable reference voltage generator.

The charge generator of the sensor arrangement provides a compensation charge generation by using controllable  
10 switches/transistors only. The amount of the compensation charge/compensation current is defined by a reference loop/controllable reference voltage generator. In particular, the reference loop/controllable reference voltage generator stabilizes the compensation charge/compensation current  
15 against temperature drift, process variations and supply changes. The proposed sensor arrangement with compensation charge generation may be used for sensor interfaces to optical as well as non-optical sensors, in particular to those sensors which generate an output signal configured as  
20 an output current.

Additional features and advantages are set forth in the detailed description that follows, and in part will be readily apparent to those skilled in the art from the  
25 description or recognized by practicing the embodiments as described in the written description and claims hereof, as well as the appended drawings. It is to be understood that both the foregoing general description and the following detailed description are merely exemplary, and are intended  
30 to provide an overview or framework to understand the nature and character of the claims.

## Brief description of the drawings

Figure 1 shows a conventional topology of a sensor arrangement comprising a charge generator to generate a compensation charge/compensation current to compensate a sensor charge/sensor current;

Figure 2 shows an embodiment of sensor arrangement comprising a charge generator to generate a compensation charge/compensation current to compensate a sensor charge/sensor current of a sensor of the sensor arrangement by using charge storage elements being configured as a parasitic capacitor of a transistor of a charge generator;

Figure 3 shows an embodiment of a sensor arrangement comprising a reference loop/controllable reference voltage generator to generate a reference voltage on a reference voltage line of the sensor arrangement and a charge generator; and

Figure 4 illustrates control signals to control transistors of the charge generator of the sensor arrangement.

## Detailed Description

Embodiments of a sensor arrangement to sense an external signal with a compensation charge generation for the sensor interface and its components are now be described more fully hereinafter with reference to the accompanying drawings. The embodiments of the sensor arrangement and its components may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein;

rather, these embodiments are provided so that the disclosure will fully convey the scope of the embodiments of the sensor arrangement and its components to those skilled in the art. The drawing are configured to clearly illustrate the  
5 different embodiments of the sensor arrangement and its components.

Figure 1 shows a conventional embodiment of a sensor arrangement 3 to sense an external signal, for example a  
10 light signal. The light signal impacts on a sensor 10, for example a photodiode. A sensor charge/sensor current  $I_s$  is generated by the sensor 10 in dependence from the intensity of the impacting light.

15 The sensor arrangement 3 further comprises a charge generator 20 being configured to generate a compensation charge/compensation current  $I_c$  at an output node O20 of the charge generator 20. The conventional sensor arrangement 3 comprises a reference voltage source 31 to provide a  
20 reference voltage  $V_{ref}$  on a reference voltage line 30.

The charge generator 20 comprises a controllable switch 21 and a capacitor 22. The capacitor 22 is charged during a first operation state of the controllable switch 21 which is  
25 illustrated in Figure 1. The capacitor 22 is conductively connected to the reference voltage  $V_{ref}$  during the first operation state. The capacitor 22 is charged by the reference voltage  $V_{ref}$ . After having charged the capacitor 22, the switching state of the controllable switch 21 is changed so  
30 that the capacitor 22 is connected to the output node O20 of the charge generator 20.

The switching state of the controllable switch 21 is alternately changed so that the capacitor 22 is charged and discharged, and a compensation charge/compensation current  $I_c$  is generated by the charge generator 20 at the output node 5 020 of the charge generator 20. The purpose of the charge generator 20 is to provide the compensation charge/compensation current  $I_c$  at the output node 020 of the charge generator 20 such that the sensor charge/sensor current  $I_s$  is compensated.

10

The output node 020 of the charge generator 20 is connected to an integrator 40. The switching sequence to switch the controllable switch 21 between the first operation state in which the capacitor 22 is coupled to the reference voltage 15  $V_{ref}$ , and a second state in which the capacitor 22 is coupled to the output node 020, is controlled such that an output signal of the integrator circuit 40 is kept at a zero level. In this case the compensation charge/compensation current  $I_c$  would compensate the sensor charge/sensor current  $I_s$  of the 20 sensor 10. The number of changes of the switching state of the controllable switch 21 is a measure for the intensity of the incident light.

According to the conventional topology for the charge 25 generator 20 shown in Figure 1, an SC (Switched Capacitor) implementation for the charge generator is most widely used in combination with a reference voltage. However, due to the permanently occurring switching cycles of the controllable switch 21, disturbing charges are generated and injected to 30 the output node 020 in addition to the desired compensation charge stored at the capacitor 22. The disturbing charges are stored in parasitic capacitors of the controllable switch 21. The controllable switch 21 may be realized by transistors so

that the parasitic capacitors of the transistors are charged/discharged during the switching cycles and distort the desired compensation charge at the output node O20. The disturbing charges are indeed relevant when a weak light intensity impacts the photodiode 10 and the sensor current  $I_s$  is small and the desired compensation charge stored at the capacitor 22 is small as well.

Figure 2 shows an embodiment of a sensor arrangement 1 to sense an external signal, wherein the sensor arrangement comprises an improved charge generator 200 in comparison to the charge generator 20 shown in Figure 1. In particular, the improved charge generator omits the generation of disturbing charges during subsequent switching cycles of the transistors of the charge generator.

The sensor arrangement 1 comprises a sensor 100 to provide a sensor charge/sensor current  $I_s$  in dependence on an external signal which is captured by the sensor. According to the exemplified embodiment shown in Figure 2, the sensor 100 is configured as a photodiode to generate the sensor charge/sensor current  $I_s$  in dependence from external light impacting the photodiode 100.

The sensor arrangement 1 further comprises the charge generator 200 to generate a compensation charge/compensation current  $I_c$  at an output node O200 of the charge generator 200 to compensate the sensor charge/sensor current  $I_s$  of the sensor. The sensor 100 is coupled to the output node O200 of the charge generator 200. The sensor arrangement 1 further comprises a reference voltage line 300 to provide a reference voltage  $V_{ref}$  which is used by the charge generator 200 to generate the compensation charge/compensation current  $I_c$ .

The output node O200 of the charge generator 200 is connected to an integrator circuit 400. An output side of the integrator circuit 400 is connected to a comparator 500. The  
5 integrator circuit 400 generates an output signal at its output side in dependence on the charge/current applied by the sensor 100 at the output node O200 and the compensation charge/compensation current  $I_c$  generated at the output node O200 by the charge generator 200. The comparator 500  
10 generates an evaluation signal at its output side in dependence from the output signal of the integrator circuit 400. The evaluation signal of the comparator 500 is evaluated by a control circuit 600 to control the generation of the compensation charge/compensation current  $I_c$ .

15 The charge generator 200 comprises at least a current branch 201. The first current branch 201 comprises a first transistor 210 having a parasitic capacitor 212 and a first conductive path. The first transistor 210 of the charge  
20 generator 200 is connected to the reference voltage line 300. The charge generator 200 further comprises a second transistor 220 being arranged in the current branch 201 having a second conductive path being coupled in series to the first transistor 210 and coupled to the output node O200  
25 of the charge generator 200. The parasitic capacitor 212 is shown in Figure 2 with the first side being coupled between a source node of the first transistor 210 and a drain node of the second transistor 220, and having a second side being coupled to a reference potential.

30 The first and the second transistor 210, 220 of the charge generator 200 are controlled by the control circuit 600 to be operated in a conductive and non-conductive state. The

conductivity of the first transistor 210 is controlled by the control signal C\_REF applied at a control terminal 211 of the first transistor 210. The conductivity of the second transistor 220 is controlled by a control signal C\_OUT applied at a control terminal 221 of the second transistor 220. The control signals C\_REF and C\_OUT are generated by the control circuit 600.

The charge generator 200 is operated in a first and a second operation state. The control circuit 600 is configured to control the first transistor 210 of the charge generator 200 in a conductive state and to control the second transistor 220 of the charge generator 200 in a non-conductive state to load the parasitic capacitor 212 by conductively coupling the parasitic capacitor 212 to the reference voltage line 300 during the first operation state. The control circuit 600 is further configured to control the first transistor 210 of the charge generator 200 in a non-conductive state and to control the second transistor 220 of the charge generator 200 in a conductive state to provide the compensation charge/compensation current  $I_c$  at the output node O200 of the charge generator 200 during the second operation state.

The control circuit 600 is configured to control the conductivity of the respective first and second conductive path of the first and second transistor 210, 220 of the charge generator 200 so that the sensor charge/sensor current  $I_s$  is compensated by the compensation charge/compensation current  $I_c$ . The compensation current  $I_c$  is generated by subsequent packets of the compensation charge that are transferred to the output node O200 of the charge generator by alternately charging and discharging the parasitic

capacitor 212 during the switching cycles of the first and the second transistor 210 and 220.

The charge generator 200 in its basic concept shown in Figure 2 is built up by the two transistors 210 and 220. The combination of the controllable switches 210 and 220 with the reference voltage  $V_{ref}$  and the parasitic capacitor 212 may be considered as a capacitive DC-DC converter or charge-pump.

When the second transistor 220 is switched from the non-conductive state during the first operation state into the conductive state during the second operation state, a disturbing charge is injected in the output node O200 of the charge generator. The disturbing charge is an AC-charge component generated by the gate-source capacitance of the second transistor 220.

In order to compensate this disturbing charge, the charge generator 200 may comprise a compensation component 230. The compensation component 230 is arranged in the current branch 201 between the second transistor 220 and the output node O200 of the charge generator 200. The compensation component 230 is configured to compensate the AC-charge component generated by the gate-source capacitance of the second transistor 220 of the charge generator 200.

In particular, the compensation component 230 may be configured as a transistor having a drain and source node which are connected to each other. Since the source and the drain terminal of the transistor 230 are connected to each other, the transistor 230 just has the function of a capacitor which is effective against the capacitor of the second transistor 220. The transistor 230 has a control

terminal 231 to apply a control signal C\_OUT\_n being generated by the control circuit 600. The transistor 230 may be used as a matching unit to compensate the AC-charge component generated by the gate-source capacitance of the second transistor 220.

The control circuit 600 generates the control signals C\_REF, C\_OUT as well as C\_OUT\_n so that the charge generator 200 generates the compensation charge/compensation current  $I_c$  at the output node O200 of the charge generator 200 so that the output signal of the integrator circuit 400 has a zero level. In this case, the charge generator 200 generates the compensation charge/compensation current  $I_c$  exactly with a level to compensate the sensor charge/sensor current  $I_s$ . When compared to the conventional charge generator 20 shown in Figure 1, the combination of the controllable switch 21 and the capacitor 22 which is configured as a concrete device according to the standard topology of Figure 2, is replaced by the string of transistors 210, 220 and 230. The function of the capacitor 22 is resumed by the parasitic capacitor 212 of the first transistor 210.

The electrical properties of the transistors 210, 220 and 230 depend on temperature effects and process variations. Figure 3 shows an improved embodiment of the sensor arrangement 2 shown in Figure 2. According to the embodiment of the sensor arrangement 3 of Figure 3, temperature effects and process variations are compensated by the utilization of a controllable reference voltage generator/reference loop/control loop 1000 in order to control the amount of injected charge provided by the charge generator 200. In particular, the controllable reference voltage generator 1000

is configured to generate/adjust the reference voltage  $V_{ref}$  on the reference voltage line 300.

The controllable reference voltage generator 1000 comprises a  
5 charge monitor circuit 700 having at least a current branch  
701 and an output node O700. The current branch 701 is  
coupled between the reference voltage line 300 and the output  
node O700 of the charge monitor circuit 700. The charge  
monitor circuit 700 is configured to provide a monitor  
10 current  $I_m$  to the output node O700 of the charge monitor  
circuit 700.

The controllable reference voltage generator 1000 comprises a  
constant current source 800 to generate a reference current  
15  $I_{ref}$ . The constant current source may be configured as a  
bandgap reference.

According to the embodiment of the sensor arrangement 3 shown  
in Figure 3, the charge monitor circuit 700 comprises a first  
20 transistor 710 and a second transistor 720 being arranged in  
the current branch 701. The first transistor 710 of the  
charge monitor circuit 700 has a parasitic capacitor 712 and  
a first conductive path. The first transistor 710 of the  
charge monitor circuit 700 is connected to the reference  
25 voltage line 300. The second transistor 720 of the charge  
monitor circuit 700 has a second conductive path being  
coupled in series to the first transistor 710 of the charge  
monitor circuit 700 and coupled to the output node O700 of  
the charge monitor circuit 700.

30

The first and the second transistor 710 and 720 of the charge  
monitor circuit 700 are controlled by the control circuit 600  
to be operated in a conductive and non-conductive state. The

first transistor 710 has a control terminal 711 to apply a control signal CM\_REF being generated by the control circuit 600. The second transistor 720 comprises a control terminal 721 to apply a control signal CM\_OUT generated by the control  
5 circuit 600.

The charge monitor circuit 700 is operated in a first and a second operation state. The control circuit 600 is configured to control the first transistor 710 of the charge monitor  
10 circuit 700 in a conductive state and to control the second transistor 720 of the charge monitor circuit 700 in a non-conductive state to load the parasitic capacitor 712 by conductively coupling the parasitic capacitor 712 to the reference voltage line 300 during the first operation state  
15 of the charge monitor circuit. The control circuit 600 is further configured to control the first transistor 710 of the charge monitor circuit 700 in a non-conductive state and to control the second transistor 720 of the charge monitor circuit 700 in a conductive state to provide the monitor  
20 current  $I_m$  at the output node O700 of the charge monitor circuit 700 during the second operation state of the charge monitor circuit 700.

The parasitic capacitor 712 of the first transistor 710 is  
25 charged by the reference voltage  $V_{ref}$  during the first operation state and discharged to the output node O700 during the second operation state. The monitor current  $I_m$  is generated by subsequent packets of the charge stored on the parasitic capacitor 712 during the first operation state of  
30 the charge monitor circuit and discharged during the second operation state of the charge monitor circuit.

When changing its switching state between the conductive and non-conductive state, the second transistor 720 generates a disturbing charge at the output node O700 which influences the monitor current  $I_m$ . The disturbing charge is an AC charge component generated by the gate-source capacitance of the second transistor 720. The charge monitor circuit 700 comprises a compensation component 730 to compensate the disturbing charge generated by the second transistor 720 of the charge monitor circuit 700, when the second transistor 720 of the charge monitor circuit 700 is switched between the conductive and non-conductive state.

The compensation component 730 of the charge monitor circuit 700 is configured to compensate the AC-charge component generated by the gate-source capacitance of the second transistor 720 of the charge monitor circuit 700. The compensation component 730 may be configured as a transistor having a control terminal 731 which is controlled by a control signal CM\_OUT\_n. The control signal CM\_OUT\_n is generated by the control circuit 600. The transistor 730 may have a drain and a source terminal which are connected together, as shown in Figure 3. The compensation component 730 thus realizes a capacitor which is effective against the gate-source capacitance of the transistor 720.

25

The controllable reference voltage generator 1000 comprises a loop controller 900 being arranged between the output node O700 of the charge monitor circuit 700 and the reference voltage line 300. The loop controller 900 is configured to generate an output voltage at the reference voltage line 300 in dependence on a comparison of the monitor current  $I_m$  and the reference current  $I_{ref}$ . The loop controller 900 may be configured as an integrator circuit.

30

According to the embodiment of the sensor arrangement 3, the reference voltage  $V_{ref}$  is generated by a control loop realized by the controllable reference voltage generator 1000, which generates the monitor charge/monitor current  $I_m$  at a constant frequency controlled by the control signals  $CM\_REF$ ,  $CM\_OUT$ ,  $CM\_OUT\_n$ . The monitor current  $I_m$  is compared with a constant reference current  $I_{ref}$  derived from the constant current source/bandgap reference. The comparison of the monitor current  $I_m$  and the reference current  $I_{ref}$  is performed by the loop controller 900.

The controllable reference voltage generator 1000 is configured to generate the reference voltage  $V_{ref}$  on the reference voltage line 300 in dependence on the monitor current  $I_m$  of the charge monitor circuit 700 and the reference current  $I_{ref}$  of the constant current source 800. The controllable reference voltage generator 1000 is configured to generate an amount of the monitor current  $I_m$  at the output node 0700 of the charge monitor circuit 700 so that the reference current  $I_{ref}$  of the constant current source 800 is compensated by the monitor current  $I_m$ .

The result of the comparison of the monitor charge/monitor current  $I_m$  with the reference current  $I_{ref}$  is used to adjust the reference voltage  $V_{ref}$  at the reference voltage line 300 so that the monitor charge per time, i.e. the monitor current  $I_m$ , is equal to the reference current  $I_{ref}$ . This means that the charge monitor circuit 700 generates exactly the monitor current  $I_m$  being equal to the reference current  $I_{ref}$ . As a consequence of this, the compensation charge/compensation current  $I_c$  at the output node 0200 is well-defined by the reference current  $I_{ref}$  of the constant current source 800.

The sensor arrangement 3 shown in Figure 3 enables to compensate temperature effects and process variations, because the charge generator 200 and the charge monitor circuit 700 comprise the same components, i.e. the transistors 210/710, 220/720 and 230/730.

Figure 4 shows control signals C\_REF, C\_OUT and C\_OUT\_n generated by the control circuit 600 to control the transistors 210, 220 and 230 of the charge generator 200. The control signals C\_REF and C\_OUT are non-overlapping clock signals. The control signal C\_OUT\_n represents the inversion of the control signal C\_OUT. The first diagram of Figure 4 illustrates the increase of the compensation charge Q\_OUT provided by the charge generator 200 at the output node O200. As shown in Figure 4, each clock period generates a certain amount of compensation charge into the output node O200 of the charge generator 200. This compensation charge is controllable by the reference voltage Vref.

In conclusion, as compared to the conventional topology of a sensor arrangement shown in Figure 1, according to the embodiments 1 and 2 of the sensor arrangement, the limiting parasitic effect of charge injection of the conventional SC implementation of a charge generator is used in the proposed sensor arrangement as the exclusive effect for charge generation. Temperature effects and process variations are compensated by providing an additional reference loop/controllable reference voltage generator in order to control the amount of injected charge.

## List of Reference Signs

|    |      |                                                         |
|----|------|---------------------------------------------------------|
|    | 1    | first embodiment of sensor arrangement                  |
|    | 2    | second embodiment of sensor arrangement                 |
| 5  | 3    | conventional embodiment of sensor arrangement           |
|    | 10   | sensor/photodiode                                       |
|    | 20   | charge generator                                        |
|    | 21   | controllable switch                                     |
|    | 22   | capacitor                                               |
| 10 | 30   | reference voltage line                                  |
|    | 31   | reference voltage source                                |
|    | 40   | integrator                                              |
|    | 100  | sensor/photodiode                                       |
|    | 200  | charge generator                                        |
| 15 | 210  | first transistor                                        |
|    | 212  | parasitic capacitor                                     |
|    | 220  | second transistor                                       |
|    | 230  | compensation device                                     |
|    | 300  | reference voltage line                                  |
| 20 | 310  | reference voltage source                                |
|    | 400  | integrator                                              |
|    | 500  | comparator                                              |
|    | 600  | control circuit                                         |
|    | 700  | charge monitor circuit                                  |
| 25 | 710  | first transistor of charge monitor circuit              |
|    | 720  | second transistor of charge monitor circuit             |
|    | 730  | compensation device of charge monitor circuit           |
|    | 800  | constant current source                                 |
|    | 900  | integrator                                              |
| 30 | 1000 | reference loop/controllable reference voltage generator |

## Claims

1. A sensor arrangement to sense an external signal, comprising:

- 5     - a sensor (100) to provide a sensor current ( $I_s$ ) in dependence from the external signal,
- a charge generator (200) to generate a compensation current ( $I_c$ ) to compensate the sensor current,
- an output node (O200) of the charge generator (200) to  
10    provide the compensation current ( $I_c$ ), wherein the sensor (100) is coupled to the output node (O200) of the charge generator (200) to provide the sensor current of the sensor (100) at the output node (O200) of the charge generator (200),
- 15    - a reference voltage line (300) to provide a reference voltage ( $V_{ref}$ ),
- a control circuit (600) to control the generation of the compensation current ( $I_c$ ),
- wherein the charge generator (200) comprises a first  
20    transistor (210) having a parasitic capacitor (212) and a first conductive path, the first transistor (210) being connected to the reference voltage line (300),
- wherein the charge generator (200) comprises a second transistor (220) having a second conductive path being  
25    coupled in series to the first transistor (210) and coupled to the output node (O200) of the charge generator (200),
- wherein the control circuit (600) is configured to control the conductivity of the respective first and second  
      conductive path of the first and the second transistor (210,  
30    220) of the charge generator (200) so that the sensor current is compensated by the compensation current ( $I_c$ ).

2. The sensor arrangement of claim 1,

wherein the first and the second transistor (210, 220) of the charge generator (200) are controlled by the control circuit (600) to be operated in a conductive and non-conductive state.

5

3. The sensor arrangement of claim 2,

- wherein the charge generator (200) is operated in a first and a second operation state,

10 - wherein the control circuit (600) is configured to control the first transistor (210) of the charge generator (200) in a conductive state and to control the second transistor (220) of the charge generator (200) in a non-conductive state to load the parasitic capacitor (212) by conductively coupling the parasitic capacitor (212) to the reference voltage line  
15 (300) during the first operation state,

- wherein the control circuit (600) is configured to control the first transistor (210) of the charge generator (200) in a non-conductive state and to control the second transistor (220) of the charge generator (200) in a conductive state to  
20 provide the compensation current ( $I_c$ ) at the output node (O200) of the charge generator (200) during the second operation state.

4. The sensor arrangement of claims 2 or 3,

25 wherein the charge generator (200) comprises a compensation component (230) to compensate a disturbing charge generated by the second transistor (220) of the charge generator (200), when the second transistor (220) of the charge generator (200) is switched between the conductive and non-conductive  
30 state.

5. The sensor arrangement of claim 4,

wherein the compensation component (230) of the charge generator (200) is configured to compensate an AC-charge component generated by a gate-source capacitance of the second transistor (220) of the charge generator (200).

5

6. The sensor arrangement of claims 1 to 5, comprising:  
a controllable reference voltage generator (1000) to generate the reference voltage ( $V_{ref}$ ) on the reference voltage line (300).

10

7. The sensor arrangement of claim 6,

- wherein the charge generator (200) comprises at least a first current branch (201), the first current branch (201) including the first transistor (210) and the second

15 transistor (220) and the compensation component (230) of the charge generator (200),

- wherein the controllable reference voltage generator (1000) comprises a charge monitor circuit (700) having at least a second current branch (701) and an output node (0700), the  
20 second current branch (701) being coupled between the reference voltage line (300) and the output node (0700) of the charge monitor circuit (700),

- wherein the charge monitor circuit (700) is configured to provide a monitor current ( $I_m$ ) to the output node (0700) of  
25 the charge monitor circuit (700).

8. The sensor arrangement of claim 7,

- wherein the controllable reference voltage generator (1000) comprises a constant current source (800) to generate a  
30 reference current ( $I_{ref}$ ),

- wherein the controllable reference voltage generator (1000) is configured to generate the reference voltage ( $V_{ref}$ ) in dependence on the monitor current ( $I_m$ ) of the charge monitor

circuit (700) and the reference current ( $I_{ref}$ ) of the constant current source (800).

9. The sensor arrangement of claim 8,

5 wherein the controllable reference voltage generator (1000) is configured to generate an amount of the monitor current ( $I_m$ ) at the output node (O700) of the charge monitor circuit (700) so that the reference current ( $I_{ref}$ ) of the constant current source (800) is compensated by the monitor current  
10 ( $I_m$ ).

10. The sensor arrangement of claims 7 to 9,

- wherein the charge monitor circuit (700) comprises a first transistor (710) and a second transistor (720),

15 - wherein the first transistor (710) of the charge monitor circuit (700) has a parasitic capacitor (712) and a first conductive path, the first transistor (710) of the charge monitor circuit (700) is connected to the reference voltage line (300),

20 - wherein the second transistor (720) of the charge monitor circuit (700) has a second conductive path being coupled in series to the first transistor (710) of the charge monitor circuit (700) and coupled to the output node (O700) of the charge monitor circuit (700).

25

11. The sensor arrangement of claim 10,

wherein the first and the second transistor (710, 720) of the charge monitor circuit (700) are controlled by the control circuit (600) to be operated in a conductive and non-  
30 conductive state.

12. The sensor arrangement of claims 10 or 11,

- wherein the charge monitor circuit (700) is operated in a first and a second operation state,
  - wherein the control circuit (600) is configured to control the first transistor (710) of the charge monitor circuit (700) in a conductive state and to control the second transistor (720) of the charge monitor circuit (700) in a non-conductive state to load the parasitic capacitor (712) by conductively coupling the parasitic capacitor (712) to the reference voltage line (300) during the first operation state of the charge monitor circuit,
  - wherein the control circuit (600) is configured to control the first transistor (710) of the charge monitor circuit (700) in a non-conductive state and to control the second transistor (720) of the charge monitor circuit (700) in a conductive state to provide the monitor current ( $I_m$ ) at the output node (O700) of the charge monitor circuit (700) during the second operation state of the charge monitor circuit (700).
13. The sensor arrangement of claims 10 to 12, wherein the charge monitor circuit (700) comprises a compensation component (730) to compensate a disturbing charge generated by the second transistor (720) of the charge monitor circuit (700), when the second transistor (720) of the charge monitor circuit (700) is switched between the conductive and non-conductive state.
14. The sensor arrangement of claims 7 to 13,
- wherein the controllable reference voltage generator (1000) comprises a loop controller (900) being arranged between the output node (O700) of the charge monitor circuit (700) and the reference voltage line (300),

- wherein the loop controller (900) is configured to generate an output voltage at the reference voltage line (300) in dependence on a comparison of the monitor current ( $I_m$ ) and the reference current ( $I_{ref}$ ).

5

15. The sensor arrangement of claim 14,  
wherein the loop controller (900) is configured as an integrator circuit.

FIG 1

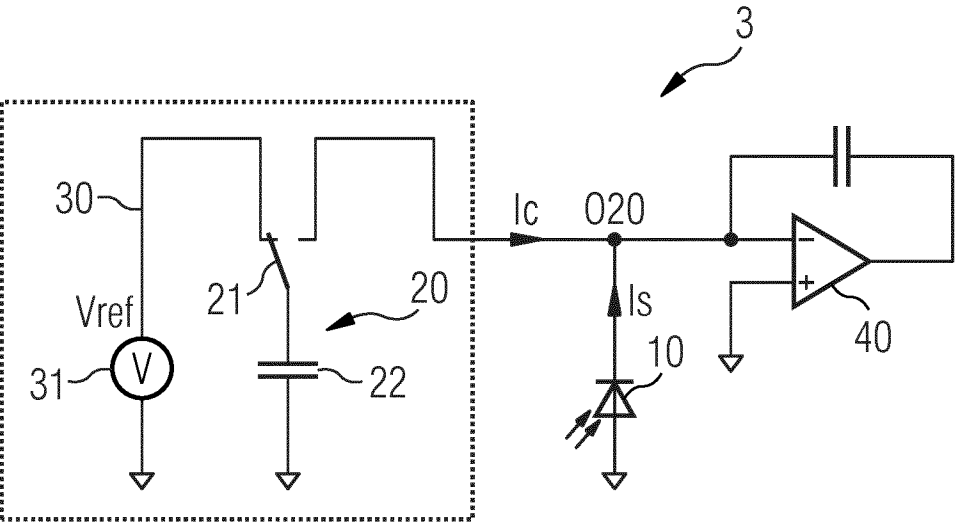


FIG 2

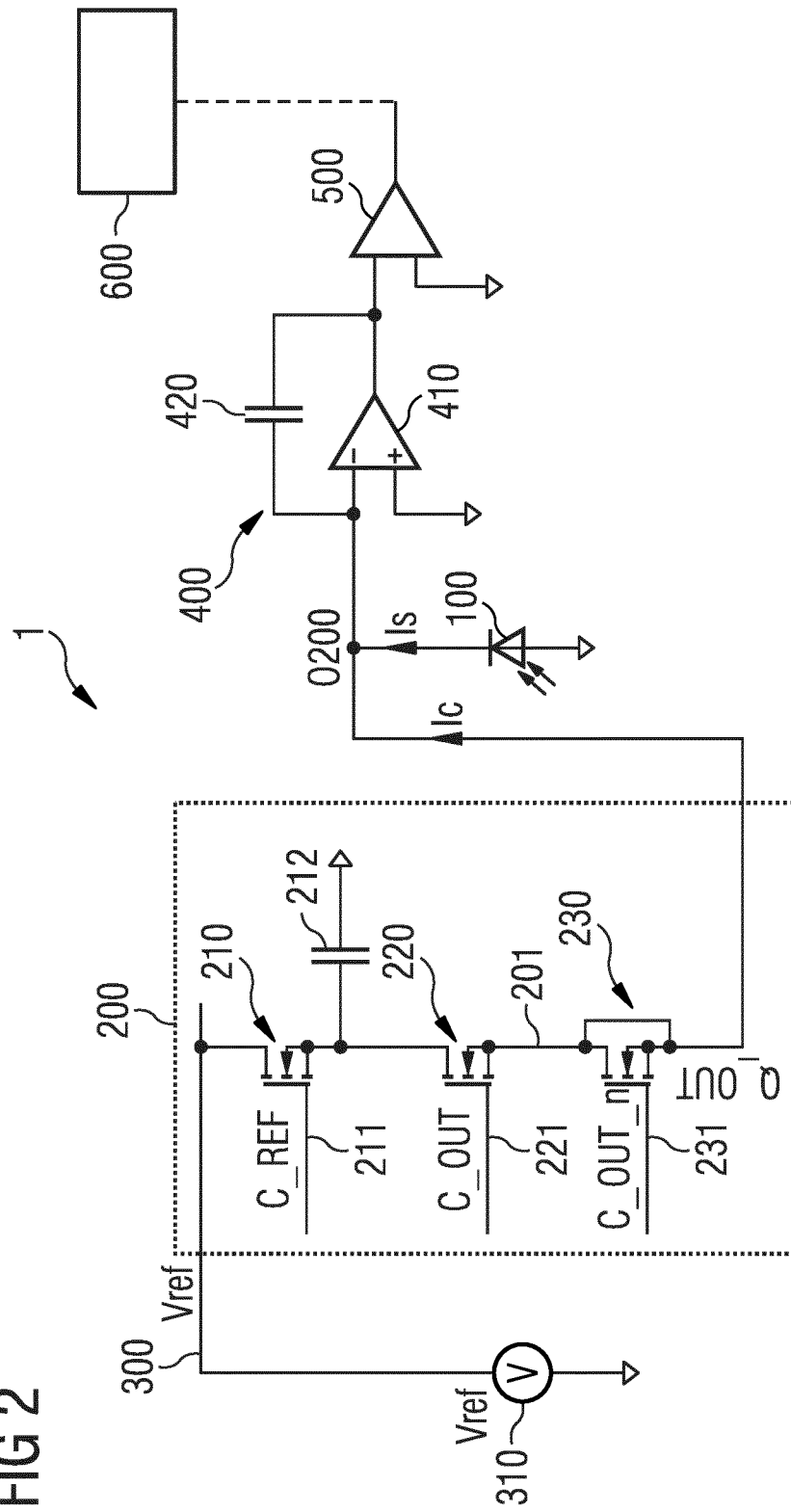


FIG 3

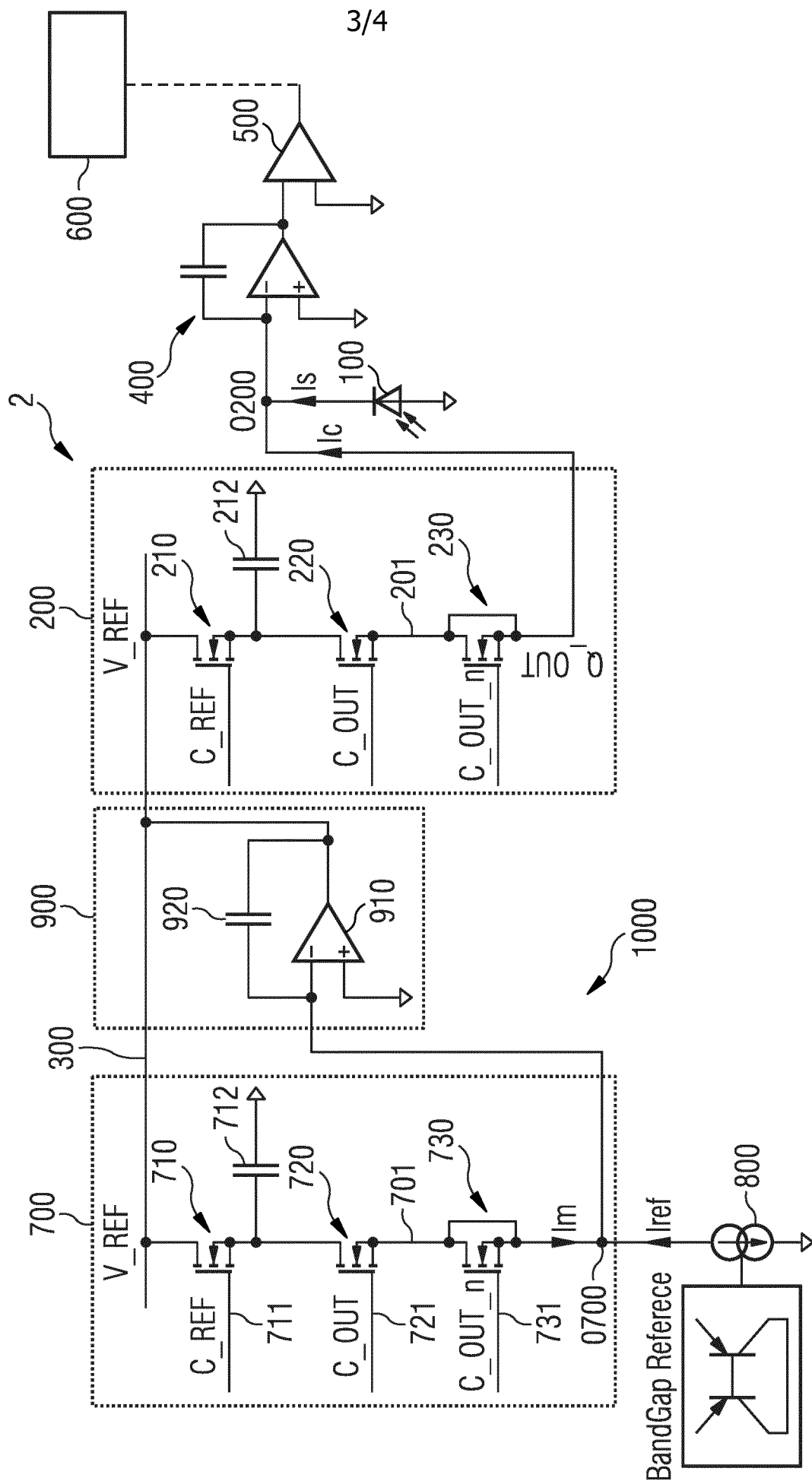
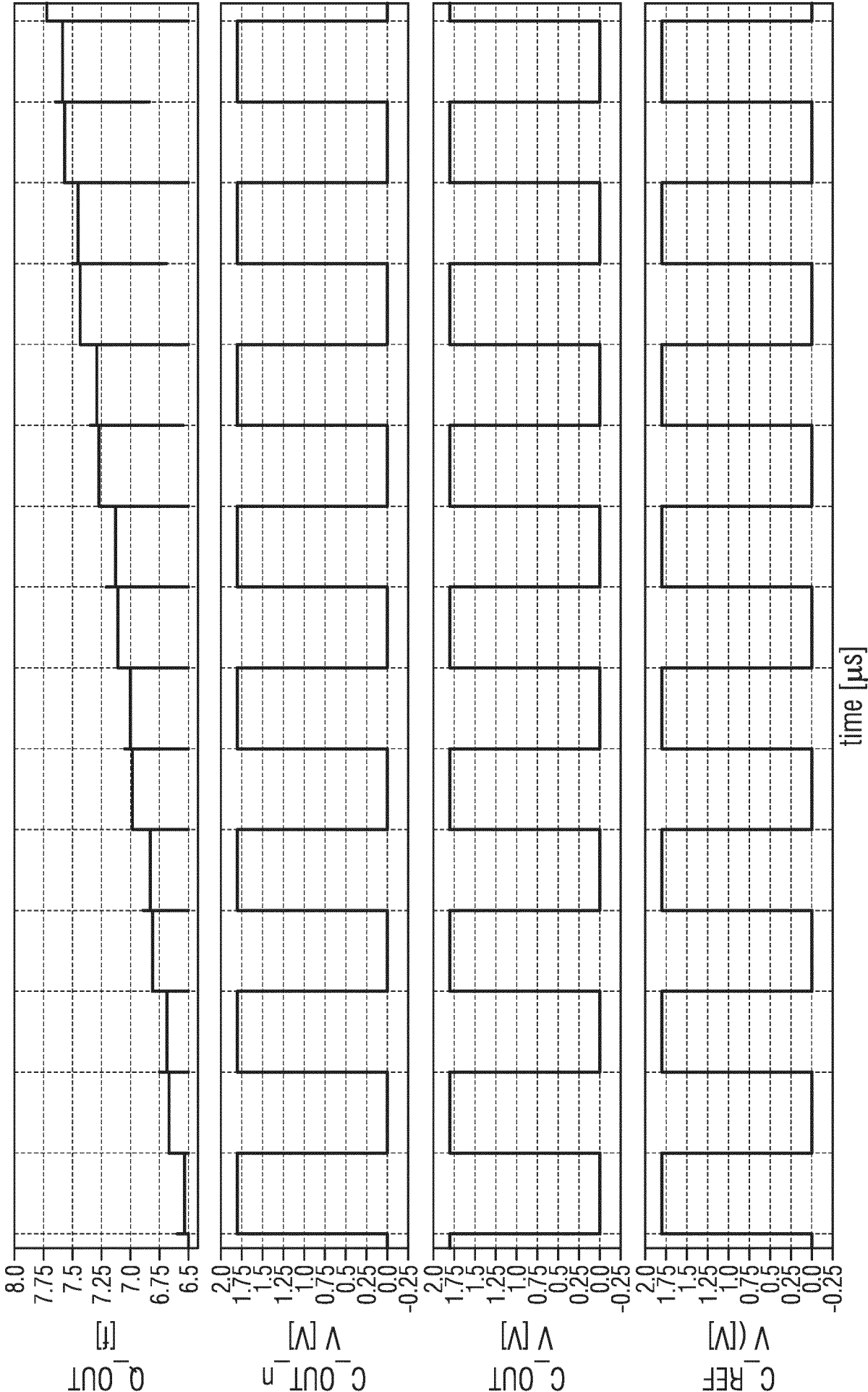


FIG 4



# INTERNATIONAL SEARCH REPORT

International application No  
PCT/EP2018/081039

A. CLASSIFICATION OF SUBJECT MATTER  
INV. H03K17/16  
ADD. H03K17/94

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03K G01D H04B H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                            | Relevant to claim No. |
|-----------|-------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| X         | US 2013/112848 A1 (LIN JOSEPH H [US] ET AL) 9 May 2013 (2013-05-09)<br>figure 6A<br>paragraph [0058]<br><br>-----<br><br>-/-- | 1-5                   |



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

14 January 2019

Date of mailing of the international search report

20/03/2019

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040,  
Fax: (+31-70) 340-3016

Authorized officer

Simon, Volker

# INTERNATIONAL SEARCH REPORT

International application No  
PCT/EP2018/081039

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                                                                                                                                                                                                                        | Relevant to claim No. |
|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| A         | <p>Behzad Razavi: "Introduction to Switched-Capacitor Circuits",<br/>3 September 2013 (2013-09-03),<br/>XP055392576,<br/>Retrieved from the Internet:<br/>URL:https://web.archive.org/web/2013090301127if_/http://www.seas.ucla.edu:80/brweb/teaching/AIC_Ch12.pdf<br/>[retrieved on 2017-07-20]<br/>paragraph 12.2.4 Charge Injection Cancellation;<br/>page 411 - page 413<br/>figures 12.24, 12.25</p> | 4,5                   |
| A         | <p>-----<br/>Roubik Gregorian ET AL: "NONIDEAL EFFECTS IN SWITCHED-CAPACITOR CIRCUITS; Nonideal Effects in the Switches"<br/>In: "Analog CMOS Integrated Circuits for Signal Processing",<br/>31 December 1986 (1986-12-31), Wiley,<br/>XP055470461,<br/>ISBN: 978-0-471-62569-8<br/>pages 462-474,<br/>page 469 - page 470<br/>figures 7.8, 7.9<br/>-----</p>                                            | 4,5                   |

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/EP2018/081039

### Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

### Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-5

#### Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

**FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210**

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-5

charge injection compensation for a switch  
---

2. claims: 6-15

implementation of a controllable reference voltage generator  
---

## INTERNATIONAL SEARCH REPORT

### Information on patent family members

International application No

PCT/EP2018/081039

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s) | Publication<br>date |
|-------------------------------------------|---------------------|----------------------------|---------------------|
| US 2013112848 A1                          | 09-05-2013          | US 2013112848 A1           | 09-05-2013          |
|                                           |                     | US 2016050382 A1           | 18-02-2016          |
|                                           |                     | US 2017295337 A1           | 12-10-2017          |
| -----                                     |                     |                            |                     |