(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 January 2015 (29.01.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/010328 A1

(51) International Patent Classification:
H03F 1/32 (2006.01)

(21) International Application Number:
PCT/CN2013/080205

(22) International Filing Date:
26 July 2013 (26.07.2013)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **NOKIA SIEMENS NETWORKS OY** [FI/FI]; Karaportti 3, FI-02610 Espoo (FI).

(72) Inventors; and

(71) Applicants *(for DM only)*: **YANG, Xiaokun** [CN/CN]; No. 1, Wang Jing East Road, Chaoyang District, Beijing 100102 (CN). **WANG, Zhancang** [CN/CN]; 1171, Building 31, Sun Wang Chang, Yun Jing Xi Li, Li Yuan, Tongzhou District, Beijing 101101 (CN).

(72) Inventor: **LANFRANCO, Sandro**; 3101 Magliocco Drive, APT 412, San Jose, California 95128 (US).

(74) Agent: **KING & WOOD MALLESONS**; 20th Floor, East Tower, World Financial Center, No. 1 Dongsanhuan Zhonglu, Chaoyang District, Beijing 100020 (CN).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

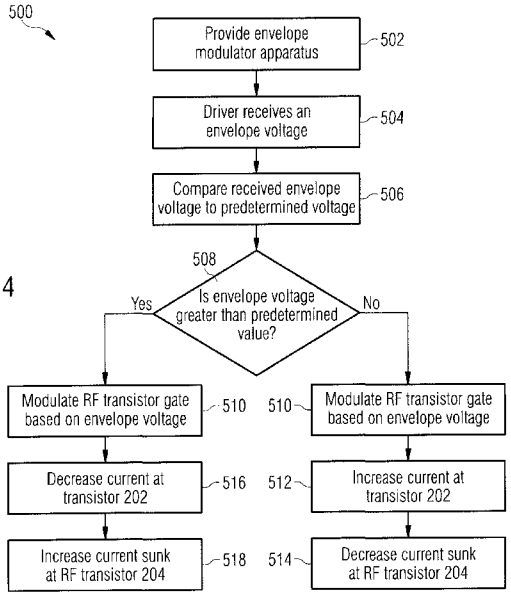
— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: METHOD, APPARATUS AND SYSTEM FOR ENVELOPE TRACKING

FIG 4



(57) **Abstract**: This disclosure relates generally to the field of wireless communication infrastructure, and more particularly to a method, apparatus and system for envelope tracking. The system for envelope tracking comprising: a transistor; an RF transistor; a driver; a switcher current source; and a subtracting network; wherein the system is configured such that when an envelope voltage is less than a predetermined voltage value, the RF transistor is configured for decreasing an amount of absorbed biasing current, and when the envelope voltage is greater than a predetermined voltage value, the RF transistor is configured for increasing an amount of absorbed biasing current. The goal of RF transistor sinking is to absorb the redundant biasing current generated by the envelope tracking supply modulator to eliminate distortions.

WO 2015/010328 A1

METHOD, APPARATUS AND SYSTEM FOR ENVELOPE TRACKING

FIELD OF TECHNOLOGY

[0001] This disclosure relates generally to the field of wireless communication infrastructure, and more particularly to a method, apparatus and system for envelope tracking.

BACKGROUND

[0002] In the wireless communication infrastructure industry, one technique that is utilized to enhance radio power amplifier (PA) efficiency is envelope tracking (ET). Envelope Tracking is a known approach to RF power amplifier design in which the power supply voltage applied to the PA is constantly adjusted to ensure that the PA is operating at peak efficiency over output power range.

[0003] Generally speaking, envelope tracking is high-efficiency architecture for power amplifiers. However, it is typically not used in commercial base transceiver station (BTS) power amplifiers because the necessary envelope modulator is difficult to implement.

SUMMARY

[0004] In one embodiment of the present disclosure, an apparatus for envelope tracking is provided and includes a power transistor, an RF transistor, a driver, a switcher current source, and a subtracting network.

[0005] In another embodiment of the present disclosure, a system for envelope tracking is provided and includes a transistor, an RF transistor, a driver, a switcher current source, and a subtracting network, wherein the system is configured such that when an envelope voltage is less than a predetermined voltage value, the RF transistor is configured to aid envelope tracking power supply for decreasing an amount of absorbed

biasing current, and when the envelope voltage is greater than a predetermined voltage value, the RF transistor is configured to aid envelope tracking power supply for increasing an amount of absorbed biasing current. The goal of RF transistor sinking is to absorb the redundant biasing current generated by the envelope tracking supply modulator to eliminate distortions.

[0006] In another embodiment of the present disclosure, a method for envelope tracking is provided and includes the steps of providing an envelope modulator apparatus, the apparatus including a transistor, an RF transistor, a driver, a switcher current source and a subtracting network; modulating, at the subtracting network, a gate of the RF transistor based on an envelope voltage; and sinking, at the RF transistor, redundant biasing current generated by the envelope modulator apparatus.

DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0007] To aid in the proper understanding of the present disclosure, reference should be made to the accompanying drawings, wherein:

[0008] Figure 1 is a circuit diagram showing an example prior art envelope modulator architecture;

[0009] Figure 2 is a circuit diagram of envelope modulator architecture in accordance with an embodiment of the present disclosure;

[0010] Figure 3 is a circuit implementation diagram of envelope modulator architecture in accordance with an embodiment of the present disclosure;

[0011] Figure 4 is a flow chart showing a method for envelope tracking in accordance with an embodiment of the present disclosure; and

[0012] Figure 5 is a graphical representation of an envelope tracking system utilizing the present disclosure.

DETAILED DESCRIPTION

[0013] Referring first to Figure 1, a conventional envelope tracking system 100 is illustrated. The system 100 includes a driver 102, a first power transistor (T1) 104, a second power transistor (T2) 106, a switcher current source 108, and a RF transistor 110. In the system 100, the driver 102, first power transistor 104 and second power transistor 106 form a linear envelope amplifier, which provides the proper envelope voltage to the RF transistor 110 as power supply. The current to the system is primarily provided by the switcher current source 108, which can be a BUCK DC-DC converter or Isw, although similar converters may be utilized, as recognized by those having ordinary skill of the art. However, the BUCK switcher does detail an exemplary application of the present invention. The reader should not construe any context specific examples given herein as limiting the present invention. The first power transistor 104 and the second power transistor 106 are configured for correcting the current to the system when needed by sourcing current and sinking current, respectively; more specifically, the first power transistor 104 can add or source current when needed, and the second power transistor can absorb or sink current when needed.

[0014] In the system 100, envelope voltage is received at the driver 102 and then sent on to a first transistor gate 112 and a second transistor gate 114, respectively. The switcher current source 108 provides current to the system, as mentioned briefly above. When current through the RF transistor 110 is low (based on an earlier predetermination made in another part of the system and not discussed in detail herein), the envelope voltage at a T1-T2-I_{sw} junction 116 is also low. To address this low voltage/low current situation, the driver 102 acts to change the voltage at the first transistor gate 112 and the second transistor gate 114, which in turn forces T1 104 to provide more current to the RF transistor 110 and T2 106 to sink or absorb less current. The net result is an increase to the current traveling through the RF transistor 110, which renders a higher and more efficient envelope voltage received at the RF transistor.

[0015] As clearly seen in the prior art system 100 of Figure 1, three total transistors are utilized: T1 104, T2 106 and the RF transistor 110. While this system does in the end

provide the proper envelope voltage to the RF transistor as power supply, the high number of system components can lead to reduced efficiency, a decreased bandwidth and a larger circuitry profile.

[0016] Referring next to Figures 2, an envelope tracking apparatus, system and method for envelope tracking in accordance with the present disclosure is provided. Turning first to Figure 2, an envelope tracking apparatus 200 is provided and includes a transistor (T1) 202, a RF transistor 204, a driver 206, a switcher current source 208, and a subtracting network 210. The current to the apparatus 200 is primarily provided by the switcher current source 208, which can be a BUCK DC-DC converter switcher current source or Isw, although similar converters may be utilized, as recognized by those having ordinary skill of the art. However, the BUCK switcher does detail an exemplary application of the present invention. The reader should not construe any context specific examples given herein as limiting the present invention. The transistor 202 and the RF transistor 204 are configured for correcting the current to the apparatus 200 when needed; more specifically, the transistor 202 can add current when needed, and the RF transistor 204 can sink or absorb biasing current when needed. Both biasing current and current from a DC-to-RF energy conversion flow through the RF transistor 204. In accordance with the present disclosure, the biasing or quiescent current of the RF transistor 204 is being acted upon (i.e., “sunk” or “absorbed”), which in turn effects the total current flowing through the RF transistor.

[0017] The driver 206 is configured for receiving envelope voltage and comparing the envelope voltage to a predetermined voltage value that is predetermined elsewhere in the system and therefore not described in detail herein. As will be described in further detail below, based on whether the envelope voltage is greater than or less than the predetermined voltage value, the driver 206 can act to adjust voltage in the apparatus 200 to ensure that an appropriate envelope voltage is provided to the RF transistor 204.

[0018] The subtracting network 210 in the present disclosure can be a combination of a passive transformer 300 (further described with respect to Figure 3) and an active operational amplifier 400 (also further described with respect to Figure 3), although it is appreciated that other similar apparatuses may be possible. As seen in Figure 2, the subtracting network 210 has three inputs, identified as "1", "2" and "4", and one output, identified as "3". Although three inputs and one output are disclosed herein, it is recognized that fewer or more inputs/outputs may be utilized, and the present disclosure is not limited to the three inputs and one output disclosed in this application.

[0019] As seen in Figure 2, the apparatus 200 further includes a transistor gate 212 and an RF transistor gate 214. When the envelope voltage at a T1-I_{sw} junction 216 is above the predetermined value, the driver 206 is configured to decrease the current through the transistor 202 (by acting on the transistor gate 212) and to increase the biasing current of the RF transistor 204 (by acting on the RF transistor gate 214). When the envelope voltage is below the predetermined value, the driver 206 is configured to increase the current through the transistor 202 (by acting on the transistor gate 212) and to decrease the biasing current of the RF transistor 204 (by acting on the RF transistor gate 214). Although the present apparatus 200 is described in the context of a base station application, it is appreciated that the apparatus 200, system and method (both described in further detail below) can be utilized in handsets and other portable wireless devices.

[0020] In other words, the apparatus 200 is configured such that when the envelope voltage exceeds the predetermined voltage value, the transistor 202 is configured for providing a decreased amount of current and the RF transistor 204 is configured for increasing the biasing current (i.e., sinking more of the biasing current). In contrast, when the envelope voltage is less than the predetermined voltage value, the transistor 202 is configured for providing an increased amount of current and the RF transistor 204 is configured for decreasing an amount of the biasing current (i.e., sinking less biasing current).

[0021] In accordance with the above, therefore, a system for envelope tracking is provided and includes the transistor 202, the RF transistor 204, the driver 206, the switcher current source 208, and the subtracting network 210. As described above, the system is configured such that when the envelope voltage is less than the predetermined voltage value, the RF transistor 204 is configured for decreasing an amount of absorbed biasing current, and when the envelope voltage is greater than the predetermined voltage value, the RF transistor 204 is configured for increasing an amount of absorbed biasing current.

[0022] More specifically, when the voltage at the T1-I_{sw} junction 216 is low, the current through the RF transistor 204 is also low. As a result, the driver 206 acts to change the voltage at the transistor gate 212 and, via the subtracting network, 210, the voltage at the RF transistor gate 214. This forces the transistor 202 to provide more current and the RF transistor 204 to sink or absorb less biasing current, thus increasing the voltage at the T1-I_{sw} junction 216. Similarly, when the voltage at the T1-I_{sw} junction 216 is high (i.e., the voltage exceeds the upper limit voltage value), the current through the RF transistor 204 is also high. Such a result would then force the driver 206 to change the voltage at the transistor gate 212 and, via the subtracting network 210, the voltage at the RF transistor gate 214, thereby forcing the transistor 202 to provide less current and the RF transistor 204 to sink or absorb more biasing current. This leads to an overall decreased amount of voltage at theT1-I_{sw} junction 216.

[0023] Turning now to Figure 3, in both the apparatus 200 and the system described above, the subtracting network 210 can be the passive transformers 300. The passive transformers 300, as known in the art, are configured for either stepping voltage up or stepping voltage down via induction. Briefly, the transformers 300 work on the principle that energy can be efficiently transferred by magnetic induction from one winding to another winding by a varying magnetic field produced by alternating current (AC). An electrical voltage is induced when there is a relative motion between a wire and a magnetic field. The AC provides the motion required by changing direction which creates a collapsing and expanding magnetic field.

[0024] When the passive transformers 300 are utilized in place of the subtracting network 210, the system and apparatus 200 work in much the same manner as described above with respect to Figure 2. However, when the passive transformers 300 are provided, they act to change the voltage at the RF transistor gate 214 through induction and subtracting node operation, as known in the art. In other words, when the voltage at the T1-I_{sw} junction 216 is low, the driver 206 acts to change the voltage at the transistor gate 212, and via the passive transformers 300, to change the voltage at the RF transistor gate 214. Specifically, when the voltage at the T1-I_{sw} junction 216 is low, the passive transformer 300 is such that a primary winding (not shown) has more turns than a secondary winding (not shown), and the operational amplifier outputs a decreased control voltage, thereby resulting in a decreased voltage output at the RF transistor gate 214. Accordingly, the current provided by the transistor 202 is increased and the amount of biasing current sunk or absorbed by the RF transistor 204 is decreased.

[0025] Similarly, when the voltage at the T1-I_{sw} junction 216 is high, the driver 206 acts to change the voltage at the transistor gate 212, and via the passive transformers 300, to change the voltage at the RF transistor gate 214. Specifically, when the voltage at the T1-I_{sw} junction 216 is high, the passive transformers 300 is such that the primary winding has more turns than the secondary winding, the operational amplifier output an increased control voltage, thereby resulting in an increased voltage output at the RF transistor gate 214. Accordingly, the current provided by the transistor 202 is decreased and the amount of biasing current sunk or absorbed by the RF transistor 204 is increased.

[0026] Referring still to Figure 3 and as briefly mentioned above, in the apparatus 200 and system of Figure 2, the subtracting network can be a pair of transformers serving as a coupler to scale down the voltage sensed, and an active operational amplifier 400. As known in the art, in an operational amplifier, the voltage entering into the amplifier positive input port subtracts the voltage entering into the negative input port. The difference or error voltage between input ports is amplified and output by the amplifier, and vice versa. As seen in Figure 3, when the voltage at the T1-I_{sw} junction 216 is low, the driver 206 acts

to change the voltage at the transistor gate 212, and via the operational amplifier 400, to change the voltage at the RF transistor gate 214. Specifically, when the voltage at the T1-I_{sw} junction 216 is low, the operational amplifier 400 acts such that the transistor gate 212 voltage scaled down and the transistor 202 output voltage scaled down are the inputs in the operational amplifier, resulting in a subtracted difference or error voltage output, thereby leading to a decreased voltage output at the RF transistor gate 214. Accordingly, the current provided by the transistor 202 is increased and the amount of biasing current sunk or absorbed by the RF transistor 204 is decreased.

[0027] Similarly, when the voltage at the T1-I_{sw} junction 216 is high, the driver 206 acts to change the voltage at the transistor gate 212, and via the inverter amplifier 400, to change the voltage at the RF transistor gate 214. Specifically, when the voltage at the T1-I_{sw} junction 216 is high, the operational amplifier 400 acts such that the transistor gate 212 voltage scaled down and the transistor 202 output voltage scaled down are the inputs in the operational amplifier, resulting in a subtracted difference or error voltage output, thereby leading to an increased voltage output at the RF transistor gate 214. Accordingly, the current provided by the transistor 202 is decreased and the amount of biasing current sunk or absorbed by the RF transistor 204 is increased, resulting in an overall decreased current through the RF transistor 204.

[0028] Referring next to Figure 4, an envelope tracking method 500 is provided. Specifically, the method 500 includes providing an envelope modulator apparatus, the apparatus including a power transistor, an RF transistor, a driver, a switcher current source and a subtracting network (block 502). Next, the driver receives an envelope voltage (block 504). Once the envelope voltage is received, the driver compares the received envelope voltage to a predetermined voltage (block 506), and determines whether the received voltage is greater than or less than the predetermined voltage (block 508).

[0029] Based on this determination, the subtracting network modulates a gate of the RF transistor based on an envelope voltage (block 510). Similar to the apparatus 200

and the system described above, the modulation at the subtracting network can occur at the passive transformers 300 and the active operational amplifier 400 combination.

[0030] Next, redundant biasing current is sunk at the RF transistor. More specifically, if the envelope voltage is less than the predetermined value, the method includes the steps of increasing a current at the transistor 202 (block 512) and decreasing the amount of biasing current absorbed at the RF transistor 204 (block 514). In contrast, if the envelope voltage is more than the predetermined value, the method includes the steps of decreasing the current at the transistor 202 (block 516) and increasing the amount of biasing current absorbed at the RF transistor (block 518).

[0031] As described above, the present disclosure provides an apparatus, system and method for envelope tracking. The present apparatus 200 provides a transistor 202 and an RF transistor 204, which is in contrast to conventional envelope tracking apparatus that generally have a first transistor, a second transistor and an RF transistor. The present apparatus, therefore, provides an envelope tracking apparatus, system and method with fewer components. In addition, the present disclosure provides improved integration capabilities, as the RF transistor is now part of the envelope tracking modulator apparatus, rather than a separate component. Further, the present disclosure provides the potential for a wider bandwidth performance because there is no longer a T2 or second transistor, as generally found in the prior art. With the removal of T2, the total parasitic capacitance will decrease, which can lead to a wider bandwidth performance. The present disclosure also provides a reduced cost system compared to conventional envelope tracking systems, because the high cost component T2 has been replaced with lower cost subtracting networks. Also, the present disclosure provides for a more efficient envelope tracking apparatus/system/method when compared with conventional systems.

[0032] Referring now to Figure 5, a simulation bench is performed on an RF power transistor, matched to 850MHz, with stimulus as 4G LTE 16QAM FDD up link SC-FDMA signal with 5MHz bandwidth, peak to average power ratio (PAPR) is ~7dB. The

instantaneous power-added efficiency (PAE) and distribution of load signal power histogram is shown together for comparison. As seen in the Figure 5, the blue invention instantaneous efficiency (utilizing the present disclosure) is higher than the prior art envelope tracking solution (shown in red). Key performance metric comparison summary is shown as below table.

	Output Power (dBm)	Average PAE (%)	EVM RMS (%)
Invention	24.98	29.57	5.87
Prior Art	24.95	25.95	2.85
Class-AB	24.97	19.88	3.73

[0033] Embodiments of the present disclosure may be implemented in software (executed by one or more processors), hardware (e.g., an application specific integrated circuit), or a combination of software and hardware. In an example embodiment, the software (e.g., application logic, an instruction set) is maintained on any one of various conventional non-transitory computer-readable media. In the context of this document, a "non-transitory computer-readable medium" may be any media or means that can contain, store, communicate, propagate or transport the instructions for use by or in connection with an instruction execution system, apparatus, or device, such as a computer. A non-transitory computer-readable medium may comprise a computer-readable storage medium (e.g., memory or other device) that may be any media or means that can contain or store the instructions for use by or in connection with an instruction execution system, apparatus, or device, such as a computer.

[0034] If desired, the different functions discussed herein may be performed in a different order and/or concurrently with each other. Furthermore, if desired, one or more of the above-described functions may be optional or may be combined.

[0035] Although various aspects of the disclosure are set out in the independent claims, other aspects of the disclosure comprise other combinations of features from the described embodiments and/or the dependent claims with the features of the independent claims, and not solely the combinations explicitly set out in the claims.

[0036] It is also noted herein that while the above describes example embodiments of the disclosure, these descriptions should not be viewed in a limiting sense. Rather, there are several variations and modifications which may be made without departing from the scope of the present disclosure as defined in the appended claims.

[0037] One having ordinary skill in the art will readily understand that the disclosure as discussed above may be practiced with steps in a different order, and/or with hardware elements in configurations which are different than those which are disclosed. Therefore, although the disclosure has been described based upon these preferred embodiments, it would be apparent to those of skill in the art that certain modifications, variations, and alternative constructions would be apparent, while remaining within the spirit and scope of the disclosure. In order to determine the metes and bounds of the disclosure, therefore, reference should be made to the appended claims.

[0038] The following abbreviations that may be found in the specification and/or the drawing figures are defined as follows:

AC = Alternating Current

BTS = Base Transceiver Station

ET = Envelope Tracking

EVM = Error Vector Magnitude

FDD = Frequency Division Dual

LTE = Long Term Evolution

PA = Power Amplifier

PAE = Power Added Efficiency

PAPR = Peak to Average Power Ratio

RF = Radio Frequency

RMS = Root Mean Squared

SC-FDMA = Single-carrier Frequency-Division Multiple Access

4G = Fourth Generation Wireless Communication

WHAT IS CLAIMED IS:

1. An apparatus comprising:

   a power transistor;

   an RF transistor;

   a driver;

   a switcher current source; and

   a subtracting network.

2. The apparatus of claim 1 wherein the apparatus is an envelope modulator.

3. The apparatus of claim 1 wherein the RF transistor is in communication with the subtracting network and is configured for absorbing biasing current in the apparatus.

4. The apparatus of claim 1 wherein the driver is configured for receiving envelope voltage and comparing the envelope voltage to a predetermined voltage value.

5. The apparatus of claim 4 further including:

   a transistor gate; and

   an RF transistor gate;

   wherein when the envelope voltage is above the predetermined value, the driver is configured to decrease the current through the transistor by acting on the transistor gate by decreasing bias and by acting on the RF transistor gate by increasing bias.

6. The apparatus of claim 4 further including:

   a transistor gate; and an RF transistor gate;

   wherein when the envelope voltage is below the predetermined value, the driver is configured to increase the current through the transistor by acting on the transistor gate by increasing bias and by acting on the RF transistor gate by decreasing bias.

7. The apparatus of claim 4 wherein when the envelope voltage exceeds the predetermined voltage value, the RF transistor is configured for increasing an amount of absorbed biasing current.

8. The apparatus of claim 4 wherein when the envelope voltage is less than the predetermined voltage value, the RF transistor is configured for decreasing an amount of absorbed biasing current.

9. The apparatus of claim 1 wherein the switcher current source is a BUCK DC-DC converter configured for providing current to the transistor and the RF transistor.

10. The apparatus of claim 1 wherein the subtracting network includes two passive transformers for signal coupling and scaling down.

11. The apparatus of claim 1 wherein the subtracting network includes an active operational amplifier to generate and amplify an error signal.

12. A system for envelope tracking comprising:

a transistor;

an RF transistor;

a driver;

a switcher current source; and

a subtracting network;

wherein the system is configured such that when an envelope voltage is less than a predetermined voltage value, the RF transistor is configured for decreasing an amount of absorbed biasing current, and when the envelope voltage is greater than a predetermined voltage value, the RF transistor is configured for increasing an amount of absorbed biasing current.

13. The system of claim 12 wherein the subtracting network includes two passive transformers for signal coupling and scaling down.

14. The system of claim 12 wherein the subtracting network includes an active operational amplifier to generate and amplify an error signal.

15. A method comprising:

providing an envelope modulator apparatus, the apparatus including a transistor, an RF transistor, a driver, a switcher current source and a subtracting network;

modulating, at the subtracting network, a gate of the RF transistor based on an envelope error voltage; and

sinking, at the RF transistor, redundant biasing current generated by the transistor.

16. The method of claim 15 further including the steps of, prior to the modulating:

receiving, at the driver, the envelope voltage;

comparing, at the driver, the received envelope voltage to a predetermined voltage; and

determining, based on the predetermined voltage, whether the received envelope voltage is greater than or is less than the predetermined voltage.

17. The method of claim 16 further including the steps of, in response to the determining:

increasing a current at the transistor if the envelope voltage is less than the predetermined value; and

decreasing the sunk biasing current at the RF transistor if the envelope voltage is less than the predetermined value.

18. The method of claim 16 further including the steps of, in response to the determining:

decreasing the current at the transistor if the envelope voltage is greater than a predetermined value; and

increasing the sunk biasing current at the RF transistor if the envelope voltage is greater than the predetermined value.

19. The method of claim 15 wherein the modulating occurs at two passive transformers for signal coupling and scaling down.

20. The method of claim 15 wherein the modulating occurs at an active operational amplifier to generate and amplify the error signal.

FIG 1 PRIOR ART

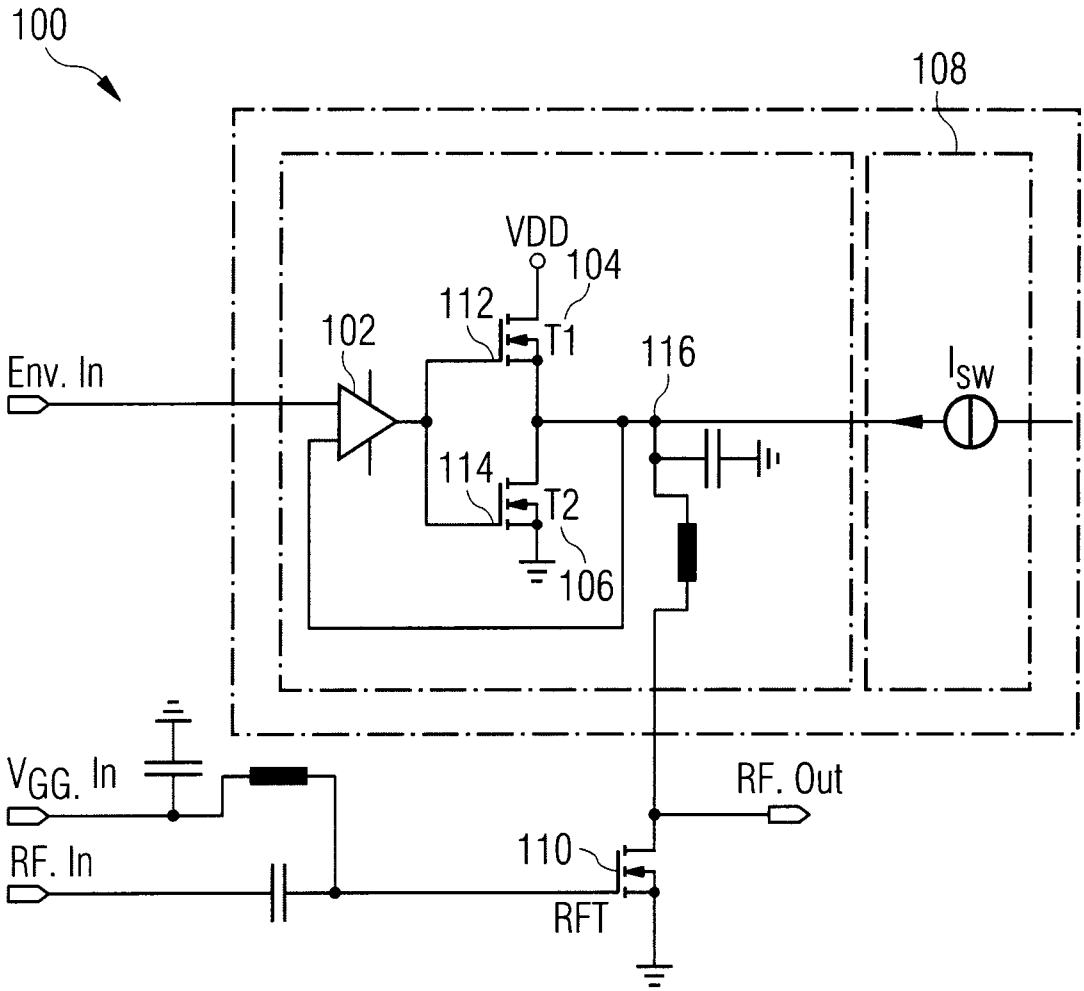


FIG 2

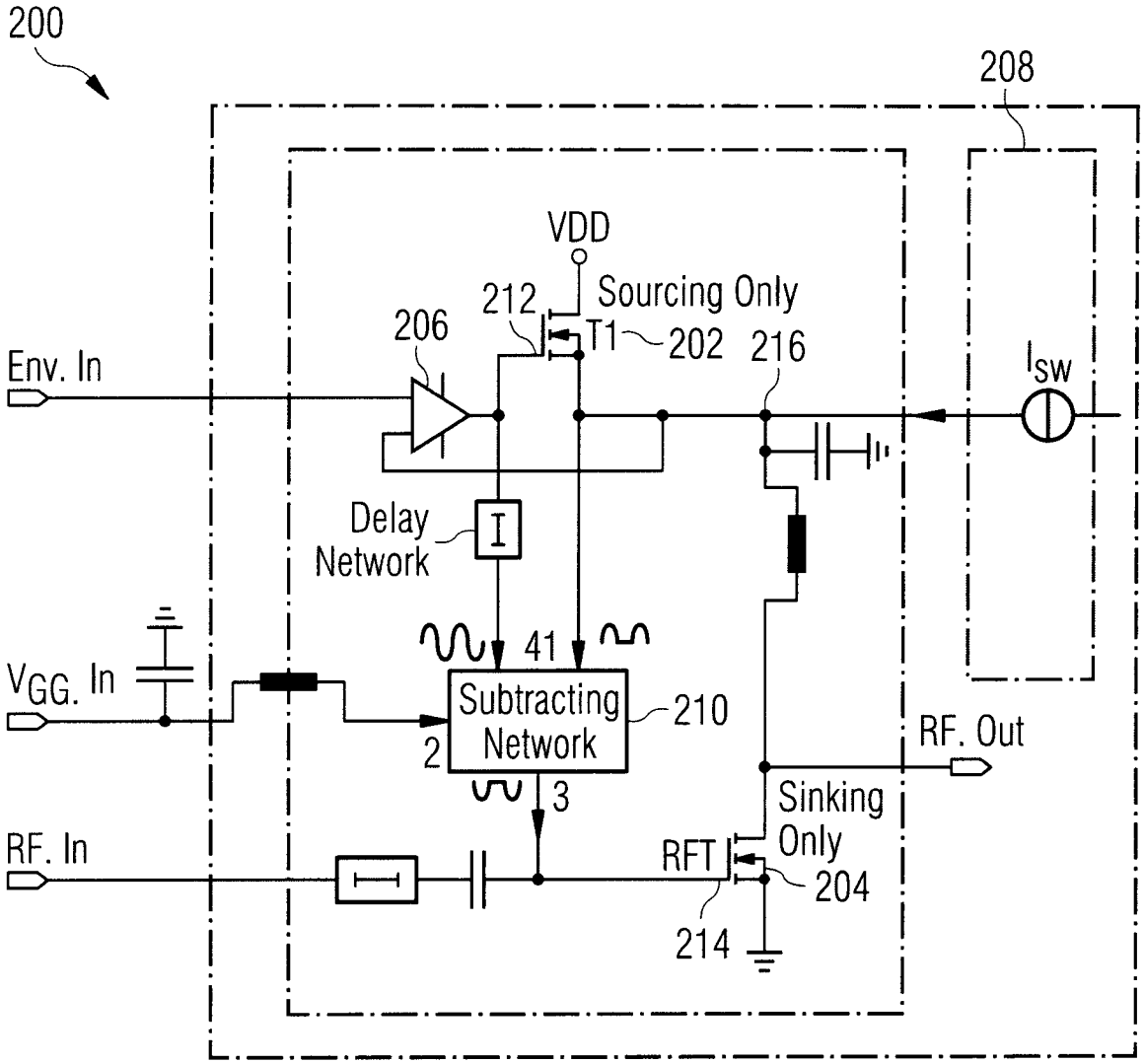

200
208
VDD
212
Sourcing Only
206
T1
202
216
Env. In
I_{SW}
Delay
Network
41
V_{GG}. In
Subtracting
Network
210
2
3
RF. Out
Sinking
Only
RF. In
RFT
204
214

FIG 3

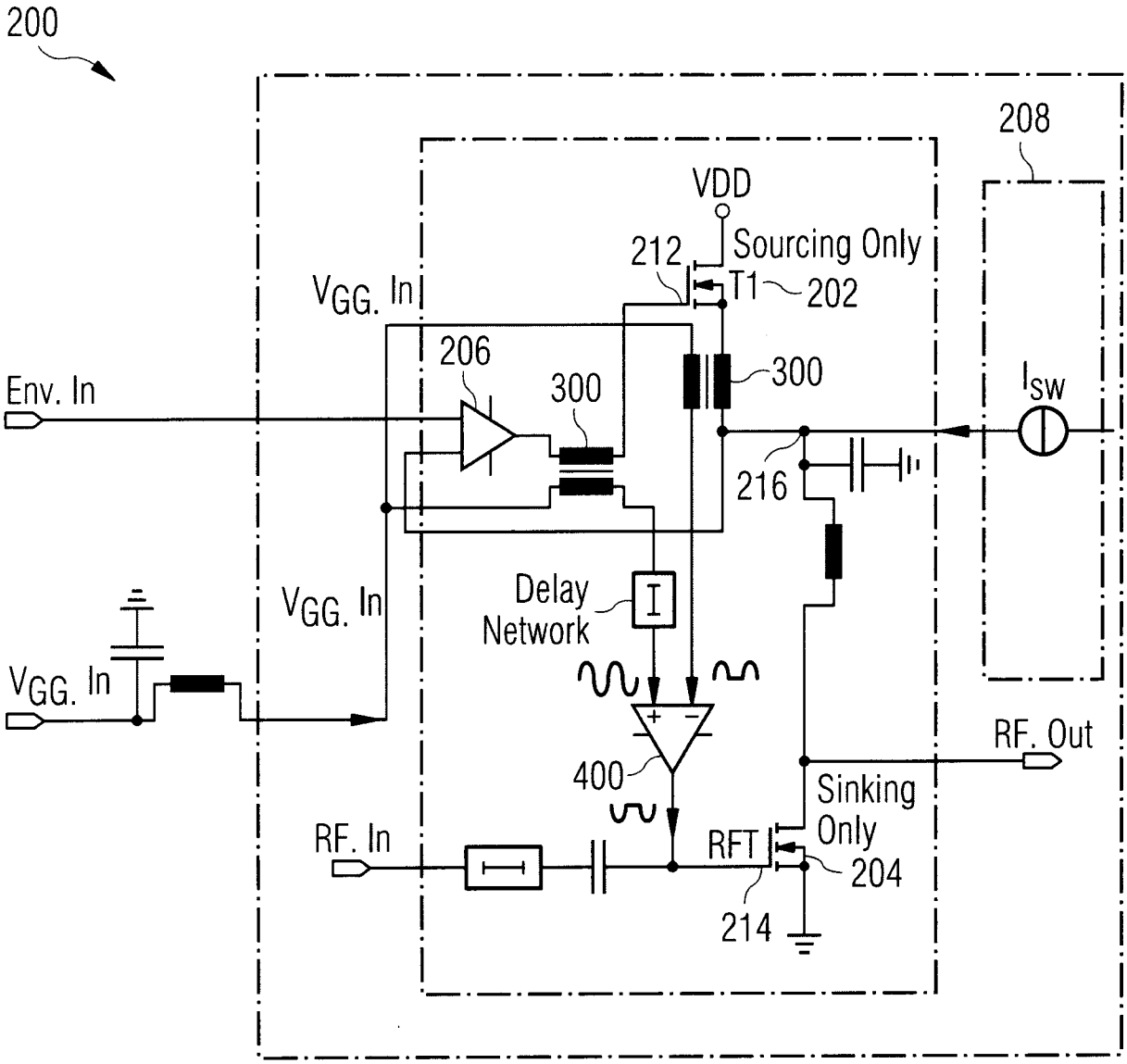
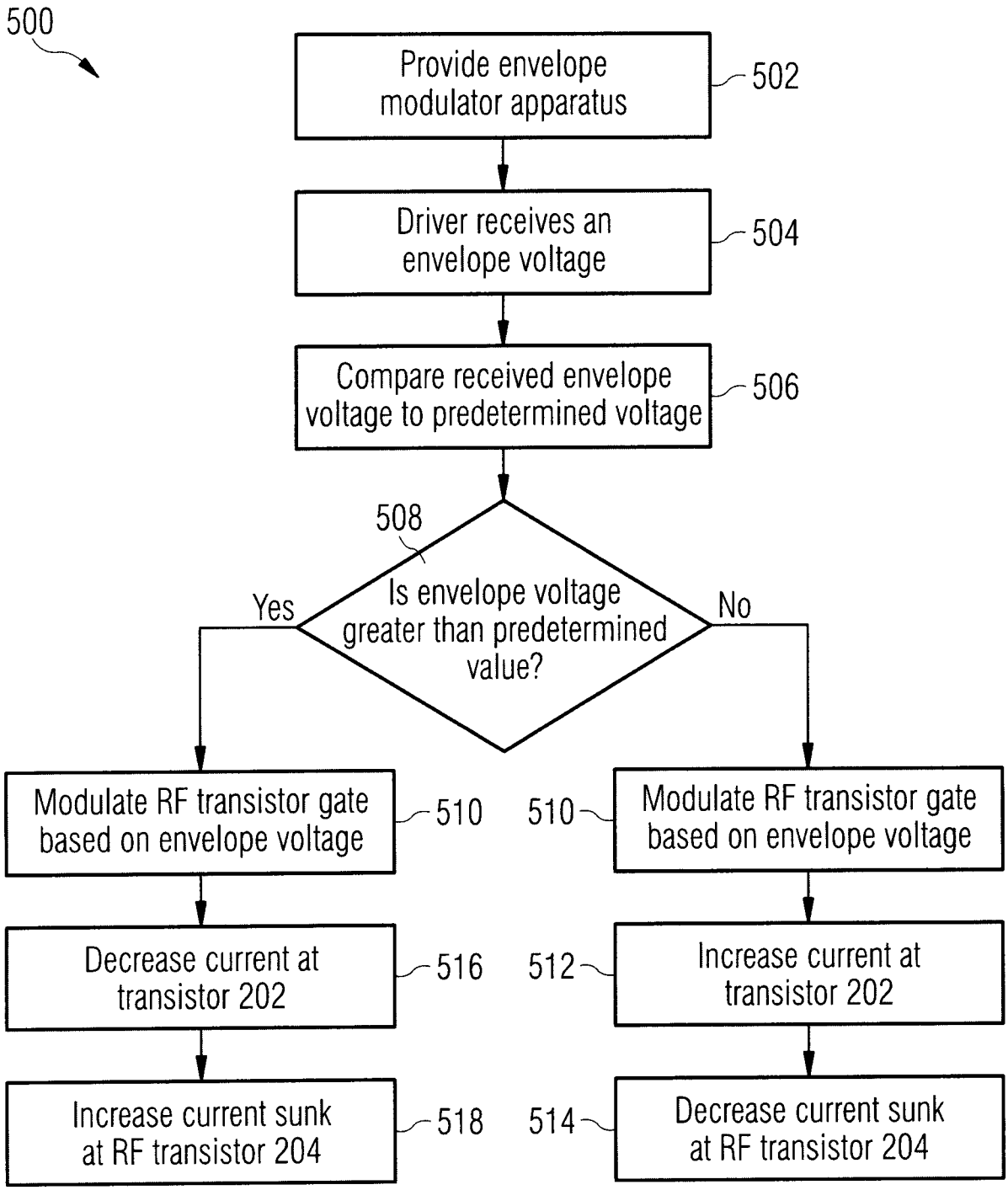

200
208
VDD
212
Sourcing Only
T1
202
VGG. In
206
300
300
Env. In
Isw
216
VGG. In
Delay
Network
VGG. In
400
RF. Out
Sinking
Only
RF. In
RFT
204
214

FIG 4


500
Provide envelope modulator apparatus
502
Driver receives an envelope voltage
504
Compare received envelope voltage to predetermined voltage
506
508
Is envelope voltage greater than predetermined value?
Yes
No
Modulate RF transistor gate based on envelope voltage
510
Decrease current at transistor 202
516
Increase current sunk at RF transistor 204
518
510
Modulate RF transistor gate based on envelope voltage
512
Increase current at transistor 202
514
Decrease current sunk at RF transistor 204

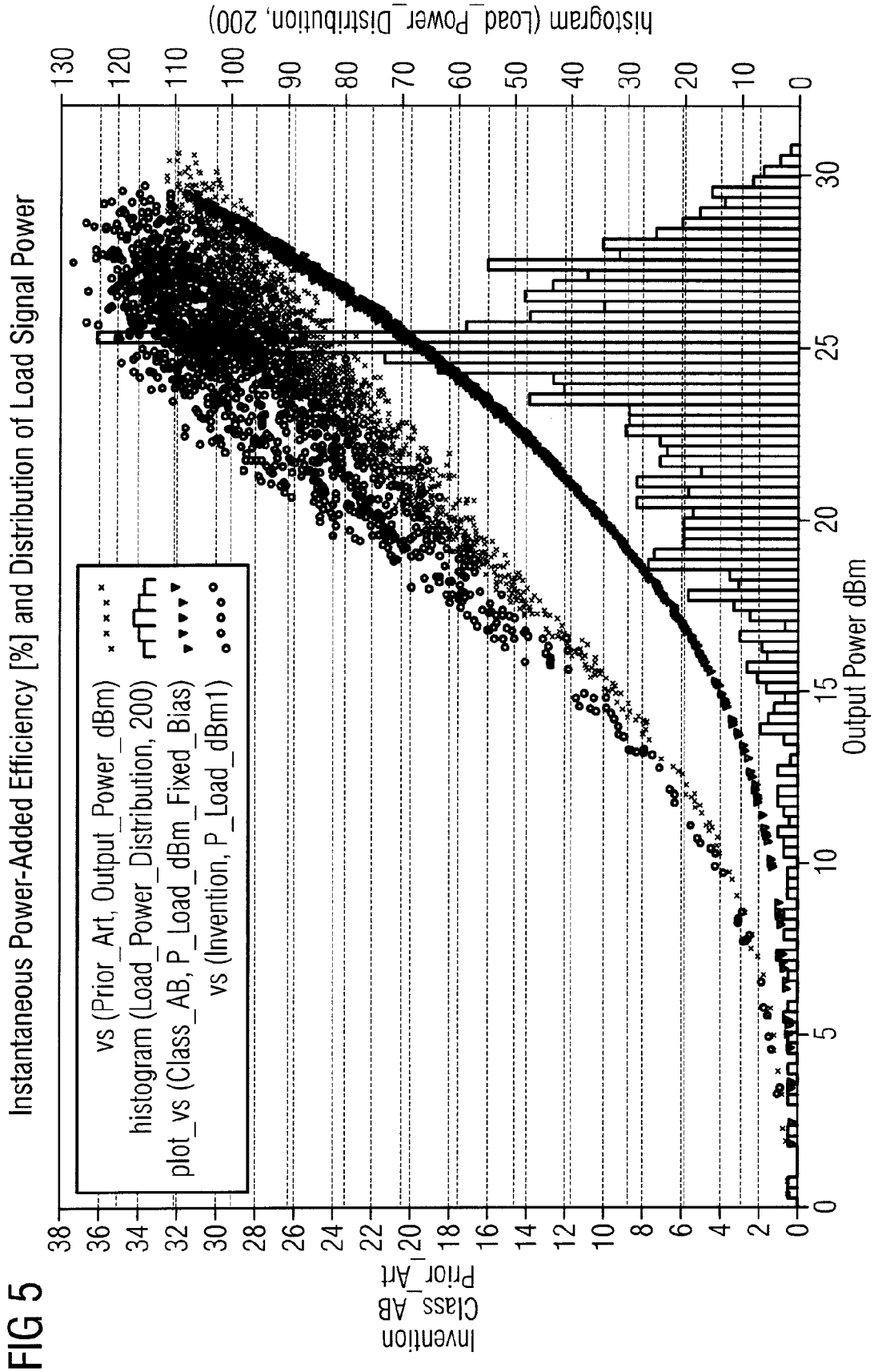

Instantaneous Power-Added Efficiency [%] and Distribution of Load Signal Power
vs (Prior_Art, Output_Power_dBm)
histogram (Load_Power_Distribution, 200)
plot_vs (Class_AB, P_Load_dBm_Fixed_Bias)
vs (Invention, P_Load_dBm1)
Invention Class_AB Prior_Art
Output Power dBm
histogram (Load_Power_Distribution, 200)

FIG 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2013/080205

A. CLASSIFICATION OF SUBJECT MATTER

H03F 1/32 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03F 1/-; 3/-; H04B 1/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS,CNTXT,VEN,INTERNET: envelope, modulat+, track+, ET, RF, radio, frequency, transistor, amplifier, bias+, current, absorb+, sink+, sunk+, nokia, siemens, subtract+,network,driver,switcher

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012326783A1 (（QUALCOMM INC）) 27 December 2012 (2012-12-27) see description, paragraphs [0018] to [0025] and [0030] to [0035], and figures 1 and 3	1, 2, 4, 9-11
Y	US 2012269240A1 (（SKYWORKS SOLUTIONS INC）) 25 October 2012 (2012-10-25) see description, paragraphs [0076] to [0079] and figures 5 and 6	1, 2, 4, 9-11
A	US 2012062323A1 (（AGENCE SPATIALE EURO）) 15 March 2012 (2012-03-15) see the whole document	1-20
A	US 2006178119A1 (（NOKIA CORP）) 10 August 2006 (2006-08-10) see the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 April 2014	**06 May 2014**

Name and mailing address of the ISA/	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA(ISA/CN) **6,Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China** **100088 China**	**WANG,Yue**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)01062089109**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2013/080205

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US 2012326783A1	27 December 2012	WO 2012178138A1	27 December 2012
		KR 2014026626A	05 March 2014
US 2012269240A1	25 October 2012	WO 2012148918A3	14 March 2013
		WO 2012148918A2	01 November 2012
		KR 2014026510A	05 March 2014
US 2012062323A1	15 March 2012	US 8669811B2	11 March 2014
		EP 2432118A1	21 March 2012
		CN 102403964A	04 April 2012
		EP 2432118B1	26 December 2012
US 2006178119A1	10 August 2006	US 7400865B2	15 July 2008
		KR 20070094980A	27 September 2007
		EP 1847013A4	03 September 2008
		KR 100939728B1	29 January 2010
		WO 2006085177A2	17 August 2006
		EP 1847013A2	24 October 2007
		WO 2006085177A3	11 January 2007
		CN 101147319A	19 March 2008
		CN 101147319B	19 May 2010
		WO 2006085177A8	26 October 2006