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(54) **Control circuit**

Steuerschaltung

Circuit de commande

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(56) References cited:
US-A- 4 335 360

- **ANDERSEN M A E: "MOS GATE DRIVER CIRCUIT WITH EXTREMELY HIGH GALVANIC ISOLATION" EPE '95: 6TH. EUROPEAN CONFERENCE ON POWER ELECTRONICS AND APPLICATIONS. SEVILLA, SEPT. 19 - 21, 1995, EUROPEAN CONFERENCE ON POWER ELECTRONICS AND APPLICATIONS, BRUSSELS, EPE ASSOCIATION, B, vol. & 1 CONF. 6, 19 September 1995 (1995-09-19), pages 1747-1751, XP000537614**
- **RUDY SEVERNS, JACK ARMIJOS: "MOSPOWER Applications Handbook" 1984 , SILICONIX INC. , SANTA CLARA, CALIFORNIA XP002235466 ISBN: 0-930519-00-0 * page 5-13; figure 7 ***

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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a control circuit for controlling a power semiconductor, the control circuit comprising a gate driver comprising a control input, auxiliary voltage inputs and an output.

[0002] For some time, gate drivers equipped with optical isolation have been commercially available that can be used for controlling at most an approximately 100-ampere power semiconductor, such as an IGBT or FET. The reason for the limited power semiconductor rating is the limited current output capacity of a gate driver, which makes it impossible to control high-current power semiconductors in a reliable manner. Because of the above-mentioned problem, using such a gate driver necessitates a separate amplifier stage by means of which the current feeding capacity can be made to satisfy the needs of larger power semiconductors as well.

[0003] A control circuit according to the preamble portion of claim 1 is disclosed in the article "MOS gate driver circuit with extremely high galvanic isolation" written by Michael A.E. Andersen from the. Technical University of Denmark 6TH. EUROPEAN CONFERENCE ON POWER ELECTRONICS AND APPLICATIONS. SEVILLA, SEPT. 19 - 21, 1995.

BRIEF DESCRIPTION OF THE INVENTION

[0004] An object of the present invention is to provide a control circuit avoiding the disadvantages mentioned above, also enabling high-current power semiconductors to be controlled in a reliable manner while employing a simple circuit. This object is achieved by a control circuit in accordance with the invention, the control circuit being characterized in that the control circuit further comprises a first resistance (R1) whose first pole is connected to the positive auxiliary voltage input (UA+) of the gate driver (A1) and whose second pole is connected to the positive input pole (Udc+) of the control circuit, the positive auxiliary voltage input (UA+) being arranged to control the first semiconductor switch (S1);
a second resistance (R2) whose first pole is connected to the negative auxiliary voltage input (UA-) of the gate driver (A1) and whose second pole is connected to the negative input pole (Udc-) of the control circuit, the negative auxiliary voltage input (UA-) being arranged to control the second semiconductor switch;
and in that the anode of the first zener diode (Z1) and the cathode of the second zener diode (Z2) are connected to the output (UAO) of the gate driver (A1).

[0005] The control circuit in accordance with the invention is based on the idea that the current output capacity of a gate driver is increased by utilizing a simple circuit. The control circuit comprises semiconductor switches that form an output, which is cophasal with the output of the gate driver. Current obtained via the semiconductor switches at the output is significantly higher than current from a mere gate driver output. Owing to the fact that the outputs are cophasal, the control circuit is unnoticeable to other components possibly connected thereto; hence, when designing other parts or sub-entities belonging to the same operational entity, it is unnecessary to take into account the addition of auxiliary components belonging to the control circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The invention is now described in closer detail in connection with the preferred embodiments with reference to the accompanying drawing, in which

[0007] Figure **1** shows a control circuit in accordance with a preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0008] According to Figure 1, a control circuit in accordance with the invention comprises a gate driver A1. The gate driver A1 is an optically isolated gate driver, whereby a control input Ctrl is electrically isolated from other outputs or inputs of the gate driver. Consequently, the potential of a circuit providing the control input can vary with respect to the potential of the control circuit. The gate driver A1 further comprises a positive UA+ and a negative UA-auxiliary voltage input and an output UAO. Conventionally used, the output of the gate driver is connected to a control electrode of a power semiconductor to be controlled. Depending on the control input, a voltage connected either to the positive or the negative auxiliary voltage input is then led to the control electrode.

[0009] The control circuit of the invention further comprises a first and a second resistance R1, R2 connected to the positive and the negative auxiliary voltage input of the gate driver. A first pole of the first resistance R1 is connected to the positive input UA+ of the gate driver A1, while a second pole forms a positive input pole Udc+ of the control circuit. In a corresponding way, a first pole of the second resistance is connected to the negative input UA- of the gate driver, while a second pole forms a negative input pole of the control circuit.

[0010] The control circuit further comprises a first and a second zener diode Z1, Z2. The first zener diode Z1 is connected between the output UAO of the gate driver A1 and the positive input pole Udc+ of the control circuit such that the cathode of the zener diode Z1 is connected to the positive input pole Udc+. In a corresponding manner, the second zener diode Z2 is connected between the output UAO of the gate driver A1 and the negative input pole Udc- of the control circuit. The second zener diode is connected in such a manner that its anode is connected to the negative input pole Udc-. Hence, the zener diodes are coupled in series between the positive and the negative input poles, a point between the zener diodes further being connected to the output of the gate driver.

[0011] In the manner shown by Figure 1, the control

circuit in accordance with a preferred embodiment of the invention further comprises a capacitor C1 connected between the positive and the negative auxiliary voltage inputs of the gate driver.

[0012] The control circuit of the invention comprises a first and a second semiconductor switches S1, S2 comprising a control electrode G and main electrodes S, D. The control electrode refers to the electrode by which the semiconductor component to be controlled is controlled, and the main electrodes refer to those electrodes of the component that, responsive to the control of the control electrode, carry out the control command. In the description of the invention, FET transistors are used as the semiconductor switches by way of example, but the semiconductor switch can be any other component appropriate for the purpose. When the semiconductor switch is an FET transistor, the control electrode is called a gate and the main electrodes are called a source S and a drain D. In the manner shown in Figure 1, a first main electrode S of the first semiconductor switch is connected to the positive input pole of the control circuit, a second main electrode D forming an output Output of the control circuit. Correspondingly, a first main electrode S of the second semiconductor S2 is connected to the negative input point Udc- of the control circuit, and a second electrode D is connected to the control circuit's output Output, which, at the same time, is the second electrode D of the first semiconductor switch.

[0013] In accordance with a preferred embodiment of the invention, the control circuit further comprises two parallel connections 1, 2 of a diode and a resistance connected between the control electrodes G, i.e. the gates, of the first and the second semiconductor switches and the auxiliary voltage inputs UA+, UA- of the gate driver. The first parallel connection 1 of a diode D1 and a resistance R3 is connected between the gate of the first semiconductor switch and the positive auxiliary voltage input UA+ of the gate driver in such a manner that the anode of the diode D1 is connected to the auxiliary voltage input UA+. The second parallel connection 2 of a diode D2 and a resistance R4 is connected between the gate of the second semiconductor switch and the negative auxiliary voltage input UA- of the gate driver in such a manner that the anode of the diode D2 is connected to the gate of the semiconductor switch S2.

[0014] The control circuit of the invention generates output voltages that are cophasal with respect to control signals supplied to the control input. The output voltages are obtained from the input voltages connected to the positive and the negative input poles Udc+, Udc-. Typically, the gate driver comprises two current paths, each of which can in turn be directed to be conducting. The output of the gate driver is then connected either to the positive, or, alternatively, to the negative auxiliary voltage input. When the higher voltage path of the gate driver is controlled to be conducting, in other words when the output of the gate driver and the positive auxiliary voltage input are electrically interconnected by the internal switch parts of the gate driver, current starts flowing through the gate driver A1. The current starts advancing from the positive input pole Udc+ whereto a positive input voltage, typically of approximately 15 volts, is connected, further passing through the first resistance R1, the higher current path of the gate driver A1 and the second zener diode, reaching the negative input pole Udc- whereto a voltage of approximately -7 volts is typically connected. When voltages are as described above, the potential difference between the positive and the negative poles is approximately 22 volts.

[0015] When current follows the above-described route it causes certain voltage losses. A current flow requires a threshold voltage of the zener diode Z2 to be lower than the overall voltage applied over the zener diode. When current flows through the zener diode, a voltage corresponding to the threshold voltage remains over it. In the exemplary case, the threshold voltage of the zener diode Z2 is 13 volts. Hence, when current flows through the zener diode Z2, the voltage of its anode increases by 13 volts, i.e. to a voltage of +6 volts. When current flows through the gate driver, a voltage loss of approximately 2 volts also takes place, as a result of which the positive auxiliary voltage input UA+ of the gate driver has a voltage of +8 volts.

[0016] In the exemplary design, the resistances R1, R2 connected to the auxiliary voltage inputs of the gate driver A1 are approximately 400 ohms, whereby the idle current of the circuit causes a voltage loss approximately of 1 volt in the resistances. The idle current refers to a current which flows via an uncontrolled circuit of the gate driver. Hence, in the above-described case, the potential of the negative auxiliary voltage input of the gate driver is approximately -6 volts.

[0017] In the control circuit in accordance with the invention, the positive auxiliary voltage input UA+ of the gate driver A1 is connected to the gate G of the first semiconductor switch S1 via the parallel connection 1 of the first diode D1 and the resistance R3. According to the preferred embodiment of the invention, the first semiconductor switch S1 is a p-channel FET transistor, and the second semiconductor switch S2 is an n-channel FET transistor. When the semiconductor switch S1 is a p-channel FET transistor, it can be controlled into a conducting state by taking the gate G of the switch to a negative potential with respect to its main electrode S. In the above-described case, this is exactly what happens, since the potential of the gate G follows the potential of the positive auxiliary voltage input of the gate driver and the potential of the main electrode S is connected to a positive input voltage, which is 15 volts in the exemplary design, directly connected to the positive input pole of the control circuit. Hence, the semiconductor switch S1 is in the conducting state.

[0018] The semiconductor switch S2 is preferably of the n-channel FET transistor type, in which case rendering it into the conducting state requires a considerable positive gate voltage with respect to the main electrode

S. If the gate driver is controlled as described above, the negative auxiliary voltage input UA- of the gate driver has the potential of -6 volts, the gate of the switch S2 also following this potential. The main electrode S of the switch S2 is connected to a negative input voltage connected to the negative input pole, whereby the voltage between the gate and the main electrode S is approximately 1 volt, which is not sufficient for the switch S2 to be switched on. It is thus obvious that while the higher semiconductor switch S1 conducts, the lower one S2 should be in a non-conducting state.

[0019] A purpose of the parallel connections 1, 2 of a diode and a resistance connected to the gates of the semiconductor switches S1, S2 is to delay a switch to be switched on appropriately such that a switch to be switched off has sufficiently time to be reliably transferred to a blocking state. Hence, the polarities of the diodes D1, D2 allow current of a direction necessary for switching off the semiconductor switches to pass through the diodes. Currents necessary for switch-off thus flow via the diodes, but currents necessary for switching on the switches must flow via the resistances R3, R4. The capacitor C1 serves to operate as a filtering capacitor and energy supply of the gate driver A1 by means of which the semiconductor switches are quickly switched off.

[0020] When the negative voltage connected to the negative input pole Udc- is to be provided to the output Output of the gate driver and, simultaneously, of the control circuit, the lower current path of the gate driver A1, i.e. the current path from the negative auxiliary voltage input UA- to the output UAO of the gate driver, should be directed to be conducting by using the control input Ctrl. When the lower current path is conducting, owing to the potential difference between the positive and the negative input poles Udc+, Udc-, current starts flowing via a route formed by the first zener diode Z1, the lower current path of the gate driver and the second resistance R2. In the exemplary design, the threshold voltage of the zener diode Z1 is 15 volts, in which case when current flows through the zener diode, the voltage from its cathode to the anode drops by a corresponding voltage to the threshold voltage, i.e. 15 volts. Owing to the drop in voltage, the potential of the output UAO of the gate driver is 0 volts. On the lower current path of the gate driver in the exemplary design, owing to the characteristics of the gate driver, no significant current loss occurs, thereby the potential of the negative auxiliary voltage input UA- of the gate driver also being approximately 0 volts. Since the potential of said auxiliary voltage input is also transferred to the gate G of the semiconductor switch S2, and since the main electrode S of the semiconductor switch has a voltage of -7 volts connected to the negative input pole Udc- of the control circuit, the switch S2 is transferred to the conducting state, remaining therein until otherwise directed. When the switch S2 is conducting, the negative input voltage, which is -7 volts in the exemplary design, connected to the negative input pole Udc- is obtained to the output Output of the control circuit.

[0021] Simultaneously with the lower switch component S2 conducting, the higher switch component is in the blocking state. The blocking state is reached since the voltage drop caused by the idle current of the gate driver in the first resistance R1 is approximately 1 volt, whereby a voltage of approximately -1 volt is applied over the gate of the switch S1 and the main electrode S, this voltage retaining the component in the blocking state.

[0022] The control circuit of the invention can be utilized for example for reliably controlling inverters or power semiconductors of other such devices comprising high-current semiconductors. The circuit of the invention enables the positive and negative voltage necessary for controlling a power semiconductor, such as an IGBT or FET, to be generated in a reliable and cost-efficient manner.

Claims

1. A control circuit for controlling a power semiconductor, the control circuit comprising a gate driver (A1) comprising

a control input (ctrl), auxiliary voltage inputs (UA+, UA-) and an output (UAO), a first semiconductor switch (S1) comprising a control electrode (G) and main electrodes (S, D), a first main electrode (S) forming a positive input pole (Udc+) of the control circuit and a second main electrode (D) forming an output (Output) of the control circuit;

a second semiconductor switch (S2) comprising a control electrode (G) and main electrodes (S, D), a first main electrode (S) forming a negative input pole (Udc-) of the control circuit and a second main electrode (D) being connected to the output (Output) of the control circuit;

a first zener diode (Z1) whose cathode is connected to the positive input pole (Udc+) of the control circuit;

a second zener diode (Z2) whose cathode is connected to the anode of the first zener diode (Z1) and whose anode is connected to the negative input pole (Udc-) of the control circuit, **characterized in that** the control circuit further comprises

a first resistance (R1) whose first pole is connected to the positive auxiliary voltage input (UA+) of the gate driver (A1) and whose second pole is connected to the positive input pole (Udc+) of the control circuit, the positive auxiliary voltage input (UA+) being arranged to control the first semiconductor switch (S1);

a second resistance (R2) whose first pole is connected to the negative auxiliary voltage input (UA-) of the gate driver (A1) and whose second pole is connected to the negative input pole (Udc-) of the control circuit, the negative auxiliary voltage input (UA-) being arranged to control the second semiconductor switch; and **in that** the anode of the first zener diode (Z1) and the cathode of the second zener diode (Z2) are connected to the output (UAO) of the gate driver (A1).

2. A control circuit as claimed in claim 1, **characterized in that** the control circuit further comprises
a capacitor (C1) connected between the auxiliary voltage inputs (UA+, UA-) of the gate driver (A1),
a parallel connection (1) of a third resistance (R3) and a first diode (D1), the parallel connection (1) being connected between the control electrode (G) of the first semiconductor switch (S1) and the positive auxiliary voltage input (UA+) of the gate driver (A1) such that the cathode of the diode (D1) is connected to the control electrode (G); and
a parallel connection (2) of a fourth resistance (R4) and a second diode (D2), the parallel connection (2) being connected between the control electrode (G) of the second semiconductor switch (S2) and the negative auxiliary voltage input (UA-) of the gate driver (A1) such that the anode of the diode (D2) is connected to the control electrode (G).

3. A control circuit as claimed in claim 1 or 2, **characterized in that** the first semiconductor switch (S1) is a p-channel FET transistor and the second semiconductor switch (S2) is an n-channel FET transistor.

Patentansprüche

1. Steuerschaltung zur Steuerung eines Leistungshalbfeiters, wobei die Steuerschaltung umfasst:

- einen Gate-Treiber (A1) mit einem Steuereingang (ctrl), Hilfsspannungseingängen (UA+, UA-) und einem Ausgang (UAO),
- einen ersten Halbleiterschalter (S1) mit einer Steuerelektrode (G) und Hauptelektroden (S, D), wobei eine erste Hauptelektrode (S) einen positiven Eingangspol (Udc+) der Steuerschaltung bildet und eine zweite Hauptelektrode (D) einen Ausgang (Ausgang) der Steuerschaltung bildet,
- einen zweiten Halbleiterschalter (S2) mit einer Steuerelektrode (G) und Hauptelektroden (S, D), wobei eine erste Hauptelektrode (S) einen negativen Eingangspol (Udc-) der Steuerschaltung bildet und eine zweite Hauptelektrode (D) mit dem Ausgang (Ausgang) der Steuerschaltung verbunden ist,
- eine erste Zener-Diode (Z1), deren Kathode mit dem positiven Eingangspol (Udc+) der Steuerschaltung verbunden ist,
- eine zweite Zener-Diode (Z2), deren Kathode mit der Anode der ersten Zener-Diode (Z1) verbunden ist und deren Anode mit dem negativen Eingangspol (Udc-) der Steuerschaltung verbunden ist,

dadurch gekennzeichnet, dass die Steuerschaltung ferner umfasst:

- einen ersten Widerstand (R1), dessen erster Pol mit dem positiven Hilfsspannungseingang (UA+) des Gate-Treibers (A1) verbunden ist und dessen zweiter Pol mit dem positiven Eingangspol (Udc+) der Steuerschaltung verbunden ist, wobei der positive Hilfsspannungseingang (UA+) zur Steuerung des ersten Halbleiterschalters (S1) ausgelegt ist,
- einen zweiten Widerstand (R2), dessen erster Pol mit dem negativen Hilfsspannungseingang (UA-) des Gate-Treibers (A1) verbunden ist und dessen zweiter Pol mit dem negativen Eingangspol (Udc-) der Steuerschaltung verbunden ist, wobei der negative Hilfsspannungseingang (UA-) zur Steuerung des zweiten Halbleiterschalters ausgelegt ist,

und dass die Anode der ersten Zener-Diode (Z1) und die Kathode der zweiten Zener-Diode (Z2) mit dem Ausgang (UAO) des Gate-Treibers (A1) verbunden sind.

2. Steuerschaltung nach Anspruch 1, **dadurch gekennzeichnet, dass** die Steuerschaltung ferner umfasst:

- einen zwischen die Hilfsspannungseingänge (UA+, UA-) des Gate-Treibers (A1) geschalteten Kondensator (C1),
- eine Parallelschaltung (1) eines dritten Widerstands (R3) und einer ersten Diode (D1), wobei die Parallelschaltung (1) zwischen die Steuerelektrode (G) des ersten Halbleiterschalters (S1) und den positiven Hilfsspannungseingang (UA+) des Gate-Treibers (A1) derart geschaltet ist, dass die Kathode der Diode (D1) mit der Steuerelektrode (G) verbunden ist, sowie
- eine Parallelschaltung (2) eines vierten Widerstands (R4) und einer zweiten Diode (D2), wobei die Parallelschaltung (2) zwischen die Steuerelektrode (G) des zweiten Halbleiterschalters (S2) und den negativen Hilfsspannungseingang (UA-) des Gate-Treibers (A1) derart geschaltet ist, dass die Anode der Diode (D2) mit der Steuerelektrode (G) verbunden ist.

3. Steuerschaltung nach Anspruch 1 oder 2, **dadurch gekennzeichnet, dass** der erste Halbleiterschalter (S1) ein p-Kanal FET-Transistor ist und der zweite Halbleiterschalter (S2) ein n-Kanal FET-Transistor ist.

Revendications

1. Circuit de commande destiné à commander un semiconducteur de puissance, le circuit de commande comprenant un pilote à grille (A1) comprenant

une entrée de commande (ctrl), des entrées de tension auxiliaires (UA+, UA-) et une sortie (UAO),
un premier commutateur à semi-conducteur (S1) comprenant une électrode de commande (G) et des électrodes principales (S, D), une première électrode principale (S) formant une dent d'entrée positive (Udc+) du circuit de commande et une seconde électrode principale (D) formant une sortie (Sortie) du circuit de commande ;
un second commutateur à semi-conducteur (S2) comprenant une électrode de commande (G) et des électrodes principales (S, D), une première électrode principale (S) formant une dent d'entrée négative (Udc-) du circuit de commande et une seconde électrode principale (D) étant connectée à la sortie (Sortie) du circuit de commande ;
une première diode Zener (Z1) dont la cathode est connectée à la dent d'entrée positive (Udc+) du circuit de commande ;
une seconde diode Zener (Z2) dont la cathode est connectée à l'anode de la première diode Zener (Z1) et dont l'anode est connectée à la dent d'entrée négative (Udc-) du circuit de commande, **caractérisé en ce que** le circuit de commande comprend en outre
une première résistance (R1) dont la première dent est connectée à l'entrée de tension auxiliaire positive (UA+) du pilote à grille (A1) et dont la seconde dent est connectée à la dent d'entrée positive (Udc+) du circuit de commande, l'entrée de tension auxiliaire positive (UA+) étant agencée pour commander le premier commutateur à semi-conducteur (S1) ;
une seconde résistance (R2) dont la première dent est connectée à l'entrée de tension auxiliaire négative (UA-) du pilote à grille (A1) et dont la seconde dent est connectée à la dent d'entrée négative (Udc-) du circuit de commande, l'entrée de tension auxiliaire négative (UA-) étant agencée pour commander le second commutateur à semi-conducteur ;
et **en ce que** l'anode de la première diode Zener (Z1) et la cathode de la seconde diode Zener (Z2) sont connectées à la sortie (UAO) du pilote à grille (A1).

2. Circuit de commande selon la revendication 1, **caractérisé en ce que** le circuit de commande comprend en outre
un condensateur (C1) connecté entre les entrées de tension auxiliaires (UA+, UA-) du pilote à grille (A1),
une connexion parallèle (1) d'une troisième résistance (R3) et d'une première diode (D1), la connexion parallèle (1) étant connectée entre l'électrode de commande (G) du premier commutateur à semi-conducteur (S1) et l'entrée de tension auxiliaire positive (UA+) du pilote à grille (A1) de telle sorte que la cathode de la diode (D1) est connectée à l'électrode de commande (G) ; et
une connexion parallèle (2) d'une quatrième résistance (R4) et d'une seconde diode (D2), la connexion parallèle (2) étant connectée entre l'électrode de commande (G) du second commutateur à semi-conducteur (S2) et l'entrée de tension auxiliaire négative (UA-) du pilote à grille (A1) de telle sorte que l'anode de la diode (D2) est connectée à l'électrode de commande (G).

3. Circuit de commande selon la revendication 1 ou 2, **caractérisé en ce que** le premier commutateur à semi-conducteur (S1) est un transistor à effet de champ (FET) à canal p et le second commutateur à semi-conducteur (S2) est un transistor FET à canal n.

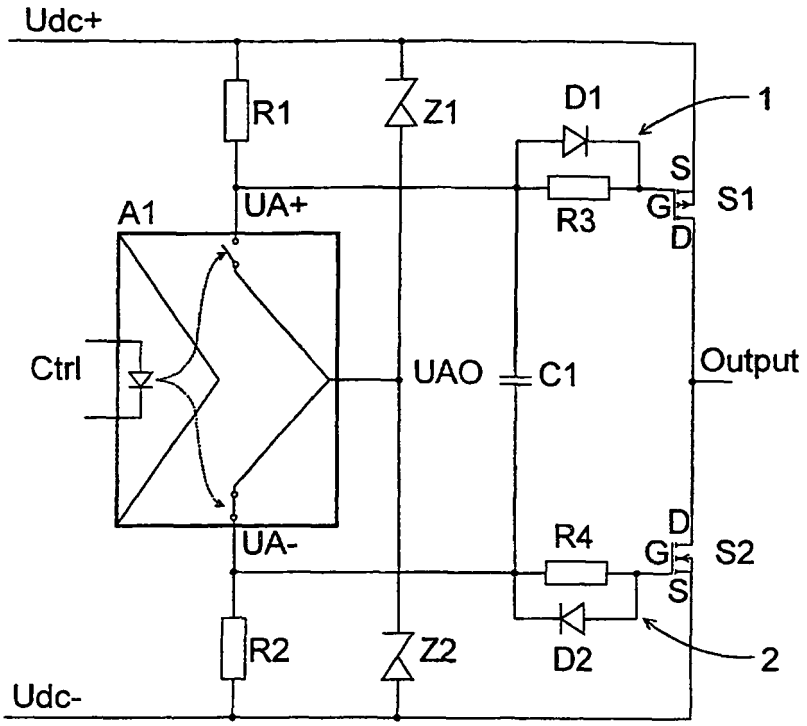

Udc+
R1
Z1
D1
1
S
S1
G
D
R3
A1
UA+
Ctrl
UAO
C1
Output
UA-
D
R4
G
S2
S
R2
Z2
D2
2
Udc-

FIG.1