(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 November 2001 (08.11.2001)

PCT

(10) International Publication Number
WO 01/84625 A1

(51) International Patent Classification⁷: H01L 21/762, 21/8247

(21) International Application Number: PCT/US01/10922

(22) International Filing Date: 3 April 2001 (03.04.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/563,179 2 May 2000 (02.05.2000) US

(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: CHAN, Maria, C.; 3427 San Saba Drive, San Jose, CA 95148 (US). FANG, Hao; 7719 Carriage Circle, Cupertino, CA 95014 (US). CHANG, Mark, S.; 1881 Farndon Avenue, Los Altos, CA 94024 (US). TEMPLETON, Michael; 80 Palmer Lane, Atherton, CA 94027 (US).

(74) Agent: RODDY, Richard, J.; Advanced Micro Devices, Inc., Mail Stop 68, One AMD Place, Sunnyvale, CA 94088-3453 (US).

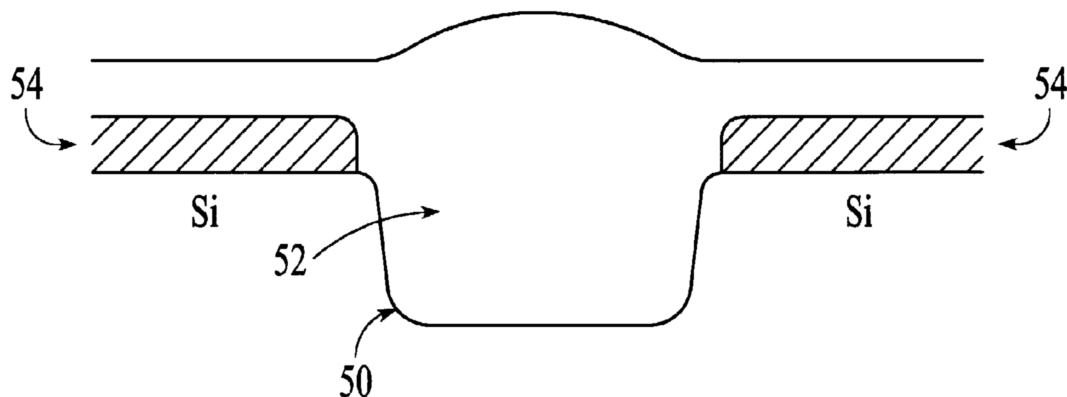
(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

[Continued on next page]

(54) **Title:** FLASH MEMORY ARRAY AND A METHOD AND SYSTEM OF FABRICATION THEREOF



(57) **Abstract:** In a first aspect of the present invention, a flash memory array is disclosed. The flash memory array comprises a substrate comprising active regions, wherein the active regions are defined by a layer of nitride, the layer of nitride including a top surface. The flash memory array further comprises shallow trenches in the substrate, each of the shallow trenches including a layer of oxide, the layer of oxide having a top surface, wherein the top surface of the layer of oxide and the top surface of the layer of nitride are on substantially the same plane and channel area wherein the occurrences of poly 1 stringers in the channel areas is substantially reduced. In a second aspect of the present invention, a method and system for fabricating a flash memory array is disclosed. The method comprises the steps of providing a layer of nitride over a substrate, forming trenches in the substrate and then growing a layer of oxide in the trenches. Finally, the layer of oxide is polished back. Through the use of the preferred embodiment of the present invention, a shallow trench isolation process is implemented as opposed to LOCOS process, thereby reducing the occurrence of poly 1 stringers in the channel area. Accordingly, the occurrence of unwanted electrical shorting paths between the adjacent regions is substantially reduced.

WO 01/84625 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

FLASH MEMORY ARRAY AND A METHOD AND SYSTEM OF FABRICATION THEREOF

TECHNICAL FIELD

The present invention relates generally to flash memory arrays and more specifically to a method and system for fabricating a flash memory array.

BACKGROUND ART

Semiconductor manufacturers have increasingly turned to high density flash memory arrays in their integrated circuit design schemes. To achieve a high density integrated circuit, the transistors must be as small as possible. Typically, these high density flash memory integrated circuits utilize NAND-type gates as opposed to NOR-type gates since NAND gates have a considerably higher density than NOR gates. Smaller transistors allow more transistors to be placed on a single substrate, thereby allowing relatively large circuit systems to be incorporated on a single, relatively small die area.

When fabricating silicon integrated circuits, devices built onto the silicon must be isolated from one another so that these devices can be subsequently interconnected to create specific circuit configurations. From this perspective, it can be seen that isolation technology is one of the critical aspects of fabricating integrated circuits.

During the manufacturing of integrated circuit devices, the devices are isolated from one another through a combination of a thick field oxide (FOX) and channel doping. For advanced deep submicronmeter and high density flash memory technology, a duel field oxidation process, or LOCOS (LOCal Oxidation of Silicon), is usually required to optimize transistor isolation.

Figure 1 is a flow chart illustrating the conventional process steps required to fabricate a NAND flash memory array. Also shown is a series of cross sectional views (Figures 1(a-g)) of a substrate showing the resulting structure.

The LOCOS process begins by thermally growing a layer of oxide on the surface of bare silicon, via step 10. Next, a nitride layer is provided over the layer of oxide, via step 12. This layer of nitride has a typical thickness in the range of around 1700 Angstroms. Then, the nitride layer is etched down to the oxide layer to define the active regions, via step 14. Next, using the nitride layer as a mask, a thin field oxide region (FOX) is grown between active regions using a thermal oxidation process, via step 16. Typically, the resulting step height 22 (see Figure 1(d)) of the oxide region is between 1500 and 2500 Angstroms. Next, the nitride layer is stripped, via step 18. A layer of type-l polysilicon (poly1) is then deposited, via step 20. Next, the poly1 is etched down to the oxide region to define the channel area, via step 22.

When utilizing this process, channel misalignments have a tendency to occur. This is due primarily to the smaller spacings of the high density flash memory arrays. A chamel misalignment occurs when the channel area is not defined directly in the middle of the FOX region. Figure 2(a) illustrates a properly aligned channel area 24 and Figure 2(b) illustrates a misaligned channel area 24'.

The etching process in step 22 is anisotropic, meaning that it removes material directionally to a predetermined depth. But due to the size of the step height of the FOX regions, along with the occurrences of channel misalignments, the etching process sometimes fails to remove all the poly1 from the channel region, leaving a residue material which is called a poly1 stringer. Figures 3(a-c) show the formation of poly1 stringers after the poly1 etch. The presence of poly1 stringers can provide a contact between the two adjacent regions and failure to remove this material can lead to unwanted electrical shorting paths between the adjacent regions.

Utilizing the NOR technology, the poly1 stringers are not a problem because steps that are implemented later in the NOR process (i.e. dipping steps, oxidation steps), effectively eliminate the poly1 stringers. However, as previously mentioned, the NAND process is utilized for high density flash memory integrated circuits since NAND gates have a considerably higher density than NOR gates. Consequently, the NAND process does not incorporate later steps to effectively eliminate the poly1 stringers.

Accordingly, what is needed is a method for reducing the occurrence of poly1 stringers in the fabrication of flash memory arrays. The present invention addresses such a need.

DISCLOSURE OF THE INVENTION

In a first aspect of the present invention, a flash memory array is disclosed. The flash memory array comprises a substrate comprising active regions, wherein the active regions are defined by a layer of nitride, the layer of nitride including a top surface. The flash memory array further comprises shallow trenches in the substrate, each of the shallow trenches including a layer of oxide, the layer of oxide having a top surface, wherein the top surface of the layer of oxide and the top surface of the layer of nitride are on substantially the same plane and channel areas wherein the occurrences of poly1 stringers in the channel areas is substantially reduced.

In a second aspect of the present invention, a method and system for fabricating a flash memory array is disclosed. The method comprises the steps of providing a layer of nitride over a substrate, forming trenches in the substrate and then growing a layer of oxide in the trenches. Finally, the layer of oxide is polished back.

Through the use of the preferred embodiment of the present invention, a shallow trench isolation process is implemented as opposed to LOCOS process, thereby reducing the occurrence of poly1 stringers in the channel area. Accordingly, the occurrence of unwanted electrical shorting paths between the adjacent regions is substantially reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a flow chart illustrating the conventional process steps required to fabricate a NAND flash memory array along with a series of cross sectional views of a substrate showing the resulting structure.

Figure 2(a) illustrates a properly aligned channel area.

Figure 2(b) illustrates a misaligned channel area.

Figures 3(a-c) show the formation of poly1 stringers.

Figure 4 is a flow chart illustrating the method steps for fabricating a NAND flash memory array in accordance with the preferred embodiment of the present invention along with a series of cross sectional views of a substrate showing the resulting structure.

Figure 5 is a cross-sectional view of the substrate showing an example of a trench isolation structure in accordance with the present invention.

Figure 6 is a cross-sectional view of the substrate showing the step height after the polishing of the oxide layer.

MODES FOR CARRYING OUT THE INVENTION

The present invention provides a method and system for fabricating a flash memory array. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment will be readily apparent to those skilled in the art and the generic principles herein may be applied to other embodiments. Thus, the present invention is not intended to be limited to the embodiments shown but is to be accorded the widest scope consistent with the principles and features described herein.

The method and system in accordance with the present invention is described in the context of a preferred embodiment. The preferred embodiment provides a method and system for fabricating a flash memory array wherein shallow trench isolation, rather than LOCOS, is used to provide field isolation structures.

Figure 4 is a flow chart illustrating the method steps for fabricating a NAND flash memory array in accordance with the preferred embodiment of the present invention. Also shown is a series of cross sectional views (Figures 4(a-g)) of a substrate showing the resulting structure.

The method begins by depositing a layer of oxide over a surface of bare silicon, via step 40. Next, a thin layer of nitride is patterned over a substrate, via step 42. Preferably, this layer of nitride defines the active regions and has a height of approximately between 1400-1700 Angstroms. A silicon trench etch is then performed to form shallow trenches in the substrate in isolation locations, via step 44. Preferably, the shallow trenches are anisotropically etched into the substrate and are approximately 3000 Angstroms in depth. After the shallow trenches are formed, a layer of oxide is grown in the shallow trenches, via step 446. Preferably this oxide layer is approximately 6000 Angstoms thick.

Please refer now to Figure 5. Figure 5 is cross-sectional view of the substrate showing an example of a trench isolation structure in accordance with the present invention after step 46. A shallow trench 50 containing the oxide layer 52 is shown located between active regions, which are masked with nitride 54.

Referring back to Figure 4, the oxide layer is then polished back, via step 48.

This is done to planarize the oxide surface. Consequently, it is preferable that the top surface of the oxide layer and the top surface of the nitride layer are on substantially the same plane after step 48. Figure 6 is cross-sectional view of the substrate after step 48 wherein the top surface of the nitride layer 60 and the top surface of the oxide layer 62 are on substantially the same plane. By polishing the oxide layer back to the nitride layer, the step height 64 is preferably between 300-900 Angstroms. This is significantly lower than the step height of the conventional process (1500-2500 Angstroms).

Again referring back to Figure 4, the nitride layer is then stripped, via step 50. A layer of poly1 is then deposited over the substrate, via step 52. Finally, the layer of poly1 is etched to define channel areas in the memory array, via step 54. Based on the significant decrease in step height provided by utilizing the method in accordance with the present invention, the subsequent deposition and etching of poly1 material results in a substantial decrease in the amount of poly1 stringers left in the channel region due to channel misalignment. Accordingly, the occurrence of unwanted electrical shorting paths between the adjacent regions is substantially reduced.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A flash memory array, comprising;

a substrate comprising active regions, wherein the active regions are defined by a layer of nitride (54), the layer of nitride (54) including a top surface;

shallow trenches (50) in the substrate, each of the shallow trenches (50) including a layer of oxide (52), the layer of oxide (52) having a top surface, wherein the top surface of the layer of oxide (52) and the top surface of the layer of nitride (54) are on substantially the same plane; and

channel areas (53) formed above the shallow trenches (50), wherein the occurrences of poly1 stringers is substantially reduced in the channel areas.

2. The flash memory array of claim 1 wherein the oxide layer (52) includes a step height (64) wherein the step height (64) is no greater than 900 Angstroms.

3. The flash memory array of claim 2 wherein the step height (64) is between 300 and 900 Angstroms.

4. A method for fabricating a memory array comprising the steps of:

(a) providing (40) a layer of nitride over a substrate;

(b) forming (42, 44) trenches in the substrate;

(c) providing (46) a layer of oxide in the trenches; and

(d) polishing (48) back the layer of oxide.

5. The method of claim 4 wherein step d) further comprises:

(d1) polishing (48) back the layer of oxide wherein a top surface of the layer of oxide and a top surface of the layer of nitride are on substantially the same plane.

6. The method of claim 5 further comprising:

(e) providing (52) a layer of poly1 over the substrate; and

(e) etching (50) the layer of poly1 to define channel areas in the memory array wherein the occurrences of poly1 stringers in the channel areas is substantially reduced.

7. The method of claim 6 wherein step (a) further comprises:

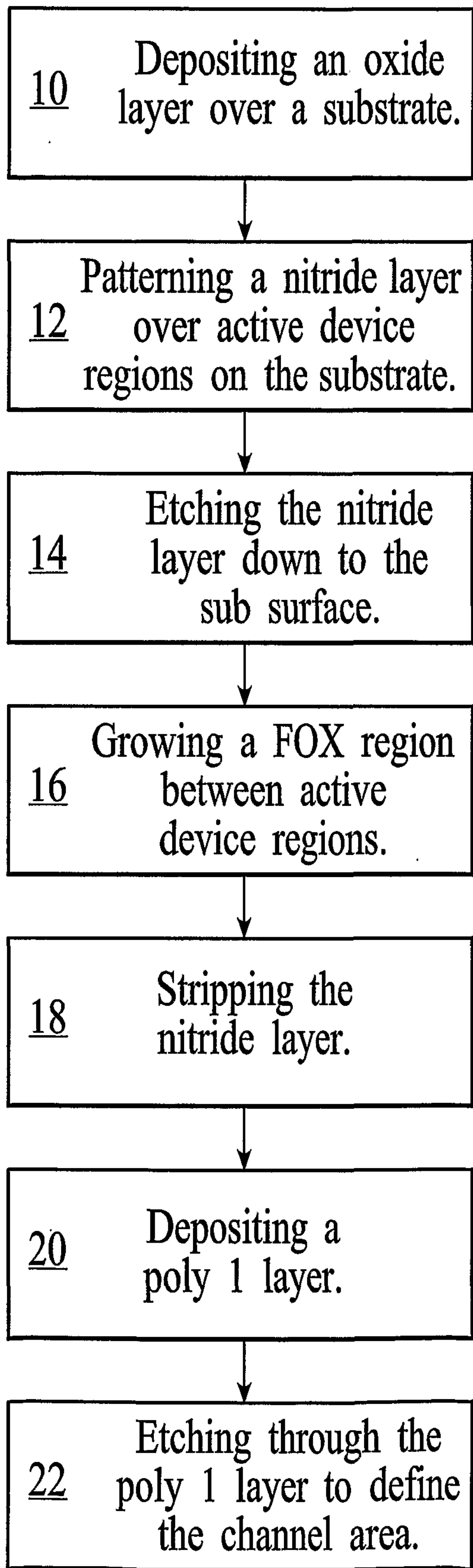
(a1) patterning (42) the layer of nitride to define active regions on the substrate.

8. The method of claim 7 wherein step (b) further comprises:

(b1) performing (44) a silicon etch to form the trenches.

9. The method of claim 8 wherein the oxide layer (52) includes a step height (64) wherein the step height is no greater than 900 Angstroms.

10. The method of claim 9 wherein the step height (64) is between 300 and 900 Angstroms.



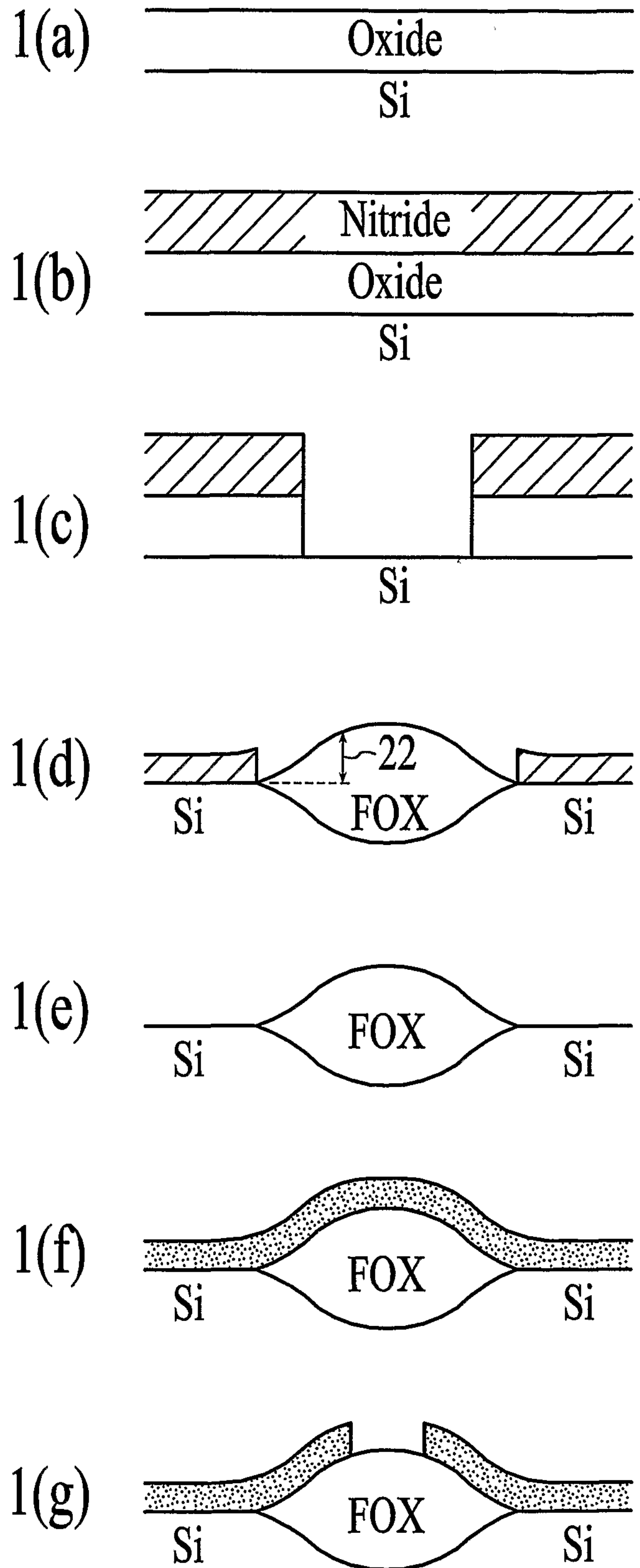


FIG. 1 (PRIOR ART)

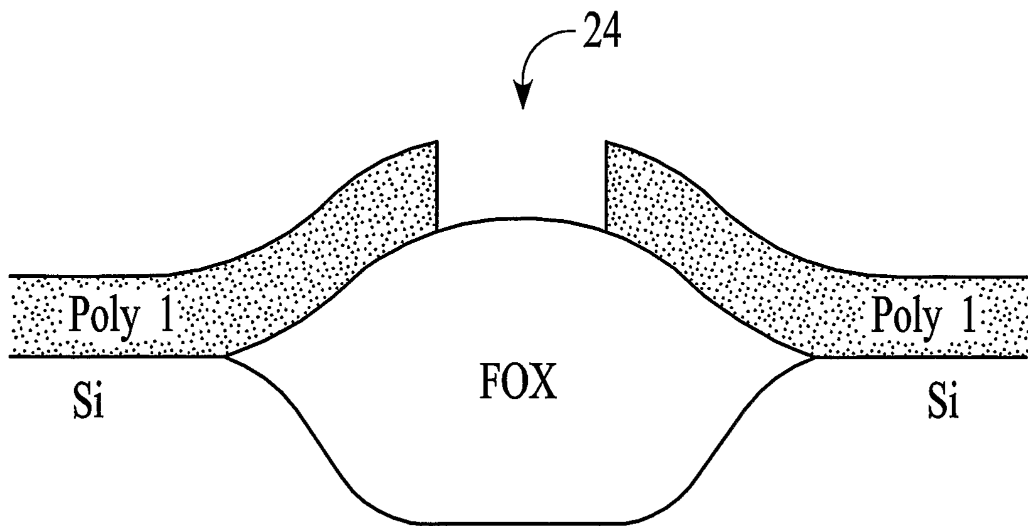


FIG. 2A
(PRIOR ART)

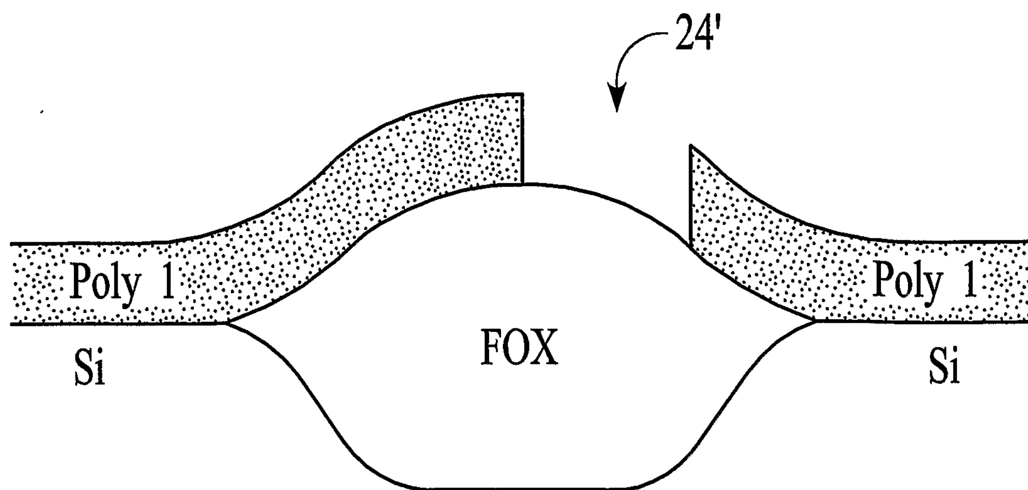


FIG. 2B
(PRIOR ART)

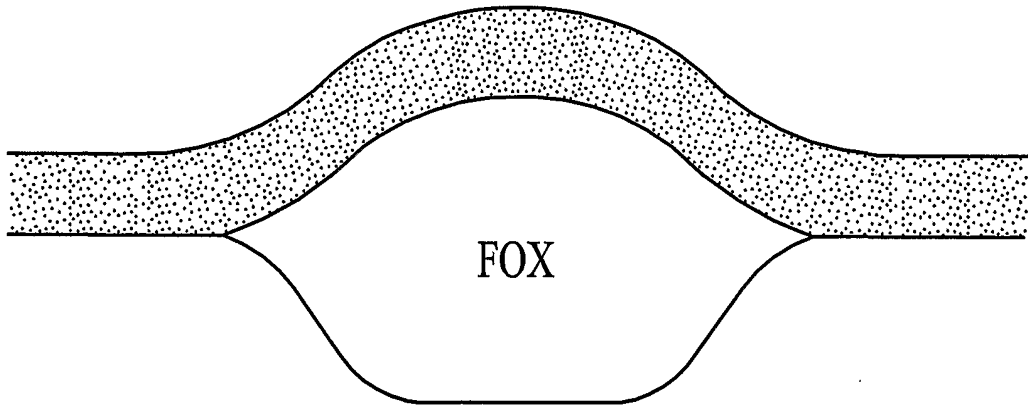


FIG. 3A
(PRIOR ART)

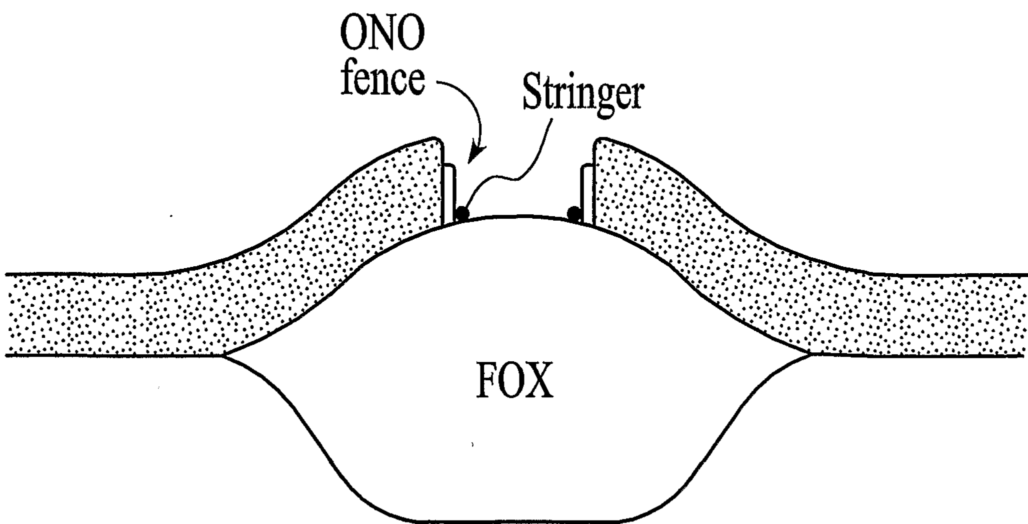


FIG. 3B
(PRIOR ART)

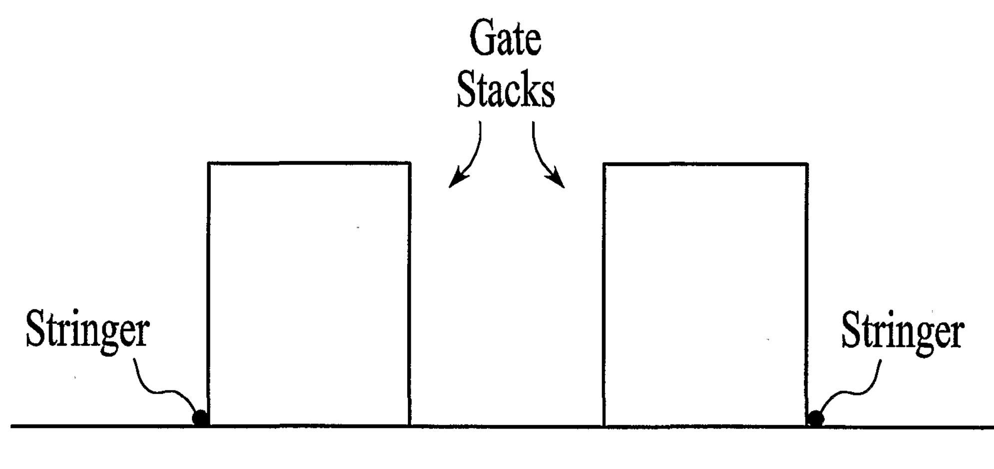
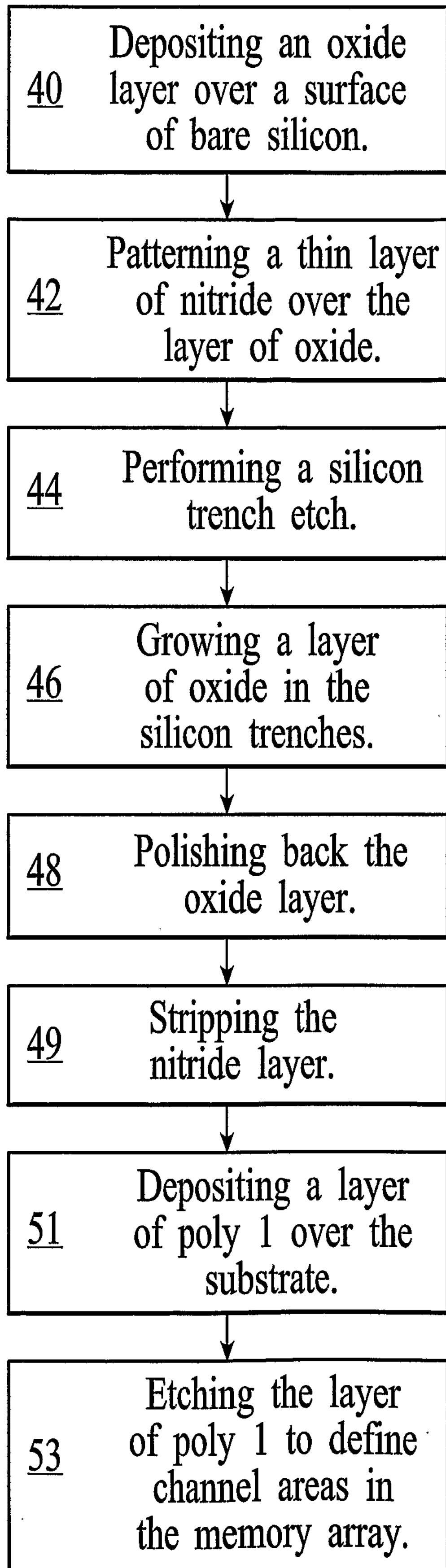


FIG. 3C
(PRIOR ART)



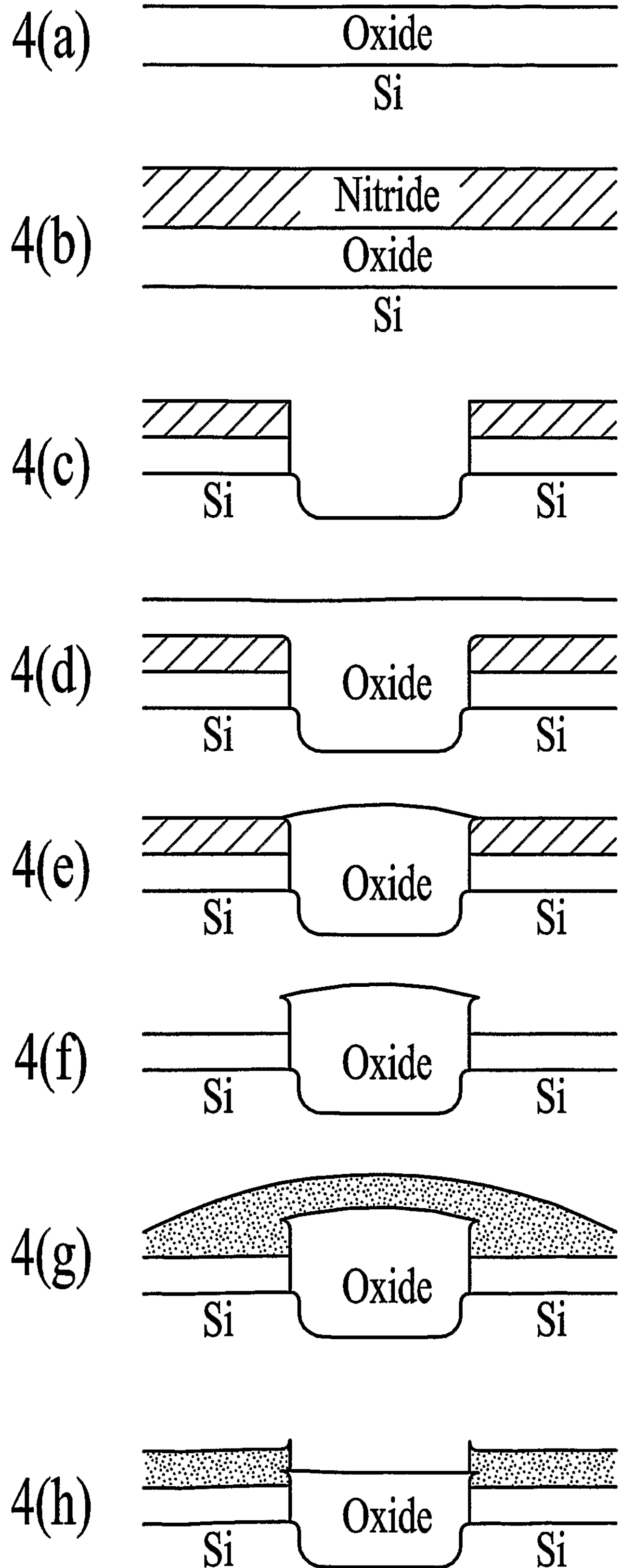


FIG. 4

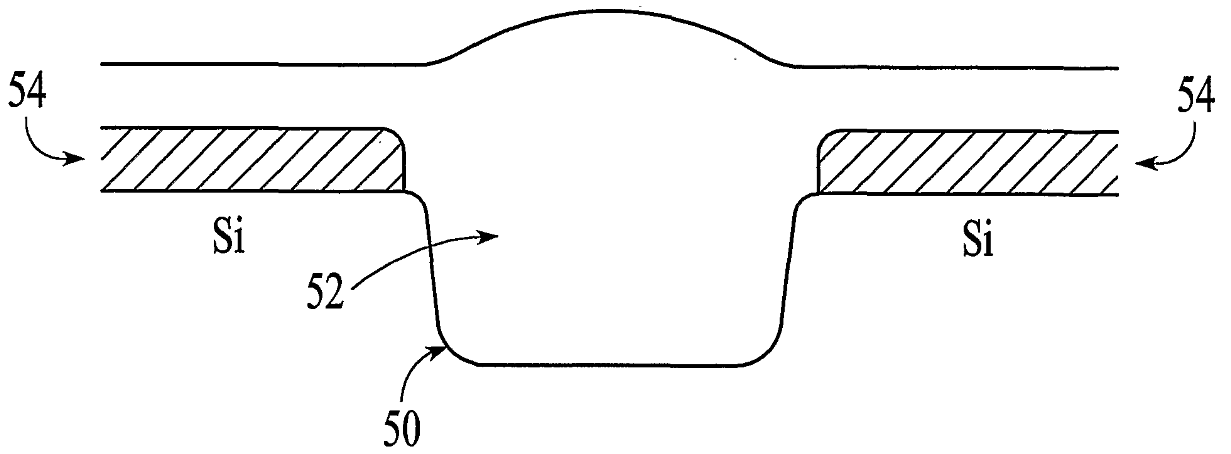


FIG. 5

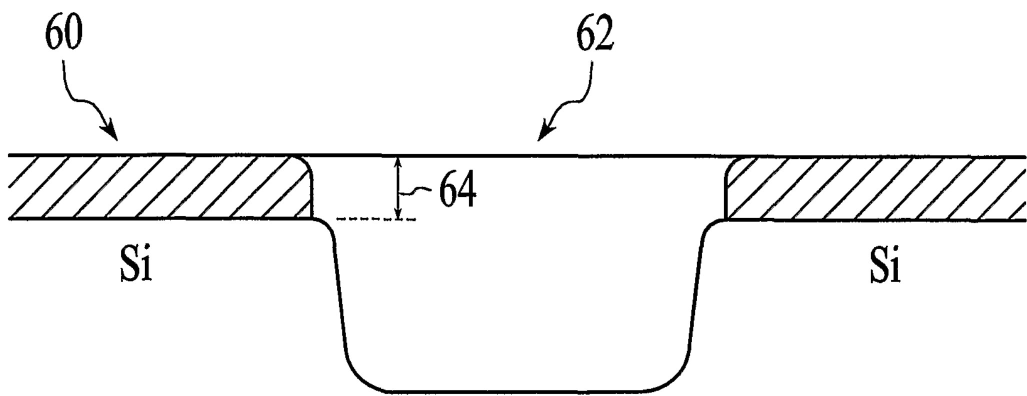


FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/10922

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/762 H01L21/8247

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 008 112 A (ACOCELLA JOYCE MOLINELLI ET AL) 28 December 1999 (1999-12-28) the whole document	1-10
X	WO 97 19467 A (BROUQUET PIERRE ;FRANCE TELECOM (FR); MASUREL CLAUDE (FR); RIVOIRE) 29 May 1997 (1997-05-29)	1-5
A	the whole document	6-10
X	US 5 885 883 A (PARK MOON-HAN ET AL) 23 March 1999 (1999-03-23)	1-5
A	the whole document	6-10
X	US 6 057 580 A (TAKEUCHI YUJI ET AL) 2 May 2000 (2000-05-02) column 12, line 30 -column 16, line 14; figures 19-40E	1,4-8

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 September 2001	26/09/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Albrecht, C

Form PCT/ISA/210 (second sheet) (July 1992)

Inte nal Application No
PC1/US 01/10922

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 12, 25 December 1997 (1997-12-25) -& JP 09 213783 A (SONY CORP), 15 August 1997 (1997-08-15) abstract -----	1,4-8

INTERNATIONAL SEARCH REPORT

rmation on patent family members

Inte ıal Application No
PCı/uS 01/10922

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 6008112	A	28-12-1999	JP	11261040 A	24-09-1999
			TW	409367 B	21-10-2000
WO 9719467	A	29-05-1997	FR	2741748 A1	30-05-1997
			FR	2741749 A1	30-05-1997
			WO	9719467 A1	29-05-1997
US 5885883	A	23-03-1999	KR	195208 B1	15-06-1999
			JP	10004136 A	06-01-1998
US 6057580	A	02-05-2000	JP	11026728 A	29-01-1999
JP 09213783	A	15-08-1997	NONE		