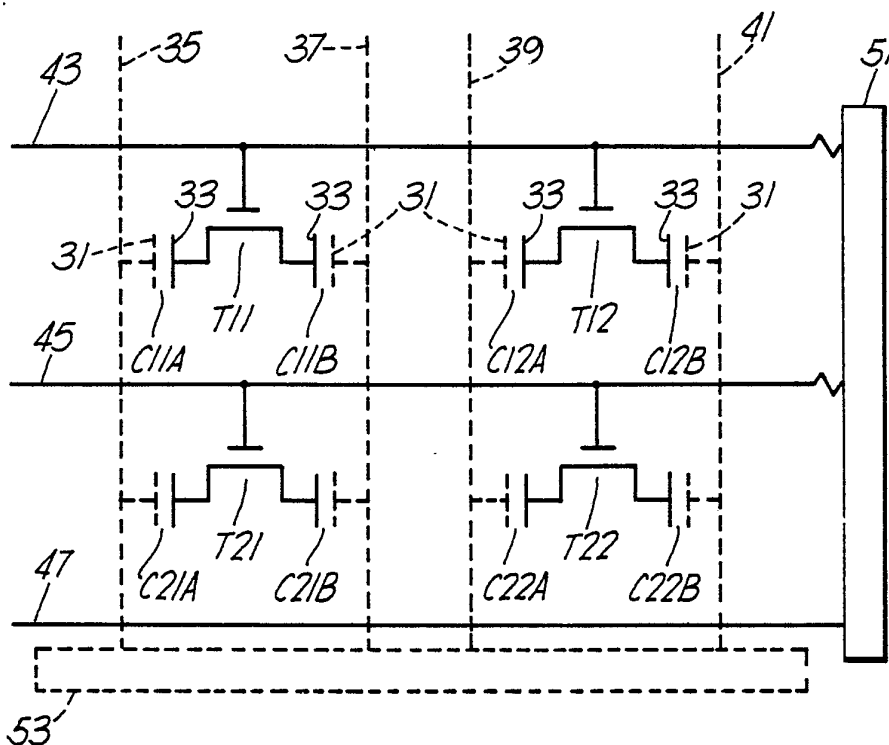




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(54) Title: MATRIX ADDRESSABLE DISPLAYS



(57) Abstract

An electro-optic display comprises a two dimensional array of liquid crystal cells (C11A,B to C44A,B) each switchable by means of electrical signals applied to respective pairs of address lines connected to the cell by respective transistors (T11 - T44). Each main electrode of each transistor is isolated from the rest of the array by a respective cell of the array.

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-1-

### Matrix Addressable Displays

This invention relates to matrix addressable displays. In particular the invention relates to matrix addressable displays of the kind comprising a two dimensional array of switchable cells, each cell having two electrodes each carried on a surface of a respective one of  
5 two plates, each cell being switchable by means of electrical signals applied to a respective pair of electrical address lines connected to the cell, each address line within a pair being connected to a different plurality of cells within the array.

To overcome the problems of multiplexing the address lines in such a display, i.e. in order to identify uniquely the cell to be  
10 switched at any one time and prevent partial switching of other cells connected to one of the pair of address lines, it is known to connect each cell to its respective pair of address lines via a respective transistor, for example, a thin film transistor, i.e. the so-called  
15 'active matrix addressing' approach.

Figure 1 is a schematic circuit diagram of part of such a known display.

Referring to Figure 1, the illustrated part of the display comprises an array of liquid crystal cells C11 to C22, each cell being  
20 represented in the figure as a capacitor. One electrode 3 of each cell is carried on the inner surface of a first insulating plate, this plate being transparent, the electrode 3 being the size of a pixel of

the display, and being made of a transparent conductor, such as indium tin oxide. The other electrode 5 of each cell is defined on the opposing surface of a second insulating plate, this surface carrying a series of parallel conductive column tracks 7, 9, 11 all components carried on this second plate being shown dotted in the figure.

In respect of each cell, there is provided a respective n channel thin film field effect transistor T11 to T22 carried on the first plate. One main electrode of each transistor, hereinafter referred to as a drain for convenience, is connected to the electrode 3 of each cell, whilst the gate of each transistor is connected to a selected gate address line 13, 15, 17 within a series of parallel conductive row tracks on the first plate. The second main electrode of the transistor hereafter referred to as the source for convenience, is connected to an earth line in the form of a family of conductive row tracks 19, 21 extending across the first plate parallel to the gate address lines 13, 15, 17.

In the use of the display, appropriate synchronised gate and source voltage pulses are applied to a selected pair of gate and source address lines. This then selectively addresses the one transistor which is connected to both the selected address lines. The capacitor constituted by the cell connected to the selected transistor is then able to charge up to the voltage required to give a response in the liquid crystal cell, the capacitor then being isolated when the transistor is subsequently switched off, the charge held on the capacitor being effective to switch the cell in the sense of changing the reflectivity of the liquid crystal and thus producing the required pixel image.

Such a display, however, suffers the disadvantage that a single short in a transistor gate results in the failure of the entire row of the display to which the shorted transistor belongs, even a single row failure being totally unacceptable in a display. Such row failures could be turned into single pixel failures by identifying and disconnecting faulty transistors, single pixel failures being much less noticeable and thus tolerable in some applications. This process is however time consuming and expensive particularly for large numbers of pixels.

The above known display presents another problem also. Due to photolithographic defects, dust particles and similar faults, shorts may occur between adjacent pairs of gate and drain lines which are carried on the same plate as the transistors, this leading to electrical interference between adjacent rows of the display. In order to ease this problem, the spacing between adjacent address lines must be relatively large, and thus useful display space is wasted and the maximum achievable resolution is limited.

It is an object of the present invention to provide an addressable matrix display of the kind specified, in which each switchable cell is addressed via a respective transistor but wherein the above problems are at least alleviated.

According to the present invention an addressable matrix display comprising a two dimensional array of switchable cells, each cell having two electrodes each carried on a surface of a respective one of two plates, each cell being switchable by means of electrical signals applied to a respective pair of electrical address lines connected to the cell by a transistor, each address line within a pair being connected to a different plurality of cells within the array and being carried on a different one of the plates, is characterised in that each main electrode of each transistor is isolated from the rest of the array by a respective cell of the array.

Each cell is suitably a liquid crystal cell.

Five matrix addressable displays in accordance with the invention will now be described, by way of example only, with reference to Figures 2 to 22 of the accompanying drawings in which:

Figure 2 is a schematic circuit diagram of the first display;

Figure 3 is a schematic plan view of the circuit elements of part of the first display;

Figure 4 illustrates a first voltage waveform scheme applicable to the first display;

Figure 5 illustrates a second voltage waveform scheme applicable to the first display;

Figure 6 is a schematic circuit diagram of part of the second display;

Figure 7 is a schematic plan view of a first circuit element configuration of the third display;

Figure 8 is a schematic plan view of a circuit element configuration of a first adaptation of the third display;

5        Figure 9 is an equivalent circuit of the circuit element configuration illustrated in Figure 8;

Figure 10 is a schematic plan view of the circuit element configuration of a second adaptation of the third display;

10       Figure 11 is an equivalent circuit of the circuit element configuration illustrated in Figure 10;

Figure 12 is an equivalent circuit diagram illustrating a row across the first and second adaptations of the third display when the row is strobed;

15       Figure 13 illustrates the arrangement of the circuit elements carried on the first plate of a third adaptation of the third display;

Figure 14 illustrates the arrangement of the circuit elements carried on the second plate corresponding to the adaptation of the third display shown in Figure 13;

20       Figure 15 illustrates an alternative arrangement of the circuit elements carried on the second plate to that shown in Figure 14;

Figure 16 illustrates the arrangement of the circuit elements carried on the first plate of a fourth adaptation of the third display;

25       Figure 17 illustrates the arrangement of the circuit elements carried on the second plate for the fourth adaptation of the third display illustrated in Figure 16;

Figure 18 illustrates the arrangement of the circuit elements carried on the first plate of the fourth display;

30       Figure 19 illustrates the arrangement of the circuit elements carried on the second plate of the fourth display;

Figure 20 illustrates the arrangement of the circuit elements carried on the first plate of the fifth display;

35       Figure 21 illustrates the arrangement of the circuit elements carried on the second plate of the fifth display; and

Figure 22 illustrates an alternative arrangement of circuit elements carried on the second plate of the fifth display.

Referring firstly to Figure 2, as in the prior art display described herebefore with reference to Figure 1, the display comprises  
5 an array of liquid crystal cells C11A, C11B, C12A, C12B, C21A, C21B--- represented as capacitors, only eight such cells being shown for the sake of clarity, although it will be appreciated that a practical display will have typically up to 2000 x 1200 cells or more. The electrodes 31, 33 of each cell are formed on the opposing surfaces of  
10 a pair of parallel transparent insulating plates, all components carried on the second plate being shown dotted. As in the prior art display the second plate carries a number of parallel conductive column tracks 35, 37, 39, 41 these being orthogonal to a number of parallel conductive gate address lines 43, 45, 47 carried on the first  
15 plate, each cell having one electrode 31 connected to one column track 35, 37, 39, 41 and one electrode 33 connected via a transistor to one gate address line 43, 45, 47, 49. Unlike the prior art display however the electrodes 33 of each pair of two adjacent cells C11A and C11B etc in a row which are carried on the first plate are connected  
20 to the drain and source of the same transistor T11 etc. Respective peripheral driver circuits 51, 53 effective to provide drive voltages to the address lines 43, 45, 47 on the first plate, and 35, 37, 39, 41 on the second plate are also provided. It will be seen that unlike the prior art display shown in Figure 1, the nominal sources of  
25 different transistors in a row are separated by the liquid crystal cells connected to that row. Thus in the event of a short between a transistor gate and source and drain the gate line will remain isolated from the rest of the circuit by the high impedance of the pair of liquid crystal cells directly connected to that transistor.  
30 This will allow the other transistors in the row to be driven, thus limiting the failure to that pair of cells which are connected to the failed transistor. It will also be seen that as only one set of address lines, i.e. the gate address lines 43, 45, 47 for each row of pixels is carried on the plate carrying the transistors, these lines  
35 will be separated by a distance corresponding to at least the vertical

dimension of the pixel. Thus the probability of shorting adjacent conductive tracks on the plate carrying the transistors is greatly reduced over the prior art display for a similar resolution display of the same area.

5           It will be appreciated that even if the fabrication yield for the second plate decreases as a result of the increased complexity with respect to the prior art second plate, this will be by far offset by the increase in the yield for the first plate which remains the more complex and expensive item due to the fact that it carries the  
10 transistors.

          It will also be appreciated that for the above reasons it is also easier to connect the peripheral driver circuit 51 for the display to the gate line. The peripheral driver circuits 51, 53 can be connected to both plates through edge connectors or by mounting  
15 chips around the periphery of each plate with soldered contacts on the gate lines on the first plate and on the column tracks on the second plate. It can be convenient in some circumstances however to arrange for alternate column tracks 35, 39 to extend beyond the connectors or driving chips connected to the remaining tracks 37, 41. Although it  
20 may be convenient in some circumstances to address each column individually, it may be preferable in other cases to link one set of alternate columns together. This can be done by providing a bus bar connecting the said set of alternate columns, the bus bar crossing over or under the remaining columns. It should, however, be  
25 appreciated that even in this case the number of overlapping regions that are potential sources of shorts is greatly reduced with respect to known displays.

          It will be appreciated that the peripheral drivers may be replaced by thin film transistors fabricated in a manner similar to  
30 the transistors used to switch the cells of the array.

          Figure 3, illustrates a suitable practical configuration of the array. As shown the column tracks eg 35, 37 in Figure 3, are made narrower where they cross a gate line e.g. 45 in Figure 3 to reduce the capacitive coupling between column tracks and gate lines.

35

Referring now also to Figure 4, in use of the display the peripheral driver circuits 51, 53 are used to apply electrical signals to the various conductive tracks. Each row of the array is sequentially addressed by a respective series of strobe pulses  $V_{GM}$  applied to each gate line 43, 45, 47, the series being temporally offset.  $V_{DATA}$ ,  $V_{REF}$  denote the voltage waveforms, with respect to earth applied to one particular pair of source and drain lines, for example 35, 37 carried on the second plate,  $\Delta V_A$  and  $\Delta V_B$  being the voltage drops across the respective cells C11A, C11B connected to these lines, it being appreciated that corresponding signals will be applied simultaneously to all the source and drain lines across the array, such that the pixels within each row of the array are simultaneously addressed. The voltages with respect to earth appearing at the electrodes 33 carried on the first plate of these cells C11A, C11B are denoted  $V_A$ ,  $V_B$ .

Thus, where the transistor T11 is an n - channel transistor

$$V_A = V_{DATA} - \Delta V_A$$

$$V_B = V_{REF} + \Delta V_B$$

The time  $T_{frame}$  taken to address each cell C11 to C22 within the array will consist of two on-cycles alternated with two off-cycles, each on-cycle being of duration  $MT_r$  where M is an integer, and  $T_r$  is the cell refresh time, the value of M being selected taking into account such factors as the characteristics of the transistors, liquid crystal material, and the speed of the driving electronics, the waveforms applied during these periods being described hereafter. Each off-cycle is of duration  $T_r$ , the function of the off-cycle being to reduce the maximum voltage between nominal source and nominal drain of each transistor after each on-cycle, these voltages otherwise resulting in high leakage currents, and eventually in the breakdown of the transistor. It will be appreciated however that the off-cycles can be omitted in some circumstances dependent on the characteristics of the transistors.

Within each on-cycle  $V_{DATA}$  consists of a series of pulses, synchronised with the leading edge of a strobe pulse  $V_{GM}$  which causes the transistor  $T_{11}$  to conduct. This is followed by an off-cycle in which both  $V_{DATA}$  and  $V_{REF}$  are at zero potential, the strobe pulse  $V_{GM}$  applied during this period enabling both cells  $C_{11A}$ ,  $C_{11B}$  to discharge. In the subsequent on-cycle,  $V_{DATA}$  consists of a series of pulses which are the complement of those in the first on-cycle and which are again synchronised with the leading edge of a strobe pulse  $V_{GM}$ , the waveforms in the second off cycle being the same as in the first off-cycle. During the first on-cycle and the first off-cycle  $V_{REF}$  is zero,  $V_{REF}$  being pulsed to a value of  $2V_{MAX}$  during the second on-cycle. Thus it will be seen that in the first on-cycle  $V_{REF}$  is always equal to 0 and  $V_{DATA}$  is either  $2V_{MAX}$  or 0 dependent on whether the cells  $C_{11A}$ ,  $C_{11B}$  are selected or unselected where  $V_{MAX}$  is the voltage required to switch the cell fully on. In the second on-cycle  $V_{REF}$  is equal to  $2V_{MAX}$  and  $V_{DATA}$  is either 0 if the cells  $C_{11A}$ ,  $C_{11B}$  are selected, or  $2V_{MAX}$  if these cells are unselected. Thus the cells which are selected will be charged to a potential difference close to  $V_{MAX}$  whilst the unselected cells will be at zero potential difference, the cells within a pair of cells connected to the same transistor of course being either both selected or both unselected.

It will be seen that in the above address scheme the polarity of the voltages  $\Delta V_A$ ,  $\Delta V_B$  applied across each chosen cell in alternate on-cycles is reversed, this preventing degradation of the liquid crystal due to electrolysis.

It will be appreciated that by virtue of the two cells connected to each transistor in a display in accordance with the invention, the capacitance to be charged by each transistor is a quarter of that in a comparable prior art display with the same resolution. This enables the use of transistors with lower on-currents, for example amorphous silicon thin film transistors.

Referring now to Figure 5, various other drive schemes for the display shown in Figure 2 are of course possible. In Figure 5 it will be seen that the strobe pulses  $V_{GM}$  applied during the second on-cycle and second off-cycle are at a different dc level to the pulses  $V_{GM}$  applied during the first on-cycle and first off-cycle.

Furthermore  $V_{REF}$  and  $V_{DATA}$  within the second off-cycle are set at  $2V_{MAX}$ . Such an alternative drive scheme has the advantage over that described in relation to Figure 4 that the maximum voltage difference between the gate of each transistor, and the corresponding cell electrodes carried on the same plate as the transistors is  $3V_{MAX}$ . It will be seen from Figure 4 that the corresponding voltage is  $4V_{MAX}$ . Thus the transistor leakage current for the Figure 5 scheme is less than for the Figure 4 scheme, this being particularly important for displays incorporating polycrystalline silicon transistors, as the leakage current is a strong function of the gate-source and gate-drain voltages. Furthermore the reliability of the transistors will be higher due to the lower fields through the gate oxide.

Referring now to Figure 6 this figure illustrates the part of the second display to be described, the part comprising a three by three array of pixels, corresponding components of each of the further displays to be described being labelled as in the first display in accordance with the invention described herebefore. The array is, as before connected to gate address lines 43, 45, 47 carried on the first plate, and reference and data address lines 35, 37, 39, 41, 42, 44 carried on the second plate, appropriate driver circuits (not shown) being provided to provide the required voltages across the address lines. The second display is however distinguished from the first display in that each pair of cells for example C11A, C11B within a pixel is addressed by two transistors T11A, T11B whose gates are driven by adjacent gate lines 43, 45 as shown in the figure. Thus in operation of the second display, as for example the gate line 45 is strobed by the pulses  $V_{GM}$ , the sets of four cells C11A, C11B, C21A, C21B etc., in the pixel rows above and below the gate line 45 will be charged to the same values by application of appropriate data and reference voltage waveforms to the source and drain lines, these being chosen such that the upper pixel row is addressed in the desired manner. The lower pixel row will then be reset and addressed in the desired manner for that row when the next gate line 47 is strobed. It will be appreciated that the uppermost and lowermost rows of transistors within the array will be exceptional in that they have gate lines devoted to themselves.

The address schemes required for this second display will be evident to those skilled in the art of matrix address displays in view of the schemes as disclosed in Figures 4 and 5 described herebefore, in conjunction with those disclosed by Takeda et al in Japan Display  
5 86, pages 204-7, published in 1986.

It will be appreciated that the advantage of the arrangement shown in Figure 6 lies in that if a transistor is faulty, and is disconnected by for example laser cutting, the cells connected to that  
10 transistor will still be charged to a definite value. If the upper transistor within a pixel, for example T21A has to be disconnected, the cells C21A, C21B will be charged to the correct value. If the lower transistor within a pixel, for example T21B is disconnected however, the cells will be charged to the value of the cells C11A, C11B in the next row above: this is nevertheless not so disturbing to  
15 an observer of the display as an obviously inactive pair of pixels. The disturbance may be further reduced by having an arrangement of driver circuits such that the gate lines are first strobed in order working down the display (--- 43, 45, 47 --) and then strobed in order working up the display (-- 47, 45, 43 --) with the result that cells  
20 connected to disconnected transistors are only charged wrongly in alternate frames.

It will be appreciated that in both displays in accordance with the invention described herebefore each pair of cells connected to the same transistor or transistors are charged to be the same  
25 potential. In some applications however, one may choose that the cells within each pair are of different shapes such that the difference in capacitance between the two cells results in a different partition of the voltages across the two cells. Alternatively where the cells within each pair be identical, but it is required that the  
30 cells within each pair are charged to different values, the arrangement shown in Figure 7 may be used. This arrangement is an adaptation of the display shown in Figure 6 in that each pair of cells within a pixel is addressed by two transistors whose gates are driven by adjacent gate lines. This third display is however distinguished  
35 from that shown in Figure 6 in that the pairs are arranged vertically and chained together into columns by the transistor source-drain

channels. In this way each cell is connected to a unique combination of two transistors by their main electrodes. The third display is also distinguished from that shown in Figure 6 in that the column address lines 35, 37, 39, 41 are replaced by respective pairs of meandering electrodes 71, 72 carried on the second plate, each electrode 71, 72 connecting alternate cell electrodes 31 on the second plate, the electrodes 71, 72 thus being interleaved as indicated in Figure 7. These electrodes will generally be fabricated with fine metal stripes, typically of aluminium, so as to provide adequate conductivity between the cell electrodes 31. In use of this third display, as the respective strobe pulses  $V_{GM}$  are applied to the successive gate lines 43, 45, 47, the pairs of cells in the rows on either side of the strobed gate line will be charged to the desired value for the upper row of cells, the lower row of cells being reset to the correct value when the next gate line down is strobed.

It will be seen that a disadvantage of the arrangement shown in Figure 7 is that the gaps between each column of cells must be relatively large in order to accommodate the two interleaving tracks. These gaps may be reduced somewhat by having a slightly zigzag arrangement of the columns of pixels but the appearance this creates may not be acceptable to the user. Figures 8 and 10 show two alternative arrangements of interleaved electrodes on the second plate in which these gaps are reduced. The corresponding equivalent circuits are shown in Figures 9 and 11 in which each cell is again shown as a capacitor and each transistor is shown as a switch, it being understood that all switches in a row are operated simultaneously as each gate line is strobed. In either of these arrangements, when one row is strobed (i.e. all the switches in that row are closed) the circuit to be addressed is equivalent to that shown in Figure 12. The addressing scheme required here is different to that used in the arrangements described above. The voltages applied to successive column i.e. second plate electrodes  $V_i$  ( $i=0,1,2,3 \dots N$ ) where  $N + 1$  is the number of column electrodes,

given by the algorithm

$$V_i = Vb_i$$

5 
$$b_i = a_i \oplus b_{i-1}$$

where  $V$  is a reference voltage and  $a_i$ ,  $b_i$  are binary digits,  $a_i$  being 1 or 0 according to whether the capacitor pair preceding column  $i$  is to be charged or not, respectively, and  $\oplus$  denotes addition modulo 2 (exclusive OR). In order to ensure absence of DC voltage across the cells, each frame consists of two fields identical except that the bit  $b_0$  is taken as 0 in one field and 1 in the other.

It will be evident that one disadvantage of the arrangements shown in Figures 8 and 10 is that it is difficult to display grey scale by varying the voltages on the cells so that they may assume intermediate values. These arrangements are therefore primarily suitable for alphagraphic displays. One preferred approach which avoids this difficulty is to have the source and drain lines carried on the second plate arranged as orthogonal sets with insulated crossovers. Although this increases the likelihood of faults in the second plate, this plate can be tested prior to assembly and, since it is the cheaper of the two, some wastage of the second plate alone may be economically acceptable. Figure 13 shows the arrangement of transistors and cell electrodes 33 on the first plate while Figures 14 and 15 show two possible connectivities for the second plate. In both cases the display may be addressed by applying waveforms of the types shown in Figures 4 and 5 as  $V_{DATA}$  to the column electrodes on the second plate and waveforms of the types shown as  $V_{REF}$  to the horizontal electrodes on the second plate.

It will be evident that in all of the arrangements shown in Figures 7 to 15 the members of a pair of cells connected by a transistor are arranged vertically, with both cells being initially charged to the required potential for the upper cell and the lower cell then being reset to the required potential in the next strobe interval. Another alternative is to connect the cells within such pairs of cells diagonally. Figure 16 shows a possible arrangement

for the first plate and Figure 17 the corresponding second plate arrangement, with D and R denoting electrodes which are driven with data and reference waveforms, respectively, indicated in the schemes of Figures 4 and 5.

5           It will be evident that in all of the arrangements shown in Figures 7 to 17 the lowest row of the array will remain set at the same value as the lowest but one unless special circuitry is provided for that row alone. Alternatively the lowest row may be masked from the user by a frame or bezel. It will also be evident that for the  
10 arrangement shown in Figures 16 and 17 alternate pixels in the first and last columns, these not being shown in the figures, must either be omitted or provided with special circuitry.

          Referring now to Figures 18 to 22, in order to produce a colour display of the type described, for example by Saito et al in  
15 the 1985 International Display Research Conference Proceedings, pages 27-29, each pixel of the matrix addressable display is divided into a triad of red, green and blue subpixels. Figures 18 and 19 illustrate such a display in accordance with the invention. Figure 18 shows part of the first plate which carries the transistors and associated gate  
20 lines 181, 183, 185, 187, each electrode 33 carried by the first plate within a pair of cells which are connected to the same transistor being associated with a respective colour filter of the same colour, red denoted R, green denoted G or blue denoted B. Each transistor within successive rows is displaced by half a subpixel.  
25 Figure 19 shows a corresponding part of the second plate which carries the electrodes 31 together with the source and drain column electrodes, it being seen that each column electrode is connected alternately to cells associated with filters of two different colours along each column.

30           A disadvantage of the arrangement shown in Figures 18 and 19 is that the whole of any one red/green/blue triad is not addressed with a single strobing interval on the respective gate lines. Figure 20 shows an alternative circuit component arrangement of the first plate which avoids this difficulty, two alternative arrangements for  
35 the corresponding second plate being shown in Figures 21 and 22. It will be seen from these figures that by applying voltage waveforms as

shown to the column electrodes carried on the second plate the whole of any red/green/blue triad may be addressed within a single strobing interval. In the figures  $D_R$ ,  $D_G$  and  $D_B$  denote voltage data waveforms for red, green and blue data respectively which are applied to the nominal transistor source lines, whilst R denotes the reference voltages applied across the nominal drain lines. The waveforms will be similar to those shown in Figures 4 and 5 with respect to the first display in accordance with the invention described herebefore.

It will be appreciated that the precise form of a display in accordance with the invention will depend on the application. In particular whilst the displays described herebefore are contained between a pair of insulating transparent plates, for example glass, one plate may take the form of a semiconductor crystal, the transistors being integrated within this crystal.

It will be appreciated that a capacitance other than a cell of the display may be used to isolate each main electrode of the transistors from the rest of the array. Such an arrangement however will not be as advantageous as a display in accordance with the invention.

It will be appreciated that whilst it is particularly convenient to use liquid crystal cells in a display in accordance with the invention, other forms of switchable cells may also be used. These include electroluminescent cells, PLZT and similar ferroelectrics, electrochromic cells, electrophoretic cells and vacuum switches.

It will also be appreciated that whilst the gate, source and drain address lines shown in the displays in accordance with the invention described herebefore are either parallel or orthogonal to each other, this invention is also applicable to non-rectangular arrays, in which the address lines take, for example, a radial configuration for use in analogue displays for instrumentation.

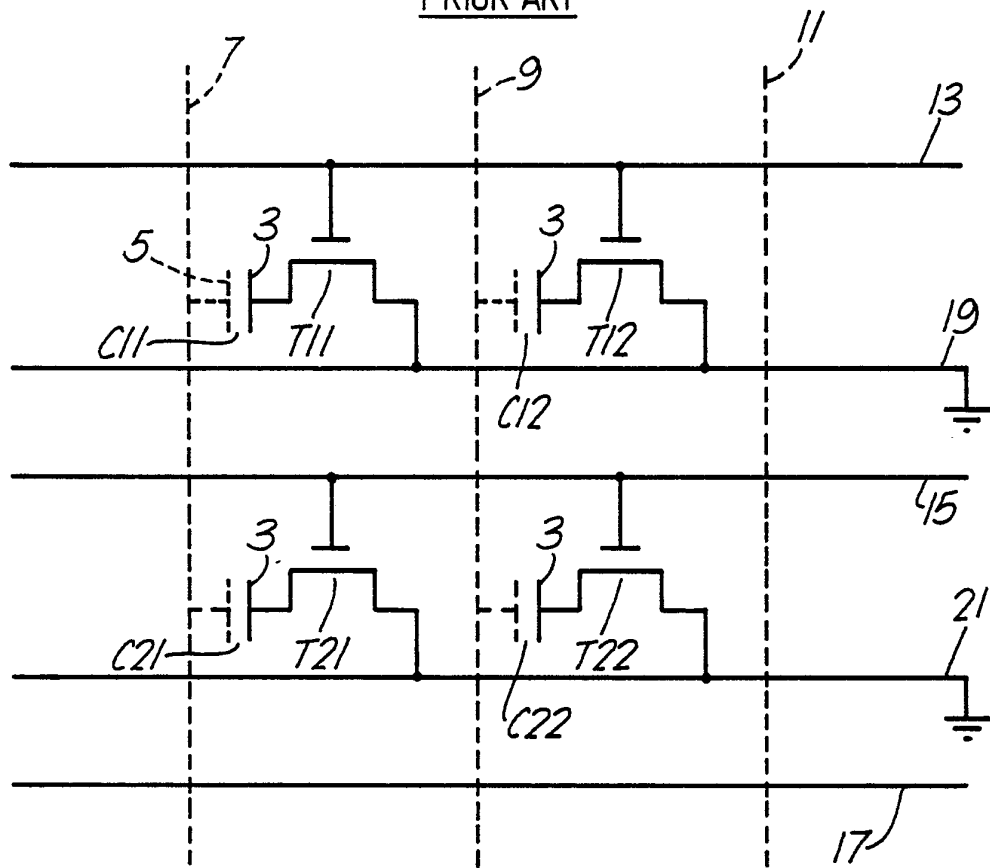
CLAIMS

1. An matrix addressable display comprising a two dimensional array of switchable cells, each cell having two electrodes each  
5 carried on a surface of a respective one of two plates, each cell being switchable by means of electrical signals applied to a respective pair of electrical address lines connected to the cell by a transistor, each address line within a pair being connected to a different plurality of cells within the array and being carried on a  
10 different one of the plates the display being characterised in that each main electrode of each transistor is isolated from the rest of the array by a respective cell of the array.
2. A display according to Claim 1 in which each cell is a liquid crystal cell.
- 15 3. A display according to either one of the preceding claims including drive means for applying drive voltages effective to periodically reverse the polarity of the voltages across each of said cells.
4. A display according to Claim 3 including means for applying a  
20 reference potential to one main electrode of each transistor, said reference potential being periodically pulsed so as to cause said periodic reversal of polarity.
5. A display according to any one of the preceding claims including a drive means for applying drive voltages effective to  
25 reduce the voltages between the main electrodes of each transistor after switching of the cells.
6. A display according to Claim 5 in which one set of said electrical signals are in the form of strobe pulses applied sequentially to the control electrodes of each transistor, the dc  
30 level of said strobe pulses varying within each said sequence so as to reduce the voltages between each main electrode and the control electrode of each transistor.
7. A display according to any one of the preceding claims in which each cell is connected to two transistors whose main electrodes  
35 are connected to the same pair of address lines.

8. A display according to any one of the preceding claims including means for applying different voltages across each pair of cells which are connected to the same transistor.
9. A display according to Claim 8 in which each cell within each  
5 said pair of cells is of different dimensions.
10. A display according to Claim 8 in which each cell is connected to a main electrode of a different one of the transistors.
11. A display according to Claim 10 in which the address lines connected to the main electrodes of the transistors comprise two  
10 individual conductive tracks, each track being connected to alternate cells along the array.
12. A display according to Claim 11 in which said two conductive tracks extend in different directions across the array.
13. A display according to any one of the preceding claims  
15 including drive means for applying voltages across the cells which may be variable so as to enable partial switching of the cells.
14. A display according to any one of the preceding claims in which each pair of cells connected to the same transistor lie within the same column or the same row of said array.
- 20 15. A display according to any one of Claims 1 to 13 in which each pair of cells connected to the same transistor lie within different columns and different rows of said array.
16. A display according to any one of the preceding claims in which each cell is associated with a colour filter.
- 25 17. A display according to Claim 16 in which each cell within a trio of cells is associated with a filter of a different primary colour.
18. A display according to Claim 17 in which the address (lines and the lines providing reference voltages to the transistors) are  
30 arranged such that each cell within said trio of cells may be addressed simultaneously.
19. A display according to any one of the preceding claims including screening means around peripheral regions of the display effective to screen cells within the array which are not uniquely  
35 addressable.

20. A matrix addressable display substantially as hereinbefore described with reference to Figures 2 to 22 of the accompanying drawings.

Fig. 1.  
PRIOR ART



2/11

Fig. 2.

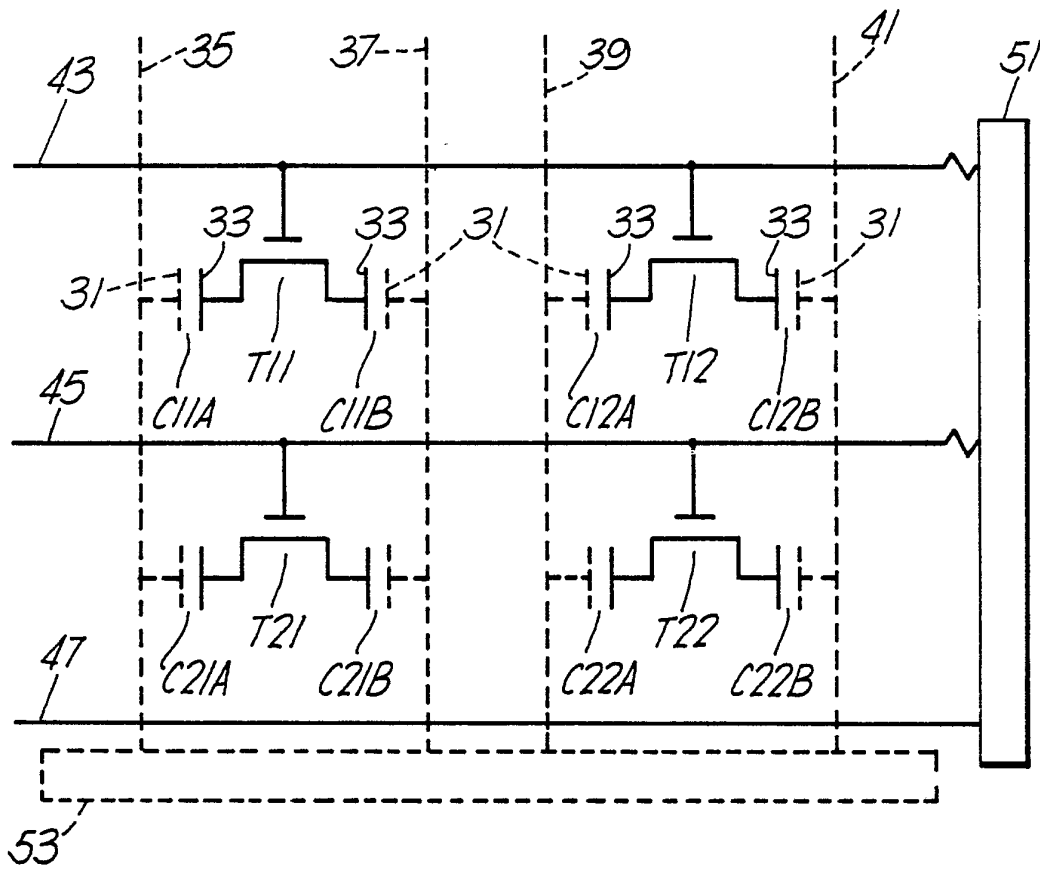
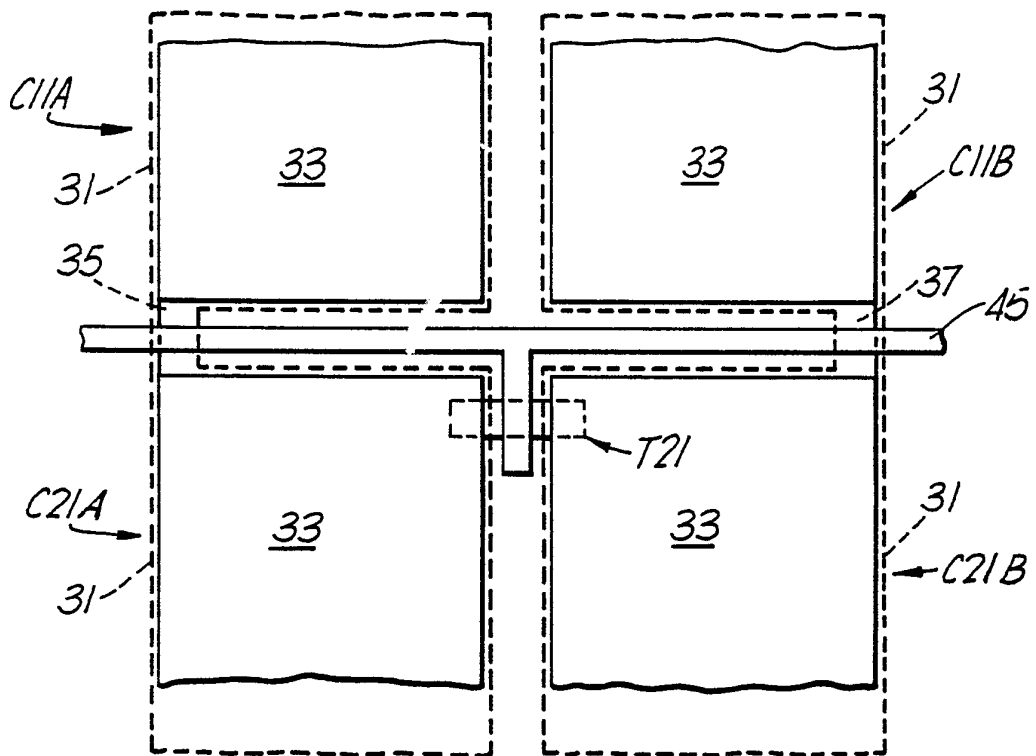


Fig. 3.



3/11

Fig. 4.

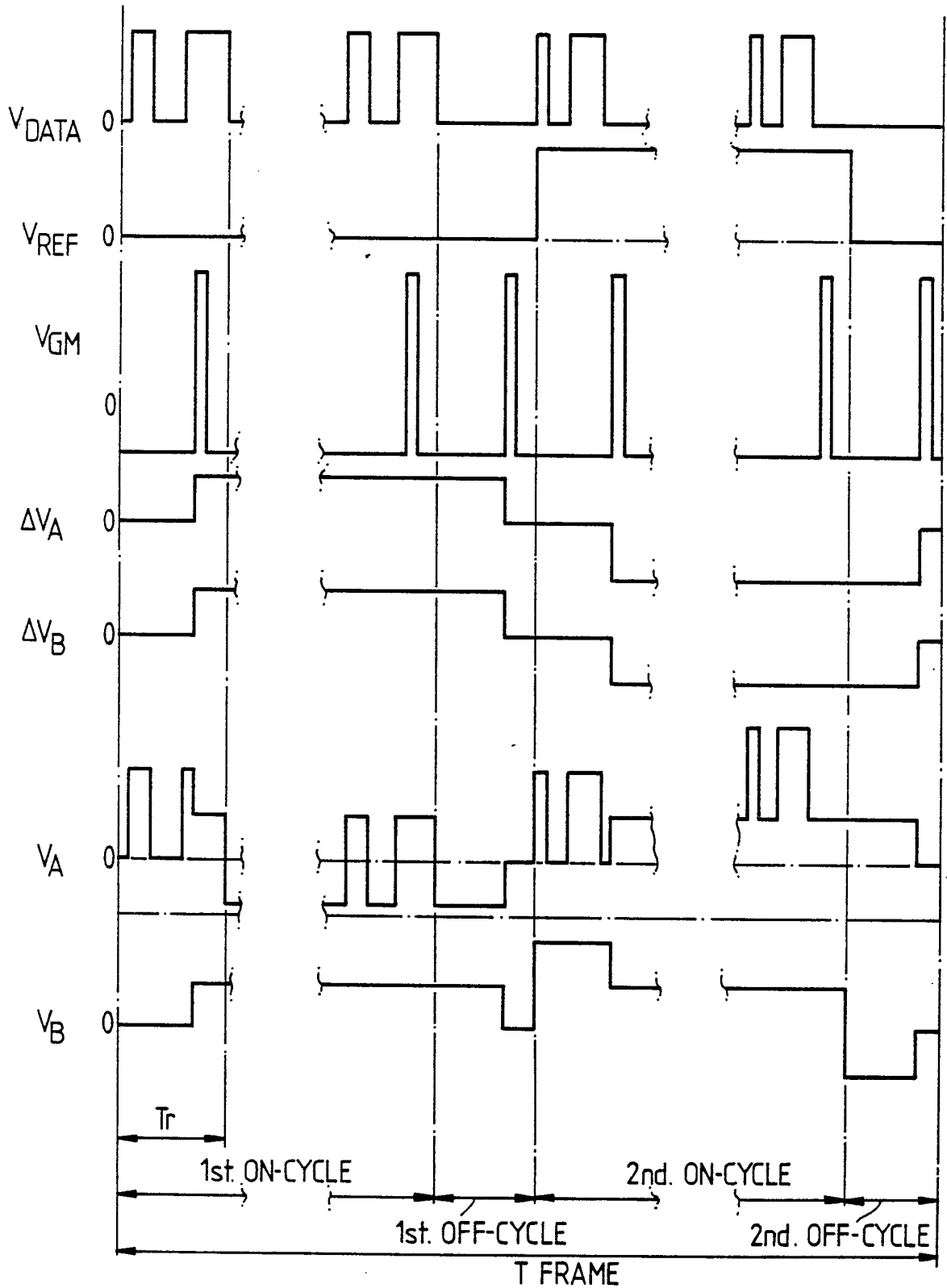


Fig. 5.

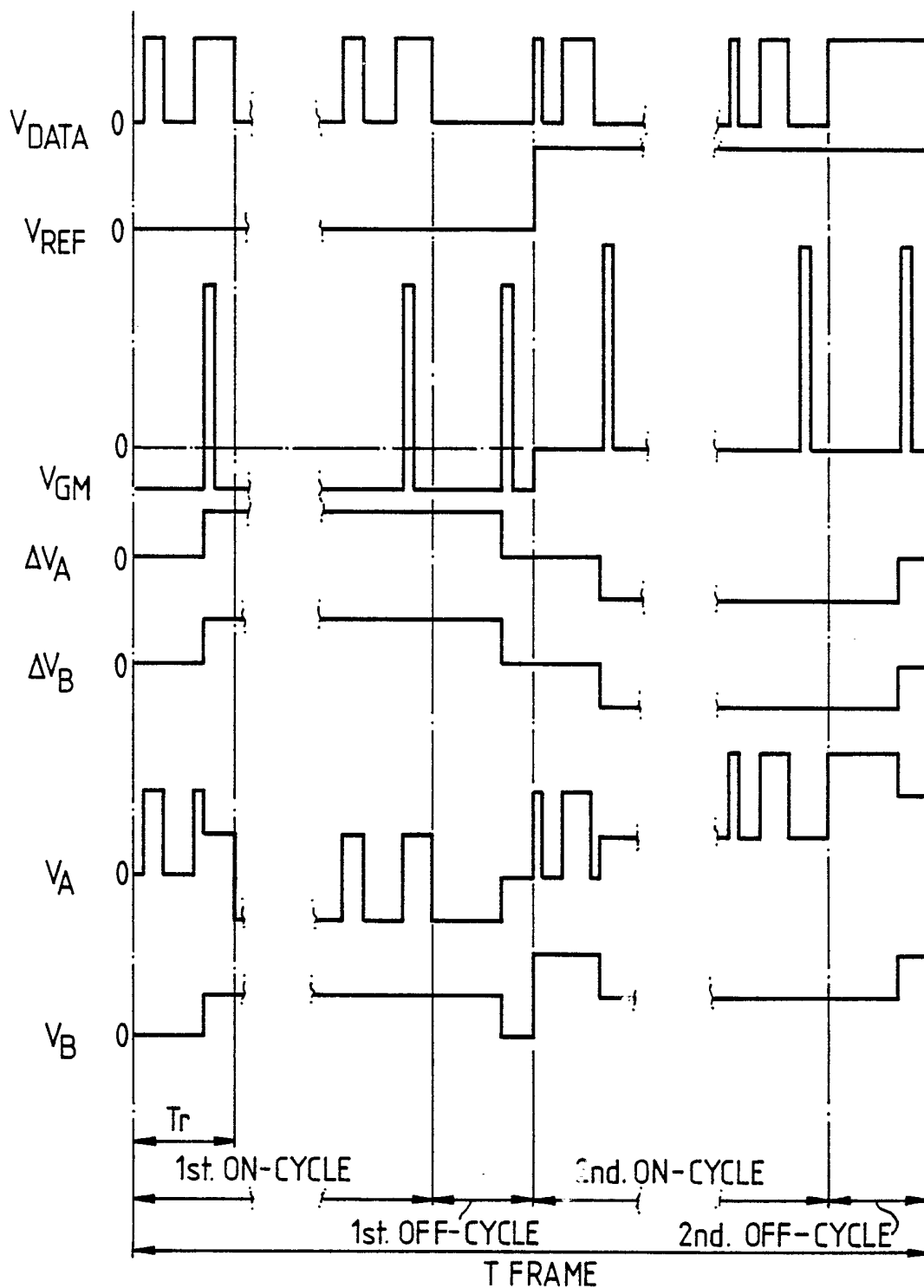


Fig. 6.

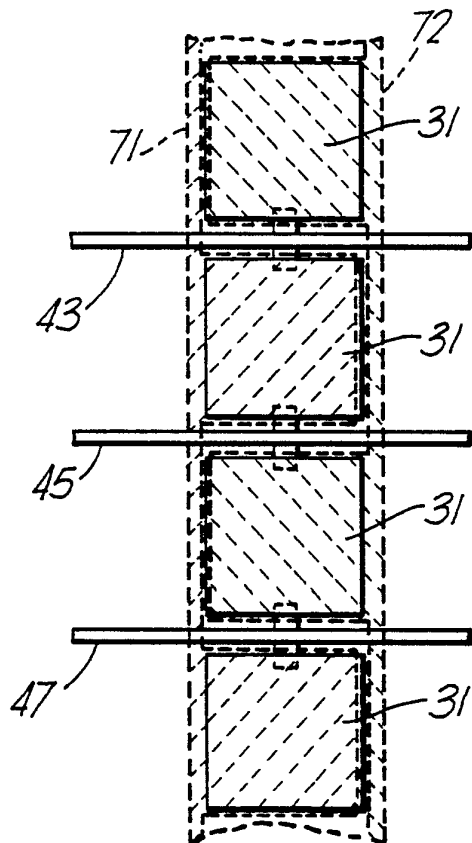
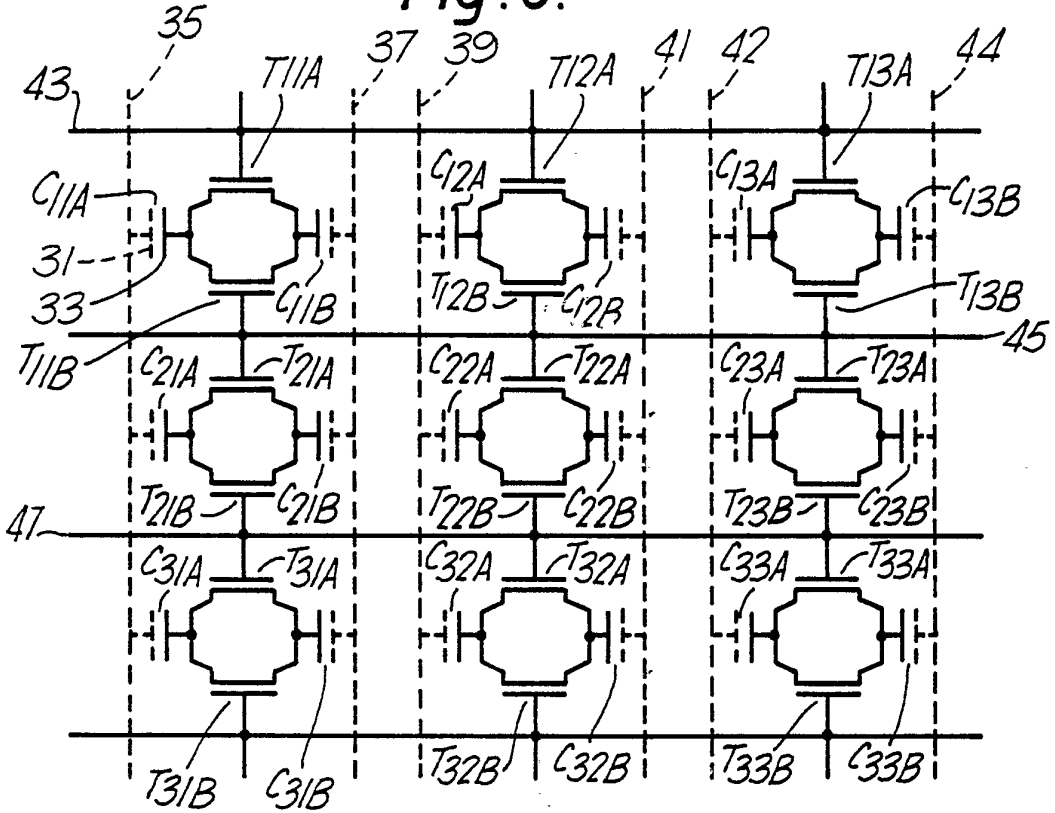


Fig. 7.

6/11

Fig. 8.

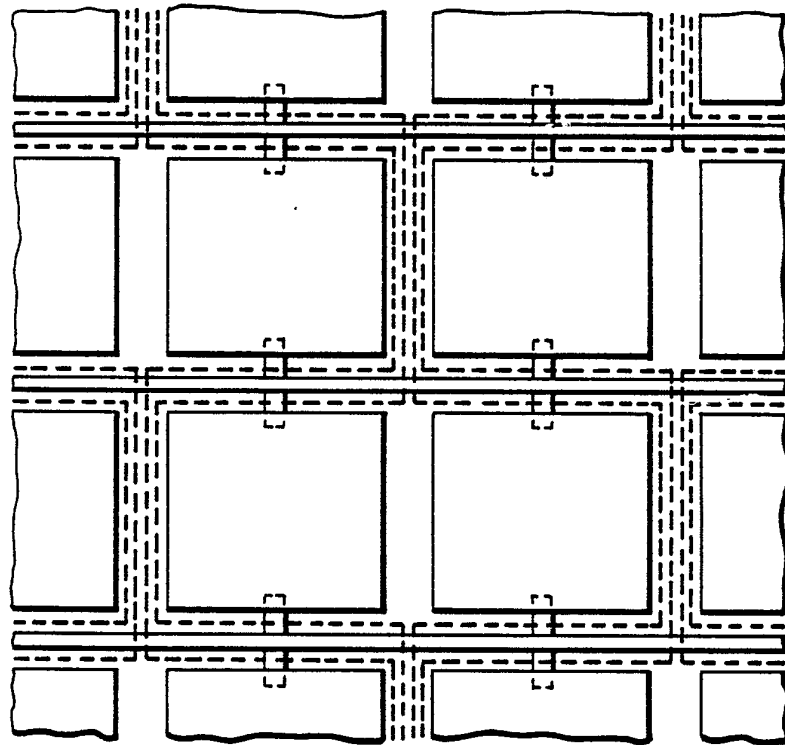
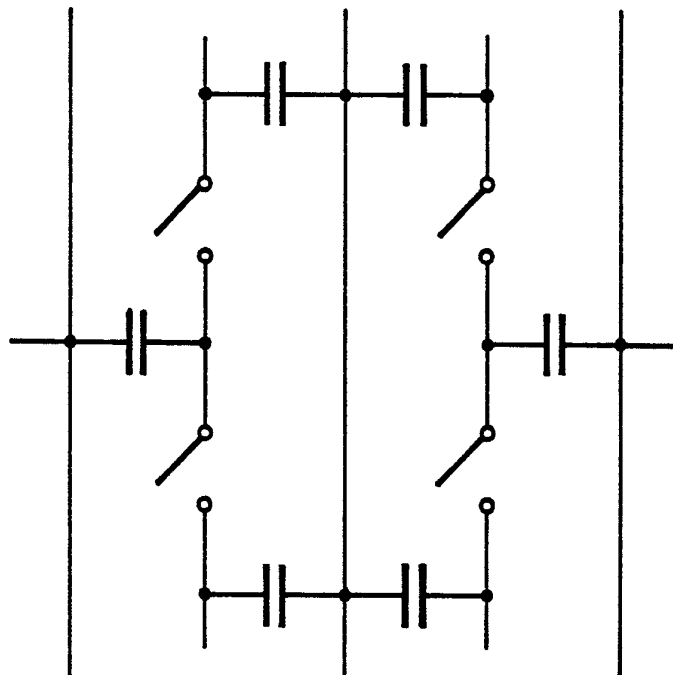


Fig. 9.



2/11

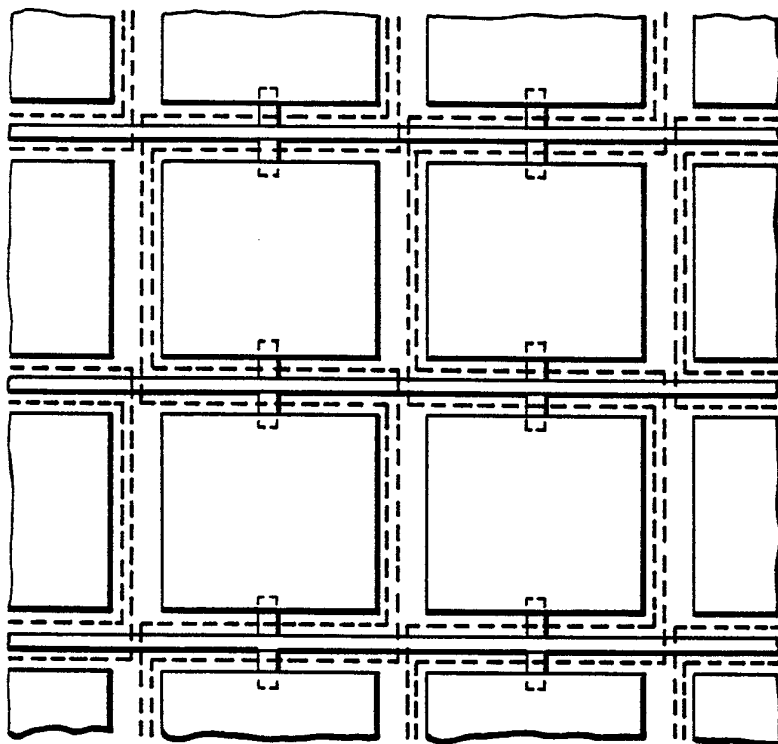


Fig. 10.

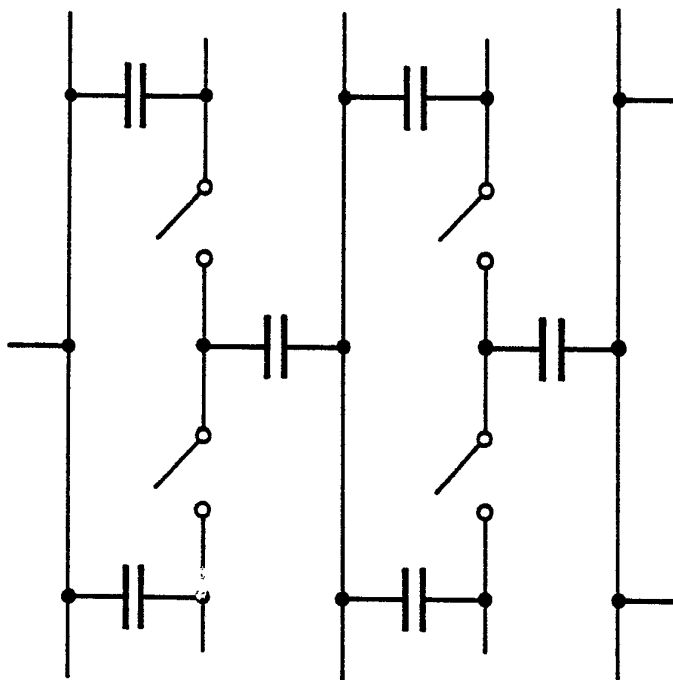


Fig. 11.

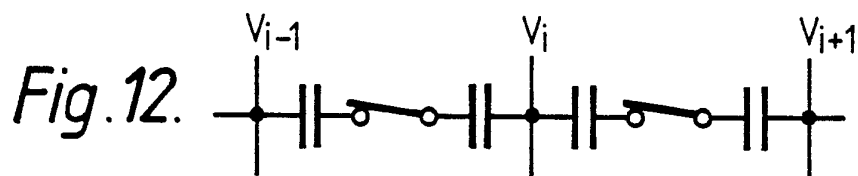


Fig. 12.

Fig. 13.

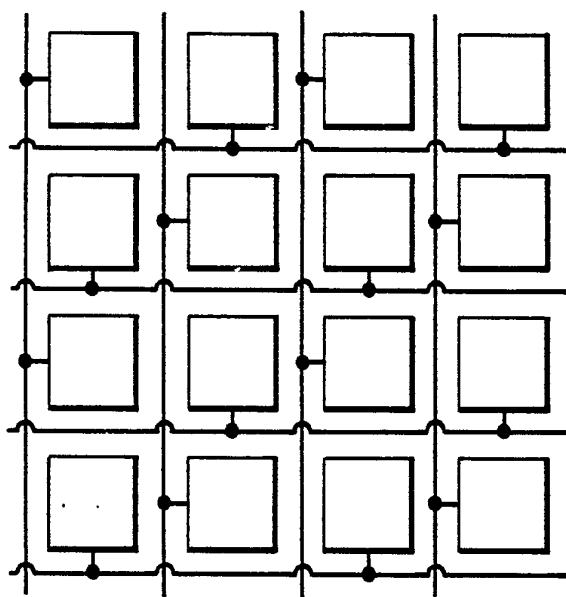
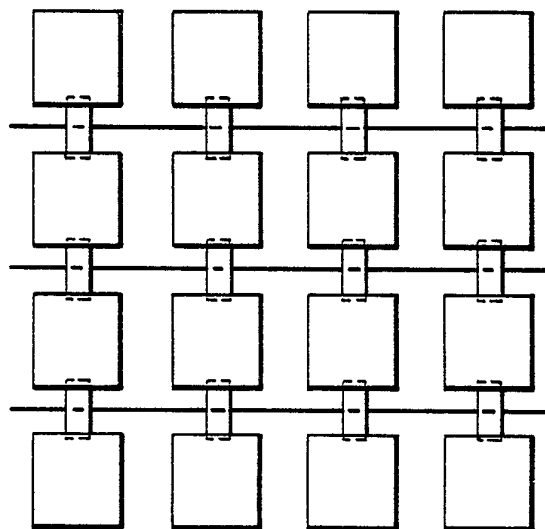
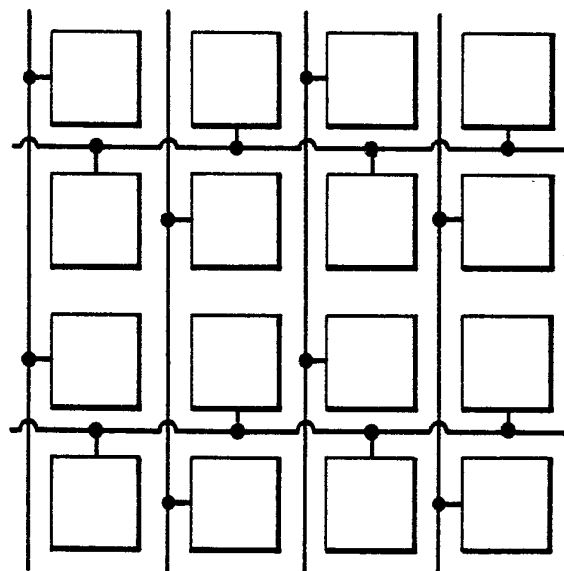


Fig. 14.

Fig. 15.



9/11

Fig. 16.

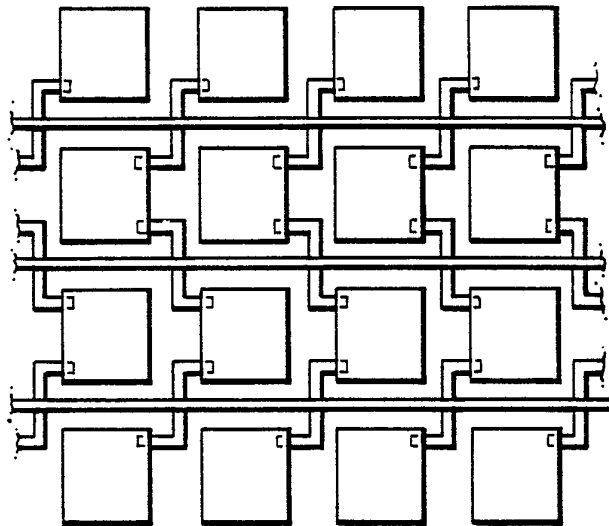
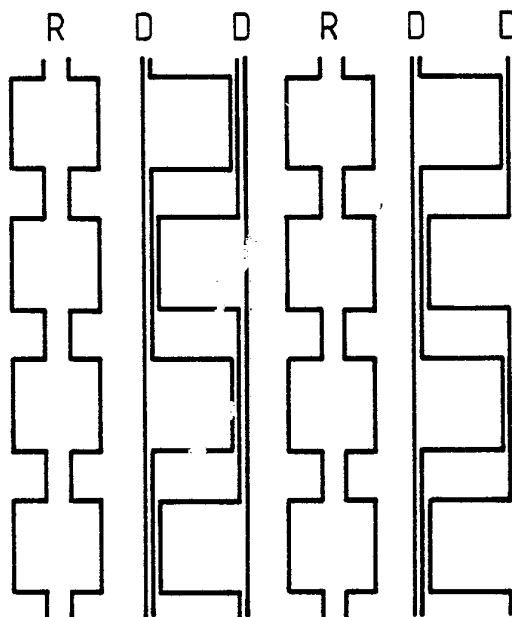


Fig. 17.



10/11

Fig. 18.

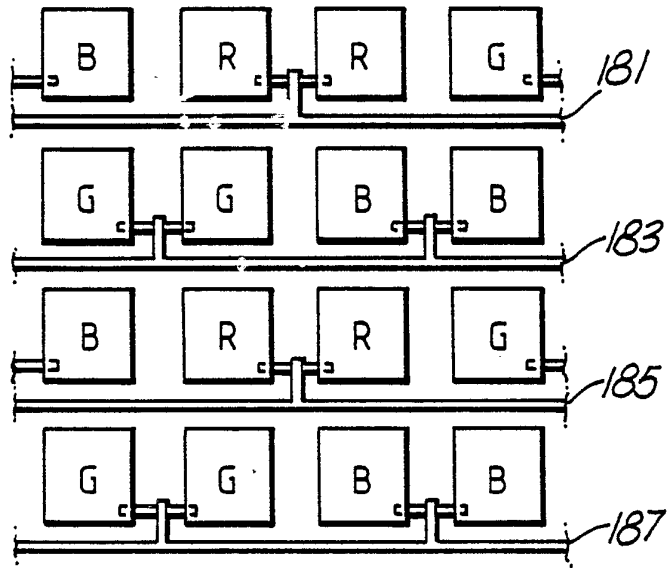
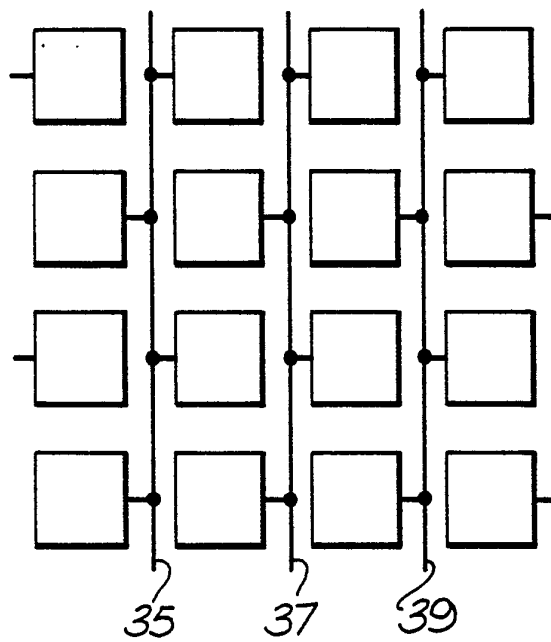


Fig. 19



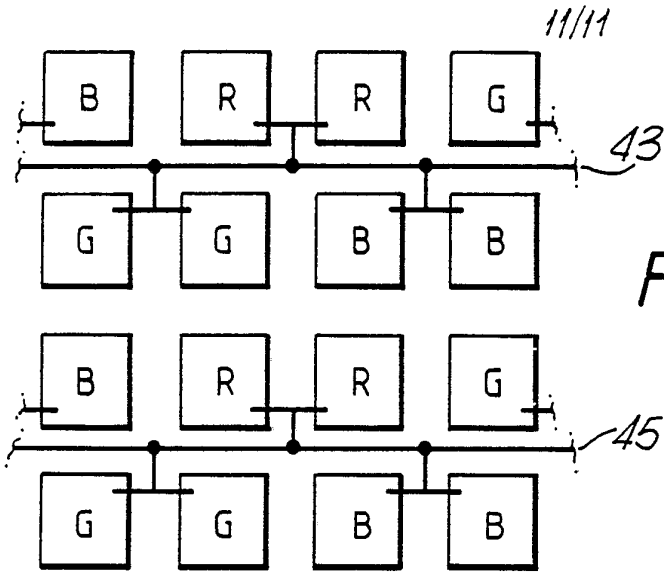


Fig. 21.

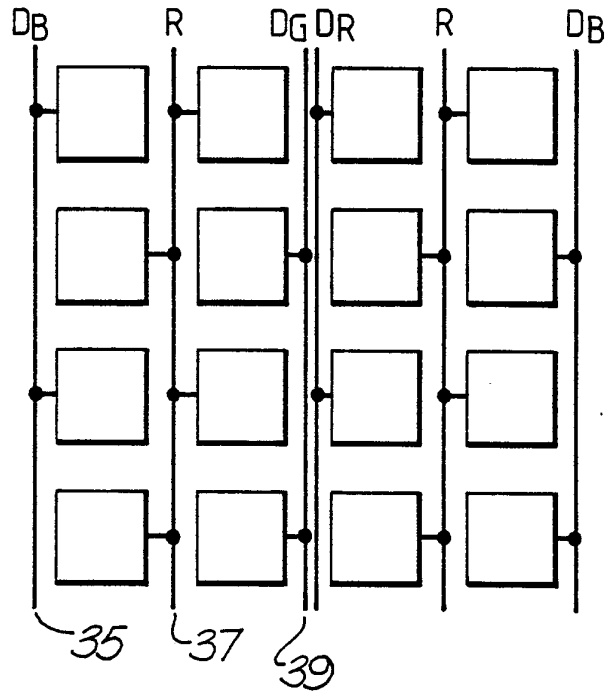
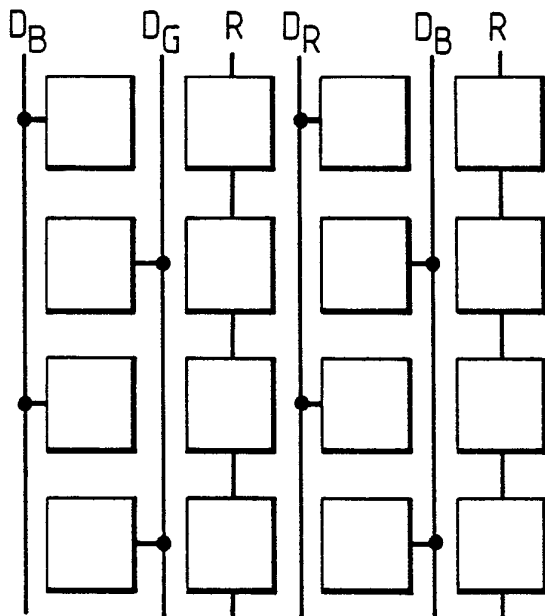
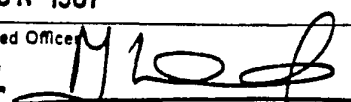


Fig. 22.



# INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 87/00104

<b>I. CLASSIFICATION OF SUBJECT MATTER</b> (if several classification symbols apply, indicate all) *		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC <sup>4</sup> : G 09 G 3/36		
<b>II. FIELDS SEARCHED</b>		
Minimum Documentation Searched <sup>7</sup>		
Classification System	Classification Symbols	
IPC <sup>4</sup>	G 09 G 3/00; G 02 F 1/00	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched <sup>8</sup>		
<b>III. DOCUMENTS CONSIDERED TO BE RELEVANT <sup>9</sup></b>		
Category <sup>9</sup>	Citation of Document, <sup>11</sup> with indication, where appropriate, of the relevant passages <sup>12</sup>	Relevant to Claim No. <sup>13</sup>
E	EP, A, 0202992 (COMMISSARIAT A L'ENERGIE ATOMIQUE) 26 November 1986, see column 1, lines 6-11; column 8, line 38 - column 9, line 17; column 11, lines 34-41; claim 1; figures 2b,3b	1-6,8-14, 20
A	WO, A, 85/02931 (HUGHES AIRCRAFT COMPANY) 4 July 1985, see page 6, line 19 - page 7, line 18; figure 2	1,2,8,10
A	EP, A, 0167408 (SHARP K.K.) 8 January 1986, see claim 1	16,17
-----		
<p>* Special categories of cited documents: <sup>10</sup></p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"Δ" document member of the same patent family</p>		
<b>IV. CERTIFICATION</b>		
Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report	
27th April 1987	09 JUN 1987	
International Searching Authority	Signature of Authorized Officer	
EUROPEAN PATENT OFFICE	M. VAN MOL 	

## ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

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INTERNATIONAL APPLICATION NO. PCT/GB 87/00104 (SA 16108)  
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This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 26/05/87

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0202992	26/11/86	JP-A- 61256330	13/11/86
		FR-A- 2581783	14/11/86
WO-A- 8502931	04/07/85	US-A- 4537471	27/08/85
		EP-A- 0167532	15/01/86
		JP-T- 61500871	01/05/86
EP-A- 0167408	08/01/86	JP-A- 61020092	28/01/86
		JP-A- 61023199	31/01/86

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see Official Journal of the European Patent Office, No. 12/82