



(51) International Patent Classification:

H04R 1/00 (2006.01) H04R 9/04 (2006.01)

H04R 3/04 (2006.01) H04R 9/06 (2006.01)

H03F 3/217 (2006.01)

(21) International Application Number:

PCT/GB2021/050178

(22) International Filing Date:

26 January 2021 (26.01.2021)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

16/777,172 30 January 2020 (30.01.2020) US

(71) Applicant: CIRRUS LOGIC INTERNATIONAL

SEMICONDUCTOR LIMITED [GB/GB]; 7B Nightingale Way, Quartermile, Edinburgh EH3 9EG (GB).

(72) Inventor: LESSO, John Paul; c/o Cirrus Logic International Semiconductor Limited, 7B Nightingale Way, Quartermile, Edinburgh EH3 9EG (GB).

(74) Agent: HOWELL, Matthew; Haseltine Lake Kempner LLP, Redcliff Quay, 120 Redcliff Street, Bristol BS1 6HU (GB).

(81) Designated States (unless otherwise indicated, for every kind of national protection available):

AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(54) Title: LOUDSPEAKER DRIVER SYSTEMS

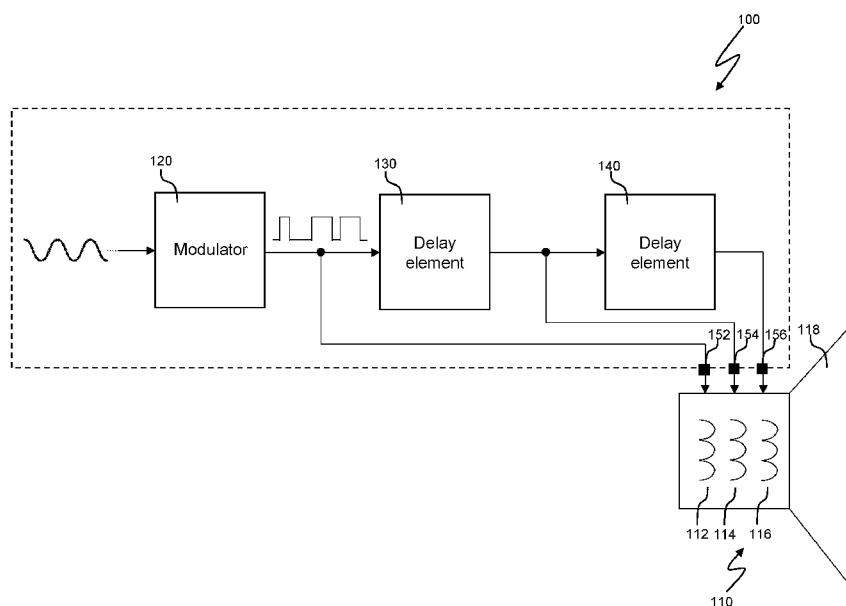


Figure 1

(57) Abstract: A system (100) for driving a loudspeaker (110) having a plurality of coils (112, 114, 116), the system comprising: a modulator (120) configured to receive an input signal and to output a pulse width modulated (PWM) output signal representative of the received input signal; a delay element (130) for receiving and applying a delay to the PWM output signal to generate a first delayed signal; a first output (152) configured to be coupled to a first coil (112) of the plurality of coils of the loudspeaker, wherein the first output is coupled to the output of the modulator (120); and a second output (154) configured to be coupled to a second coil (114) of the plurality of coils of the loudspeaker, wherein the second output is coupled to the output of the delay (130).

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

LOUDSPEAKER DRIVER SYSTEMS

Field of the Invention

5

The present disclosure relates to the field of loudspeaker driver systems. In particular, the present disclosure relates to a system and method for driving a loudspeaker that has a plurality of coils.

Background

10

15

There is a continuing requirement in portable electronic devices such as mobile telephones, tablet and laptop computers, portable speakers, headphones, earphones, earbuds and the like for loudspeaker systems that are capable of producing high volume audio outputs whilst occupying as small a physical volume as possible.

20

One approach to generating high volume audio outputs in portable electronic devices is to use a boosted power supply to drive a relatively large loudspeaker. However, larger loudspeakers suffer from reduced sensitivity, meaning that an increase in the electrical power input to the loudspeaker does not necessarily result in a corresponding increase in the loudness of the audio output produced by the loudspeaker.

25

Another approach is to use two loudspeakers mounted in a back to back configuration. Whilst this may increase the loudness of the audio output produced, a disadvantage of this dual loudspeaker arrangement is that the resistances of the loudspeakers are presented to the loudspeaker driver circuitry in parallel. This arrangement also increases (e.g. doubles) the physical volume occupied by the loudspeakers, which can be problematic in small form factor devices which may lack sufficient space for two loudspeakers.

30

35

Loudspeakers having a plurality of coils are known. In general such multi-coil loudspeakers are used in one of two different configurations. In a first configuration a loudspeaker includes a plurality of different coils, each of which is responsive to input signals in a different frequency band. In a loudspeaker of this type each coil must be driven by a drive signal carrying frequencies in the frequency band of the coil. One way of achieving this is to encode an input audio signal using a pulse density modulator and

to apply appropriate digital filtering to generate a plurality of digital signals corresponding to the respective frequency bands of the coils of the loudspeaker, with each of the plurality of digital signals being used to drive the appropriate one of the loudspeaker coils.

5

A second multi-coil loudspeaker configuration includes a drive coil for driving the cone of the loudspeaker and a sense coil for sensing the amount of excursion of the loudspeaker cone by detecting a current induced in the sense coil as a result of movement of the loudspeaker cone. Loudspeakers of this type are typically coupled to speaker protection
10 systems which monitor the amount of excursion of the speaker cone, as detected by the sense coil, and limit the amplitude of the signal that drives the drive coil in the event that over-excursion of the cone is detected.

A need exists for a system for providing an increase in the loudness of audio output by
15 a single loudspeaker without requiring a boosted power supply.

Summary

According to a first aspect, the invention provides a system for driving a loudspeaker
20 having a plurality of coils, the system comprising:

- a modulator configured to receive an input signal and to output a pulse width modulated (PWM) output signal representative of the received input signal;

- a delay element for receiving and applying a delay to the PWM output signal to generate a first delayed signal;

- 25 a first output configured to be coupled to a first coil of the plurality of coils of the loudspeaker, wherein the first output is coupled to the output of the modulator; and

- a second output configured to be coupled to a second coil of the plurality of coils of the loudspeaker, wherein the second output is coupled to the output of the delay element.

30

The modulator may comprise a class D amplifier, for example.

The input signal may comprise an audio signal.

35 The input signal may comprise a digital signal and the modulator may comprise a digital modulator.

The modulator and the delay element may be configured to receive a clock signal.

The delay element may comprise a clocked buffer.

5

The delay element may alternatively comprise a counter.

The delay element may further comprise an edge detector and an edge generator, wherein:

10 the edge detector is configured to detect an edge of an input PWM signal and to trigger the counter on detection of the edge;

 the counter is configured to count pulses of the clock signal until a predetermined number is reached and to output a signal to the edge generator when the predetermined number is reached; and

15 the edge generator is configured to output a delayed and inverted version of the input PWM signal in response to receiving the signal from the counter.

The delay element may be configured to apply a delay equal to one period of the output PWM signal to the output PWM signal.

20

The delay element may form at least part of a finite impulse response (FIR) filter arrangement.

The FIR filter arrangement may be configured to receive a configuration signal and, based on the configuration signal, to adapt in response to a variation in a frequency of the PWM output signal output.

25

The FIR filter arrangement may be operative, in response to the configuration signal, to adjust a predetermined value used by a counter of the FIR filter arrangement.

30

The FIR filter arrangement may be configured to suppress a carrier of the PWM output signal.

The FIR filter arrangement may be configured to provide a zero at a carrier frequency of the PWM output signal.

35

A carrier frequency of the PWM output signal may be modulated based on a control signal.

The control signal may be based on an operating mode of the system or on an input
5 signal level of the input signal.

According to a second aspect the invention provides an integrated circuit comprising a system according to the first aspect.

10 According to a third aspect the invention provides a device comprising a system according to the first aspect, wherein the device comprises a portable device, battery powered device, a mobile telephone a notebook, laptop or tablet computing device a smartwatch or an accessory device.

15 According to a fourth aspect the invention provides a method for driving a loudspeaker having a plurality of coils, the method comprising:

receiving an input signal and outputting a pulse width modulated (PWM) output signal representative of the received input signal; and

20 applying a delay to the PWM output signal to generate a first delayed signal;
outputting the PWM modulated output signal to a first coil of the plurality of coils;
and

outputting the first delayed signal to a second coil of the plurality of coils.

The method according may comprise modulating the input signal with a class D amplifier
25 to generate the PWM output signal.

The input signal may comprise an audio signal, for example.

The input signal may comprise a digital signal and the method may comprise modulating
30 the input signal with a digital modulator to generate the PWM output signal.

The method may further comprise synchronising the modulated PWM output signal and the first delayed signal to a clock signal.

35 The delay may be applied to the PWM output signal using a clocked buffer.

The delay may alternatively be applied to the PWM output signal using a counter.

Applying the delay may comprise:

- 5 detecting an edge of an input PWM signal and triggering the counter on detection of the edge;
- counting pulses of the clock signal until a predetermined number is reached; and
- outputting a delayed and inverted version of the input PWM signal in response to receiving a signal from the counter indicating that the predetermined number has been reached.

10

The delay may be equal to one period of the output PWM signal to the output PWM signal.

According to a fifth aspect the invention provides a system for driving a loudspeaker having a plurality of coils, the system comprising:

15

- a modulator for receiving an input signal and outputting a first PWM output signal for driving a first coil of the plurality of coils;
- a finite impulse filter (FIR) arrangement for receiving the PWM output signal and to outputting a second PWM output signal for driving a second coil of the plurality of coils,
- 20 wherein the FIR arrangement is configured to adapt to a variation in a frequency of the PWM output signal output so as to suppress a carrier of the PWM output signal.

20

According to a sixth aspect the invention provides a system for driving a transducer having a plurality of coils, the system comprising:

25

- a modulator for outputting a digital output signal representative of a received analogue input signal at a modulator output;
- a clock controlled delay element for applying a delay to the digital output signal to generate a first delayed signal at a delay element output;
- wherein the modulator output is couplable to a first coil of the plurality of the coils
- 30 of the transducer and the delay element output is couplable to a second coil of the plurality of coils of the transducer.

30

The system may further comprise a clock signal generator operative to generate a clock signal for the clock controlled delay element.

35

According to a seventh aspect the invention provides an integrated circuit comprising the system of the sixth aspect.

According to an eighth aspect the invention provides a system for driving a transducer,
5 the system comprising:

a modulator for outputting a digital output signal representative of a received analogue input signal at a modulator output;

a delay element for applying a delay to the digital output signal to generate a first delayed signal at a delay element output;

10 a first inductor having a first terminal coupled to the modulator output; and

a second inductor having a first terminal coupled to the delay element output,

wherein a second terminal of the first inductor is coupled to a second terminal of the second inductor to provide an output node for a drive signal to drive the transducer.

15 The first inductor and the second inductor may comprise first and second coils of the transducer.

The transducer may comprise a loudspeaker, for example.

20 According to a ninth aspect the invention provides a module comprising the system of the eighth aspect and a transducer.

According to a tenth aspect the invention provides an integrated circuit according to the eighth aspect.

25

Brief Description of the Drawings

Embodiments of the invention will now be described, strictly by way of example only, with reference to the accompanying drawings, of which:

30

Figure 1 is a schematic representation of a system for driving a loudspeaker having a plurality of coils;

Figure 2 is a simplified schematic representation of a FIR DAC;

35

Figure 3 is a schematic representation of a system for driving a loudspeaker having a plurality of coils which uses a class D amplifier to generate a pulse width modulated signal to drive the coils of the loudspeaker;

- 5 Figure 4 is a schematic representation of a system for driving a loudspeaker having a plurality of coils which uses a digital modulator to generate a pulse width modulated signal to drive the coils of the loudspeaker;

Figure 5 is a schematic representation of a digital delay unit;

10

Figure 6 is a schematic representation of a digital delay implemented using a counter;

Figure 7 is a schematic representation of a system for driving a loudspeaker having a plurality of coils which uses a digital modulator to generate a pulse width modulated signal to drive the coils of the loudspeaker, in which a PWM repetition signal is variable;

15

Figure 8 is a schematic representation of a system for driving a multi-coil transducer;

Figure 9 is a schematic representation of a system for driving a single-coil loudspeaker; and

20

Figure 10 is a schematic representation of a system for driving a single-coil transducer.

Detailed Description

- 25 Referring to **Figure 1**, a system for driving a loudspeaker having a plurality of coils (also referred to as a multi-coil loudspeaker) is shown generally at 100. The system 100 illustrated in Figure 1 is configured to drive a loudspeaker 110 having first, second and third coils 112, 114, 116, but it will be appreciated that the principles described here are applicable to multi-coil loudspeakers having any number of coils.

30

The system 100 includes a modulator 120 which is configured to receive an analogue input signal such as an audio signal and convert it to a pulse width modulated (PWM) output signal. The modulator 120 may be a class D modulator, for example. The modulator 120 may be implemented, for example, in circuitry (e.g. discrete circuitry or
35 integrated circuitry) or by processing circuitry (e.g. a digital signal processor) executing appropriate software code.

An output of the modulator 120 is coupled to an input of a first delay element 130 such that the PWM signal output by the modulator 120 is input to the first delay element 130. The output of the modulator 120 is also connected to a first output terminal 152 of the system 100, which is configured to be coupled to the first coil 112 of the loudspeaker 110, such that the PWM signal that is output by the modulator 120 is also input to the first coil 112 of the loudspeaker 110 when the loudspeaker is coupled to the system 100.

The first delay element 130 is configured to apply a delay to the input PWM signal and to output a delayed version of the PWM signal.

An output of the first delay element 130 is coupled to an input of a second delay element 140 such that the delayed version of the PWM signal output by the first delay element 130 is input to the second delay element 140. The output of the first delay element 130 is also connected to a second output terminal 154 that is configured to be coupled to the second coil 114 of the loudspeaker 110, such that the delayed version of the PWM signal that is output by the first delay element 130 is also input to the second coil 114 of the loudspeaker 110.

The second delay element 140 is configured to apply a further delay to the input PWM signal and to output a further delayed version of the PWM signal. An output of the second delay element 140 is connected to a third output terminal 156 that is configured to be coupled to the third coil 116 of the loudspeaker 110, such that the further delayed version of the PWM signal that is output by the second delay element 140 is input to the third coil 116 of the loudspeaker 110.

The first and second delay elements may be implemented, for example, in discrete or integrated circuitry, or in processing circuitry executing suitable software code. Where the delay elements are implemented in integrated circuitry, they may be integrated with the modulator circuitry in a single integrated circuit (IC), or alternatively may be integrated together as a standalone IC. Alternatively, each delay element may be integrated as a separate IC.

As will be appreciated by those skilled in the art, the combination of the first and second delay elements 130, 140, first, second and third coils 112, 114, 116 and cone 118 of the

loudspeaker 110 acts as a FIR DAC (Finite Impulse Response Digital to Analogue Converter), as will now be explained with reference to Figure 2.

As shown generally at 200 in **Figure 2**, a FIR DAC typically comprises a plurality (in this example three) of digital delay elements 202, 204, 206. A first one of the digital delay elements 202 is configured to receive a digital signal at its input, to apply a delay to the received digital signal, and to output a first delayed digital signal to a second one of the digital delay elements 204. The first delayed digital signal is also output to a first digital to analogue converter (DAC) 208.

The second digital delay element 204 is configured to receive the first delayed digital signal at its input, to apply a delay to the received first delayed digital signal, and to output a second delayed digital signal to a third one of the digital delay elements 206. The second delayed digital signal is also output to a second DAC 210.

The third digital delay element 206 is configured to receive the second delayed digital signal at its input, to apply a delay to the received second delayed digital signal, and to output a third delayed digital signal to a third DAC 212.

The first, second and third DACs 208, 210, 212 are configured to convert the received first, second and third delayed digital signals into respective first, second and third analogue signals, and to output the first, second and third analogue signals to a summation unit 214. The summation unit 214 sums the received first, second and third analogue signals and outputs the result of this summation as an analogue output signal.

As will be appreciated, the combination of the digital delay elements 202, 204, 206, the DACs 208, 210, 212 and the summation unit 214 performs the functions of a finite impulse response filter and a digital to analogue converter, such that the analogue output signal constitutes a filtered analogue version of the digital input signal.

In the system 100 of Figure 1, the delay elements 130, 140 perform the digital delay function of a FIR DAC, whilst the coils 112, 114, 116 of the loudspeaker 110 (in combination with any additional filtering components associated with the coils 112, 114, 116) perform digital to analogue conversion of the digital signals input to the coils 112, 114, 116. The function of summing the analogue signals is performed by the cone 118 of the loudspeaker 110, whose movement is governed by the combination of the

magnetic fields generated by the coils 112, 114, 116, and thus outputs an analogue audio signal that represents the sum of the analogue signals generated by the coils 112, 114, 116.

5 The arrangement of the delay elements 130, 140, the coils 112, 114, 116 and the cone 118 in a FIR DAC configuration helps to reduce the effect of out-of-band signals (i.e. signals outside of the audio frequency band) and jitter in the audio signal output by the loudspeaker 110. For example, the FIR DAC arrangement helps to suppress a carrier signal of the PWM signal output by the modulator 120.

10

The PWM signal may be generated in a number of different ways. For example, the modulator 120 may be a class D amplifier, as will now be described with reference to Figure 3.

15 The system illustrated in **Figure 3** includes similar components to the system of Figure 1, so like reference signs have been used to denote like components in Figures 1 and 3. The system 300 of Figure 3 includes a class D amplifier 310, made up of a comparator 312, a carrier signal generator 314, a first switching device 316 and a second switching device 318. The class D amplifier 310 may be implemented as discrete circuitry, or
20 alternatively may be implemented as integrated circuitry. The class D amplifier 310 in this example is configured to receive an analogue input signal and to output at an output 320 thereof a PWM output signal, in a manner that will be familiar to those skilled in the art, but it will be appreciated that a digital class D amplifier could be used where the input signal is a digital signal.

25

The output 320 of the class D amplifier 310 is coupled to the first delay element 130 and is also connected to a first output terminal 152 of the system 300, which is configured to be coupled to the first coil 112 of the loudspeaker 110, such that the PWM signal that is output by the modulator 310 to the first delay element 320 is also input to the first coil
30 112 of the loudspeaker 110 when the loudspeaker is coupled to the system 300. The first delay element 130 outputs a first delayed version of the PWM signal that is output by the class D amplifier to a second output terminal 154 that is configured to be coupled to the second coil 114 and to the second delay element 140, and the second delay element 140 outputs a second delayed version of the PWM signal that is output by the
35 class D amplifier to a third output terminal 156 that is configured to be coupled to the third coil 116, as described above with reference to Figure 1.

Figure 4 is a schematic representation of a system 400 for driving a multi-coil loudspeaker having a plurality of coils which uses a digital modulator to generate a pulse width modulated signal to drive the coils of the loudspeaker. The system illustrated in
5 Figure 4 includes similar components to the systems of Figures 1 and 3, so like reference signs have been used to denote like components in Figures 1, 3 and 4.

The system illustrated in Figure 4 includes a digital modulator 410 having an input 420 and an output 430. A digital input signal D_{IN} (e.g. a digital audio signal) is received at the
10 input 420, and a PWM output signal representing the digital input signal D_{IN} is output at the output 430. The output 430 of the digital modulator 410 is coupled to a first delay element 130 and to a first output terminal 152 of the system 400, which is configured to be coupled to a first coil 112 of a multi-coil loudspeaker 110. The first delay element 130 outputs a first delayed version of the PWM output by the digital modulator 400 to a
15 second output terminal 154, which is configured to be coupled to a second coil 114 of the multi-coil loudspeaker 110.

For simplicity, the loudspeaker 110 is shown as having two coils, but it will be appreciated that the loudspeaker 110 could include more than two coils.
20

In the system illustrated in Figure 4 a clock signal CLK with a frequency F_s (generated by a clock of a host device in which the system 400 is provided, for example) is received by the digital modulator 410 and the first delay element 130 to ensure synchronous operation of the digital modulator 410 and the first delay element 130.
25

In operation of the system a delay $\beta - \alpha$ between the output 430 (α) of the digital modulator 410 and the output (β) of the first delay element 130 may be large, relative to the frequency F_s of the clock signal CLK. For example, the frequency F_s of the clock signal CLK may be 6.144MHz, whereas the PWM repetition (carrier) frequency may be 384kHz.
30 Thus in this example in order to filter the PWM carrier frequency from the output of the first delay element 130 the delay imposed by the first delay element 130 should be one PWM period of the PWM signal output by the digital modulator 410, i.e. $1/384\text{kHz} \approx 2.6\mu\text{s}$. In the example illustrated in Figure 4 the first delay element 130 delays the input signal by one PWM period and inverts it.

35

The delay elements 130, 140 described above may be implemented in a number of different ways. In one example, illustrated in **Figure 5**, a simple delay element may comprise one or more clocked buffers.

- 5 Alternatively, a delay element may be more efficiently realised as a counter that counts up to a predetermined number before toggling the output. **Figure 6** is a schematic representation of such a delay element.

10 The delay element 600 of Figure 6 is a digital delay element that comprises an edge detector 610, a counter 620 and an edge generator 630.

15 The edge detector 610 is configured to receive an input PWM signal (e.g. the PWM signal output by the modulator 120, 300 or 410 of Figure 1, 3 or 4). On detection of an edge of the input PWM signal, e.g. a rising edge, the edge detector 610 outputs a signal to the counter 620 to cause the counter 620 to commence counting clock pulses of the clock signal CLK. The counter 620 continues counting pulses until a predetermined number, equal to the number of clock pulses in one period of the input PWM signal (e.g. $2.6\mu\text{s} \times 6.144\text{MHz} = 16$) has been reached.

20 For example, where the PWM repetition frequency is 384kHz and the frequency F_s of the clock signal CLK is 6.144MHz as described above, one period of the PWM signal will last approximately $2.6\mu\text{s}$, so the predetermined number of clock pulses is 16 (i.e. $2.6\mu\text{s} \times 6.144\text{MHz} = 16$).

25 When the predetermined number has been reached a signal is output by the counter 620 to the edge generator 630, which outputs an inverted and delayed version of the input PWM signal as an output PWM signal. For example, where the counter 620 was triggered by detection of a rising edge of the input PWM input signal, the edge generator 630 will output a delayed version of the input PWM signal commencing with a falling
30 edge as the output PWM signal.

In general the PWM repetition frequency may be varied. For example, the PWM repetition frequency may be reduced to save power when the modulator is idling. The delay element(s) which make up the FIR filter of the system may thus be reconfigurable
35 to adapt to different PWM repetition frequencies.

Figure 7 is a schematic representation of a system 700 for driving a multi-coil loudspeaker which uses a digital modulator to generate a pulse width modulated signal to drive the coils of the loudspeaker, in which a PWM repetition signal is variable. The system 700 illustrated in Figure 7 includes similar components to the system of Figure 4, so like reference signs have been used to denote like components in Figures 4 and 7.

The system 700 of Figure 7 includes a digital modulator 410 of the kind described above with reference to Figure 4, which outputs a PWM output signal to a FIR filter arrangement 710, which may comprise, for example, one or more delay elements of the kind described above with reference to Figures 1-6. The FIR filter arrangement outputs a plurality of signals to output terminals 720 of the system 700, which are configured to be coupled to the coils of a multi-coil loudspeaker 110, each of the plurality of signals driving a different coil 112, 114, 116 of the multi-coil loudspeaker 110.

The FIR filter arrangement 710 receives a configuration signal Config which may be provided, for example, by the digital modulator 400 or by a controller of a host device incorporating the system 700. The configuration signal causes the FIR filter arrangement 710 to adapt or reconfigure in response to a variation in the PWM repetition frequency of the PWM signal output by the modulator 410, e.g. by adjusting the predetermined value used by a counter of the FIR filter arrangement, thus to accommodate the variation in the PWM repetition frequency.

The FIR filter arrangement 710 may be optimised to suppress a carrier of the PWM signal. For example the FIR filter arrangement 710 may be configured to provide a zero at the PWM carrier frequency. The PWM carrier frequency may be modulated based on some control signal, which may be based, for example, on an operating mode (e.g. high power/low power) of the system 700 or on an input signal level of the input signal D_{IN} . The FIR filter arrangement 710 is reconfigurable to adapt to changes in the PWM carrier frequency in response to the configuration signal Config.

The discussion above relates to driving a multi-coil loudspeaker. However, those skilled in the art will readily appreciate that the principles discussed above are equally applicable to other multi-coil transducers.

Figure 8 is a schematic representation of a system for driving a multi-coil transducer (i.e. a transducer having a plurality of coils). The system 800 illustrated in Figure 8 is

configured to drive a loudspeaker 810 having first and second coils 812, 814, but it will be appreciated that the principles described here are applicable to multi-coil transducers having any number of coils.

- 5 The system 800 includes a modulator 820 which is configured to receive an analogue input signal such as an audio signal and convert it to a digital output signal, e.g. a pulse width modulated (PWM) signal. The modulator 820 may be, for example, an asynchronous or self-oscillating PWM modulator. The modulator 820 may be a class D modulator, for example. The modulator 820 may be implemented, for example, in
10 circuitry (e.g. discrete circuitry or integrated circuitry) or by processing circuitry (e.g. a digital signal processor) executing appropriate software code.

An output of the modulator 820 is coupled to an input of a clock controlled delay element 830 such that the digital signal output by the modulator 820 is input to the clock controlled
15 delay element 830. The output of the modulator 820 is also connected to a first output terminal 852 of the system 800, which is configured to be coupled to the first coil 812 of the transducer 810, such that the digital signal that is output by the modulator 820 is also input to the first coil 812 of the transducer 810 when the transducer 810 is coupled to the system 800.

20

The clock controlled delay element 830 is configured to apply a delay to the input digital signal and to output a delayed version of the digital signal. The clock controlled delay element 830 may comprise, for example, a clocked buffer or a digital delay element of the kind described above with reference to Figures 5 and 6.

25

An output of the clock controlled delay element 830 is coupled to a second output terminal 854 of the system 800, which is configured to be coupled to the second coil 814 of the transducer 810, such that the delayed version of the digital signal output by the modulator 820 that is output by the clock controlled delay element 830 is input to the
30 second coil 814 of the loudspeaker 810.

The system 800 further includes a clock signal generator 840, operative to generate and output a clock signal to the clock controlled delay element 830.

- 35 The clock controlled delay element 830 may be implemented, for example, in discrete or integrated circuitry, or in processing circuitry executing suitable software code. Where

the clock controlled delay element 830 is implemented in integrated circuitry, it may be integrated with the modulator circuitry in a single integrated circuit (IC), or alternatively may be integrated together as a standalone IC. Alternatively, the clock controlled delay element 830 may be integrated as a separate IC.

5

In the example illustrated in Figure 8, one clock controlled delay element 830 is provided, but it will be appreciated that more a plurality of such delay elements could be provided, with an output of each delay element supplying a delayed version of the digital signal output by the modulator 820 to a different coil of a multi-coil transducer.

10

As will be appreciated by those skilled in the art, the combination of the clock controlled delay element 830 and the first and second 812, 814 coils of the transducer 810 acts as a FIR DAC (Finite Impulse Response Digital to Analogue Converter), in the manner described above with reference to Figure 2.

15

The present disclosure also extends to systems (e.g. circuitry) for driving a loudspeaker or other transducer having a single coil.

Figure 9 is a schematic representation of a system 900 for driving a single-coil loudspeaker 910.

20

The system 900 includes a modulator 920 which is configured to receive an analogue input signal such as an audio signal and convert it to a digital (e.g. PWM) output signal. The modulator 920 may be a class D modulator, and/or an asynchronous or self-oscillating PWM modulator for example. The modulator 920 may be implemented, for example, in circuitry (e.g. discrete circuitry or integrated circuitry) or by processing circuitry (e.g. a digital signal processor) executing appropriate software code.

25

An output of the modulator 920 is coupled to an input of a first delay element 930 such that the PWM signal output by the modulator 920 is input to the first delay element 930. The output of the modulator 920 is also coupled to a first terminal of a first inductor 950 of the system 900.

30

The first delay element 930 is configured to apply a delay to the input digital signal and to output a delayed version of the digital signal. An output of the first delay element 930 is coupled to an input of a second delay element 940 such that the delayed version of

35

the digital signal output by the first delay element 930 is input to the second delay element 940. The output of the first delay element 930 is also coupled to a first terminal of a second inductor 960.

- 5 The second delay element 940 is configured to apply a further delay to the input digital signal and to output a further delayed version of the digital signal. An output of the second delay element 940 is coupled to a first terminal of a third inductor 970.

10 The first and second delay elements may be implemented, for example, in discrete or integrated circuitry, or in processing circuitry executing suitable software code. Where the delay elements are implemented in integrated circuitry, they may be integrated with the modulator circuitry in a single integrated circuit (IC), or alternatively may be integrated together as a standalone IC. Alternatively, each delay element may be integrated as a separate IC.

15 Second terminals of the first, second and third inductors 950, 960, 970 are coupled together and to an output terminal or node 980 of the system 900, which is configured to be coupled to an input terminal of the loudspeaker 910. Thus the output terminal or node 980 provides an output node for a drive signal to drive the transducer 910.

20 As will be appreciated by those skilled in the art, the combination of the first and second delay elements 930, 940, first, second and third inductors 950, 960, 970 and a cone 912 of the loudspeaker 910 acts as a FIR DAC (Finite Impulse Response Digital to Analogue Converter), as explained above with reference to Figure 2.

25 The system 900 may be implemented as a single integrated circuit, in which case the inductors 950, 960, 970 may be embedded or on-chip inductors. Alternatively, the system 900 may be implemented as a module comprising one or more integrated circuits implementing the modulator 920 and delay elements 930, 940 mounted on a substrate
30 such as a printed circuit board (PCB), with the inductors 950, 960, 970 also being mounted on the substrate externally of the integrated circuit(s). In some examples the loudspeaker 910 may also be mounted on the substrate so as to form part of the module. Alternatively, the loudspeaker may be provided separately and thus may not form part of the module.

35

Figure 10 is a schematic representation of a system for driving a single-coil transducer.

The system 1000 includes a modulator 1020 which is configured to receive an analogue input signal such as an audio signal and convert it to a digital output signal, e.g. a pulse width modulated (PWM) signal. The modulator 1020 may be, for example, an asynchronous or self-oscillating PWM modulator and/or a class D modulator, for example. The modulator 1020 may be implemented, for example, in circuitry (e.g. discrete circuitry or integrated circuitry) or by processing circuitry (e.g. a digital signal processor) executing appropriate software code.

10 An output of the modulator 1020 is coupled to an input of a clock controlled delay element 1030 such that the digital signal output by the modulator 1020 is input to the clock controlled delay element 1030. The output of the modulator 1020 is also connected to a first output terminal 1052 of the system 1000, which is configured to be coupled to a first terminal of a first inductor 1060.

15 The clock controlled delay element 1030 is configured to apply a delay to the input digital signal and to output a delayed version of the digital signal. The clock controlled delay element 1030 may comprise, for example, a clocked buffer or a digital delay element of the kind described above with reference to Figures 5 and 6.

20 An output of the clock controlled delay element 1030 is coupled to a second output terminal 1054 of the system 1000, which is configured to be coupled to a first terminal of a second inductor 1060.

25 Second terminals of the first and second inductors 1060, 1070 are coupled together and to an output terminal or node 1052 of the system 1000, which is configured to be coupled to an input terminal of the transducer 1010. Thus the output terminal or node 1052 provides an output node for a drive signal to drive the transducer 1010.

30 The clock controlled delay element 1030 may be implemented, for example, in discrete or integrated circuitry, or in processing circuitry executing suitable software code. Where the clock controlled delay element 1030 is implemented in integrated circuitry, it may be integrated with the modulator circuitry in a single integrated circuit (IC), or alternatively may be integrated together as a standalone IC. Alternatively, the clock controlled delay
35 element 1030 may be integrated as a separate IC.

The system 1000 further includes a clock signal generator 1040, operative to generate and output a clock signal to the clock controlled delay element 1030.

5 In the example illustrated in Figure 10, one clock controlled delay element 1030 is provided, but it will be appreciated that more a plurality of such delay elements could be provided, with an output of each delay element supplying a delayed version of the digital signal output by the modulator 1020 to a different inductor.

10 As will be appreciated by those skilled in the art, the combination of the clock controlled delay element 1030, the first and second inductors 1060, 1070 and the transducer 1010 acts as a FIR DAC (Finite Impulse Response Digital to Analogue Converter), in the manner described above with reference to Figure 2.

15 The system 1000 may be implemented as an integrated circuit, in which case the inductors 1060, 1070 may be embedded or on-chip inductors. Alternatively, the system 1000 may be implemented as a module comprising one or more integrated circuits implementing the modulator 1020, clock controlled delay elements 1030 and clock 1040 mounted on a substrate such as a printed circuit board (PCB), with the inductors 1060, 1070 also being mounted on the substrate externally of the integrated circuit(s). In some
20 examples the transducer 1010 may also be mounted on the substrate so as to form part of the module. Alternatively, the transducer 1010 may be provided separately and thus may not form part of the module.

25 Embodiments may be implemented in a range of applications and in particular are suitable for audio applications.

Embodiments may be implemented as an integrated circuit which in some examples could be a codec or audio DSP or similar. Embodiments may be incorporated in an electronic device, which may for example be a portable device and/or a device operable
30 with battery power. The device could be a communication device such as a mobile telephone or smartphone or similar. The device could be a computing device such as a notebook, laptop or tablet computing device. The device could be a wearable device such as a smartwatch. The device could be a device with voice control or activation functionality. In some instances the device could be an accessory device such as a
35 headset or the like to be used with some other product.

The skilled person will recognise that some aspects of the above-described apparatus and methods, for example the discovery and configuration methods may be embodied as processor control code, for example on a non-volatile carrier medium such as a disk, CD- or DVD-ROM, programmed memory such as read only memory (Firmware), or on a data carrier such as an optical or electrical signal carrier. For many applications, embodiments will be implemented on a DSP (Digital Signal Processor), ASIC (Application Specific Integrated Circuit) or FPGA (Field Programmable Gate Array). Thus the code may comprise conventional program code or microcode or, for example code for setting up or controlling an ASIC or FPGA. The code may also comprise code for dynamically configuring re-configurable apparatus such as re-programmable logic gate arrays. Similarly the code may comprise code for a hardware description language such as Verilog TM or VHDL (Very high speed integrated circuit Hardware Description Language). As the skilled person will appreciate, the code may be distributed between a plurality of coupled components in communication with one another. Where appropriate, the embodiments may also be implemented using code running on a field-(re)programmable analogue array or similar device in order to configure analogue hardware.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word “comprising” does not exclude the presence of elements or steps other than those listed in a claim, “a” or “an” does not exclude a plurality, and a single feature or other unit may fulfil the functions of several units recited in the claims. Any reference numerals or labels in the claims shall not be construed so as to limit their scope.

CLAIMS

1. A system for driving a loudspeaker having a plurality of coils, the system comprising:
- 5 a modulator configured to receive an input signal and to output a pulse width modulated (PWM) output signal representative of the received input signal;
- a delay element for receiving and applying a delay to the PWM output signal to generate a first delayed signal;
- a first output configured to be coupled to a first coil of the plurality of coils of the
- 10 loudspeaker, wherein the first output is coupled to the output of the modulator; and
- a second output configured to be coupled to a second coil of the plurality of coils of the loudspeaker, wherein the second output is coupled to the output of the delay element.
- 15 2. A system according to claim 1 wherein the modulator comprises a class D amplifier.
3. A system according to claim 1 wherein the input signal comprises an audio signal.
- 20 4. A system according to claim 1 wherein the input signal comprises a digital signal and the modulator comprises a digital modulator.
5. A system according to claim 1 wherein the modulator and the delay element are configured to receive a clock signal.
- 25 6. A system according to claim 5 wherein the delay element comprises a clocked buffer or a counter.
7. A system according to claim 6 wherein the delay element further comprises an
- 30 edge detector and an edge generator, wherein:
- the edge detector is configured to detect an edge of an input PWM signal and to trigger the counter on detection of the edge;
- the counter is configured to count pulses of the clock signal until a predetermined number is reached and to output a signal to the edge generator when the predetermined
- 35 number is reached; and

the edge generator is configured to output a delayed and inverted version of the input PWM signal in response to receiving the signal from the counter.

8. A system according to claim 1 wherein the delay element is configured to apply a
5 delay equal to one period of the output PWM signal to the output PWM signal.

9. A system according to claim 1 wherein the delay element forms at least part of a finite impulse response (FIR) filter arrangement.

10 10. A system according to claim 9 wherein the FIR filter arrangement is configured to receive a configuration signal and, based on configuration signal, to adapt in response to a variation in a frequency of the PWM output signal output.

11. A system according to claim 10 wherein the FIR filter arrangement is operative, in
15 response to the configuration signal, to adjust a predetermined value used by a counter of the FIR filter arrangement.

12. A system according to claim 11 wherein the FIR filter arrangement is configured to suppress a carrier of the PWM output signal.

20

13. A system according to claim 12 wherein the FIR filter arrangement is configured to provide a zero at a carrier frequency of the PWM output signal.

14. A system according to claim 1 wherein a carrier frequency of the PWM output
25 signal can be modulated based on a control signal.

15. A system according to claim 14 wherein the control signal is based on an operating mode of the system.

16. A system according to claim 14 wherein the control signal is based on an input
30 signal level of the input signal.

17. An integrated circuit comprising a system according to claim 1.

18. A device comprising a system according to claim 1, wherein the device comprises a portable device, battery powered device, a mobile telephone a notebook, laptop or tablet computing device a smartwatch or an accessory device.
- 5 19. A method for driving a loudspeaker having a plurality of coils, the method comprising:
- receiving an input signal and outputting a pulse width modulated (PWM) output signal representative of the received input signal; and
- applying a delay to the PWM output signal to generate a first delayed signal;
- 10 outputting the PWM modulated output signal to a first coil of the plurality of coils; and
- outputting the first delayed signal to a second coil of the plurality of coils.
20. A system for driving a loudspeaker having a plurality of coils, the system
- 15 comprising:
- a modulator for receiving an input signal and outputting a first PWM output signal for driving a first coil of the plurality of coils;
- a finite impulse filter (FIR) arrangement for receiving the PWM output signal and to outputting a second PWM output signal for driving a second coil of the plurality of coils,
- 20 wherein the FIR arrangement is configured to adapt to a variation in a frequency of the PWM output signal output so as to suppress a carrier of the PWM output signal.
21. A system for driving a transducer having a plurality of coils, the system comprising:
- a modulator for outputting a digital output signal representative of a received
- 25 analogue input signal at a modulator output;
- a clock controlled delay element for applying a delay to the digital output signal to generate a first delayed signal at a delay element output;
- wherein the modulator output is couplable to a first coil of the plurality of the coils of the transducer and the delay element output is couplable to a second coil of the
- 30 plurality of coils of the transducer.
22. A system according to claim 21 further comprising a clock signal generator operative to generate a clock signal for the clock controlled delay element.
- 35 23. An integrated circuit comprising the system of claim 21 or claim 22.

24. A system for driving a transducer, the system comprising:
a modulator for outputting a digital output signal representative of a received
analogue input signal at a modulator output;
a delay element for applying a delay to the digital output signal to generate a first
5 delayed signal at a delay element output;
a first inductor having a first terminal coupled to the modulator output; and
a second inductor having a first terminal coupled to the delay element output,
wherein a second terminal of the first inductor is coupled to a second terminal of
the second inductor to provide an output node for a drive signal to drive the transducer.
10
25. A system according to claim 24 wherein the first inductor and the second inductor
comprise first and second coils of the transducer.
26. A system according to claim 23 or claim 24 wherein the transducer comprises a
15 loudspeaker.
27. A module comprising the system of any one of claims 24 – 26 and a transducer.
28. An integrated circuit comprising the system of any one of claims 24 – 26.
20

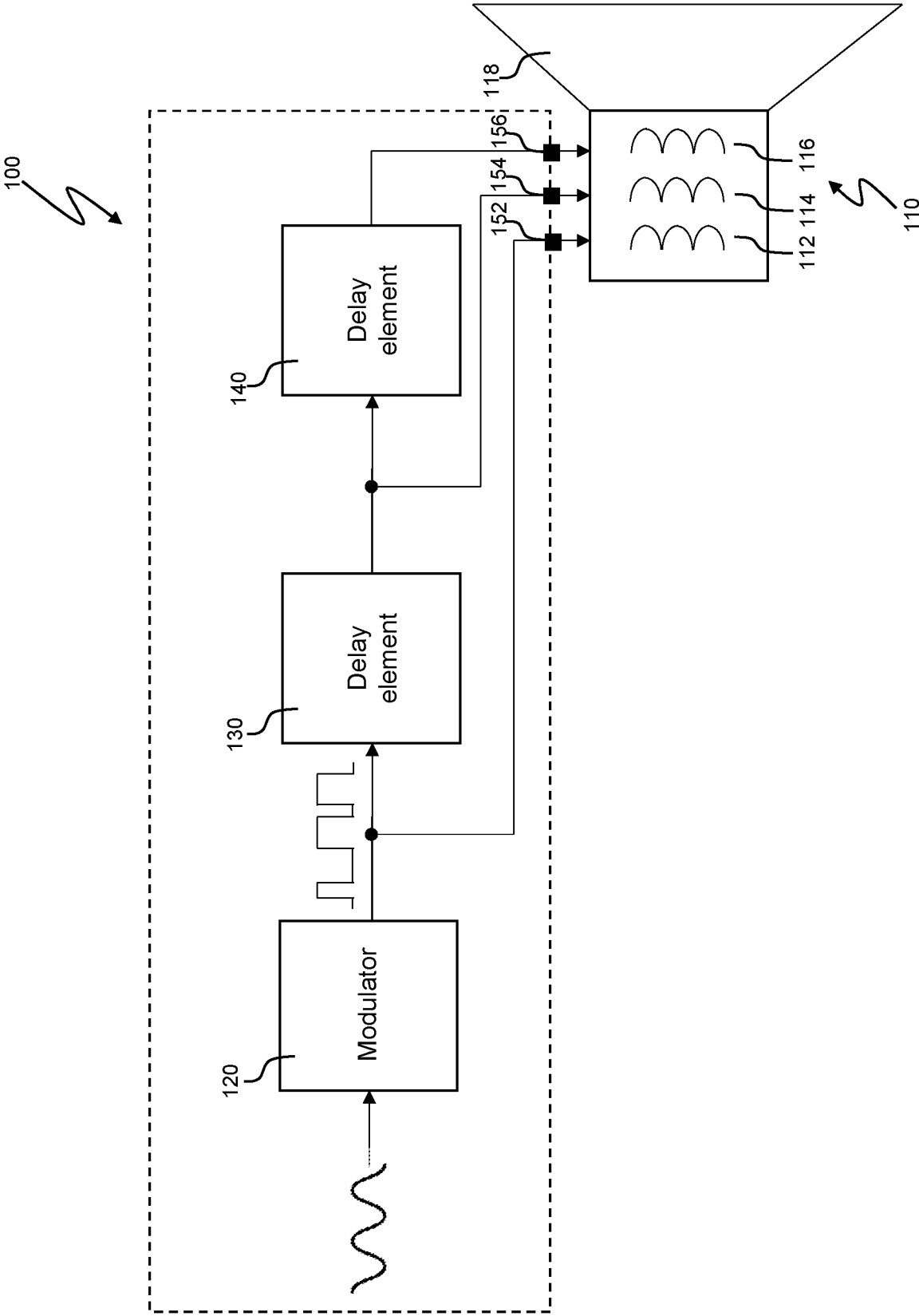


Figure 1

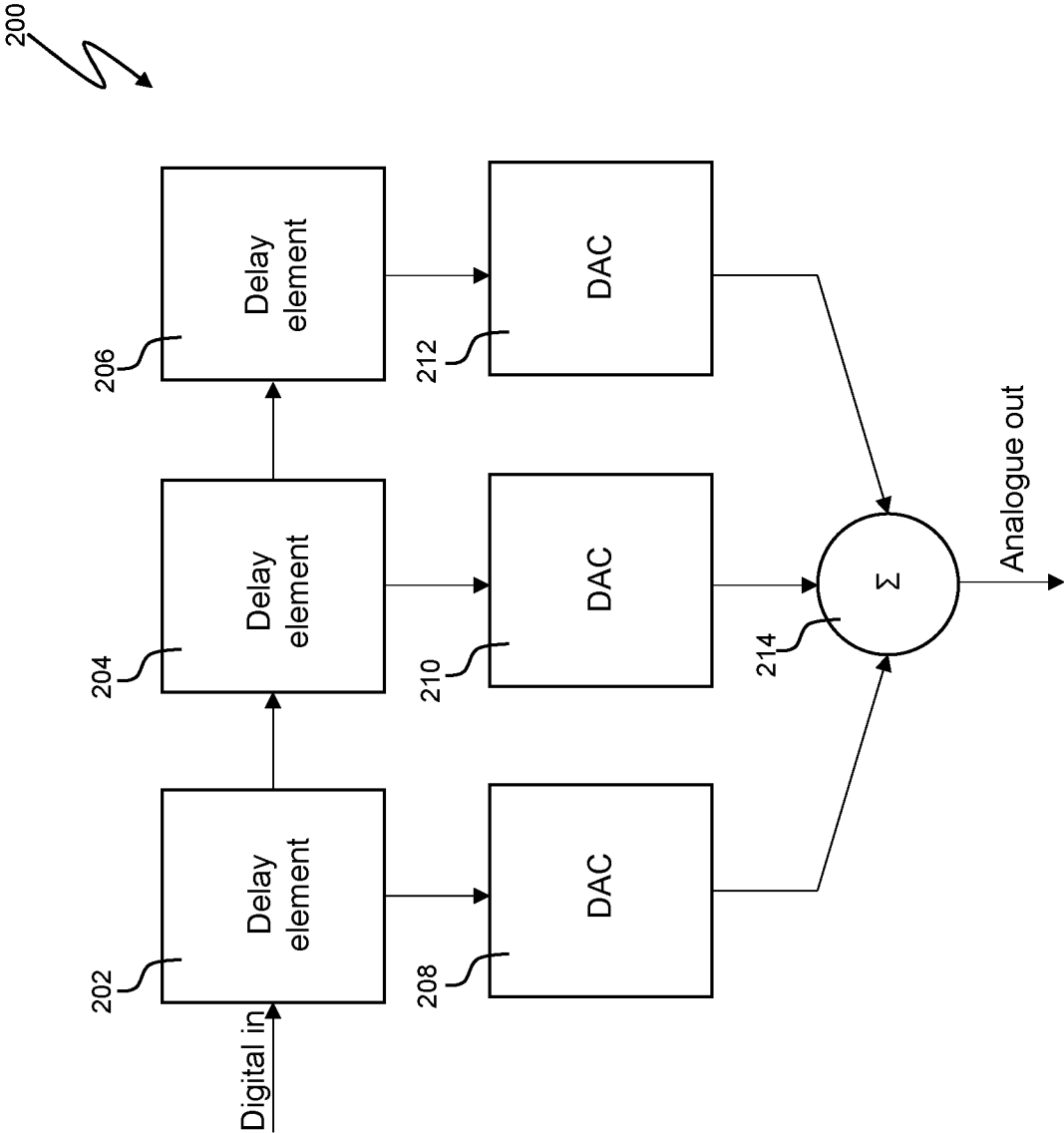


Figure 2

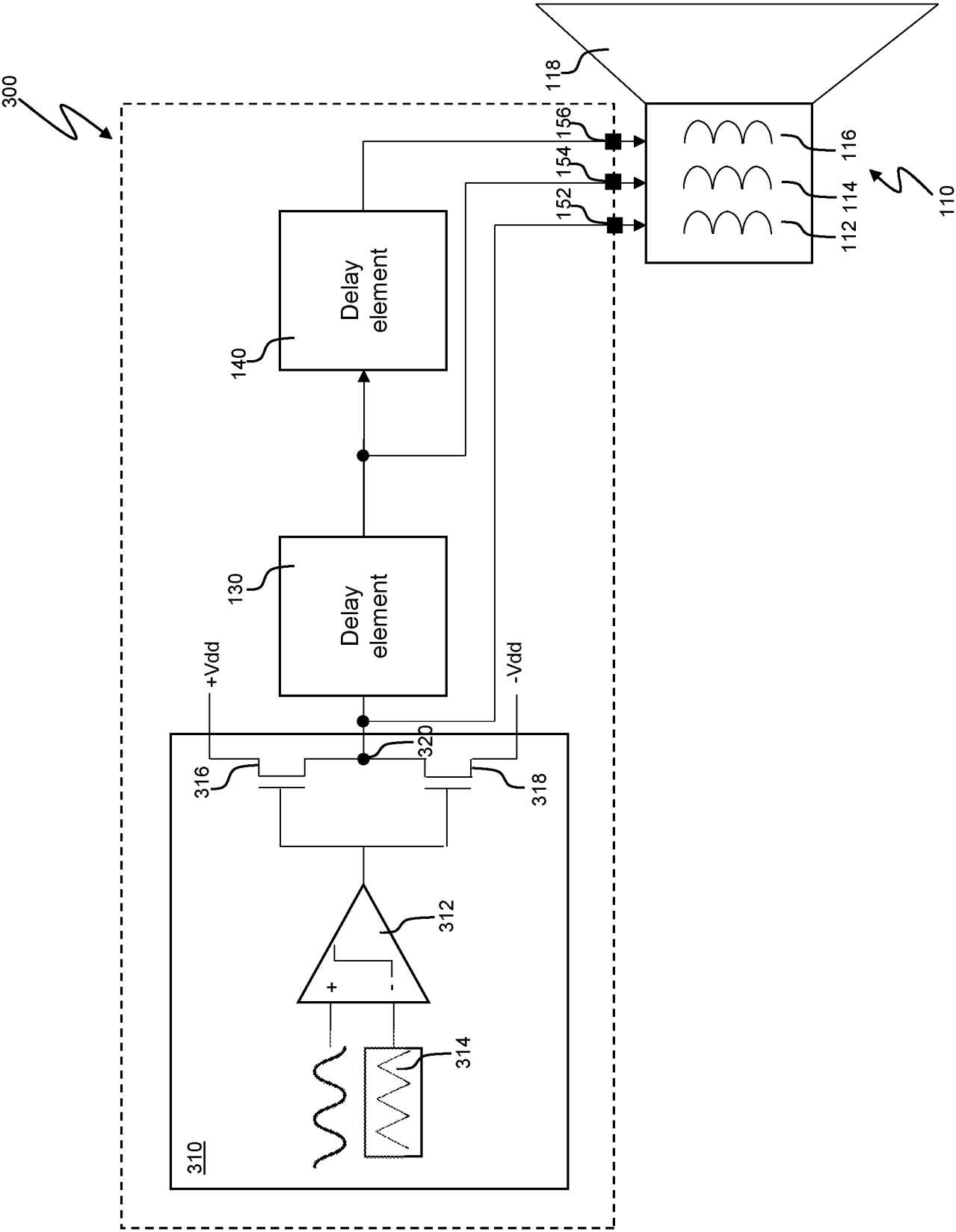


Figure 3

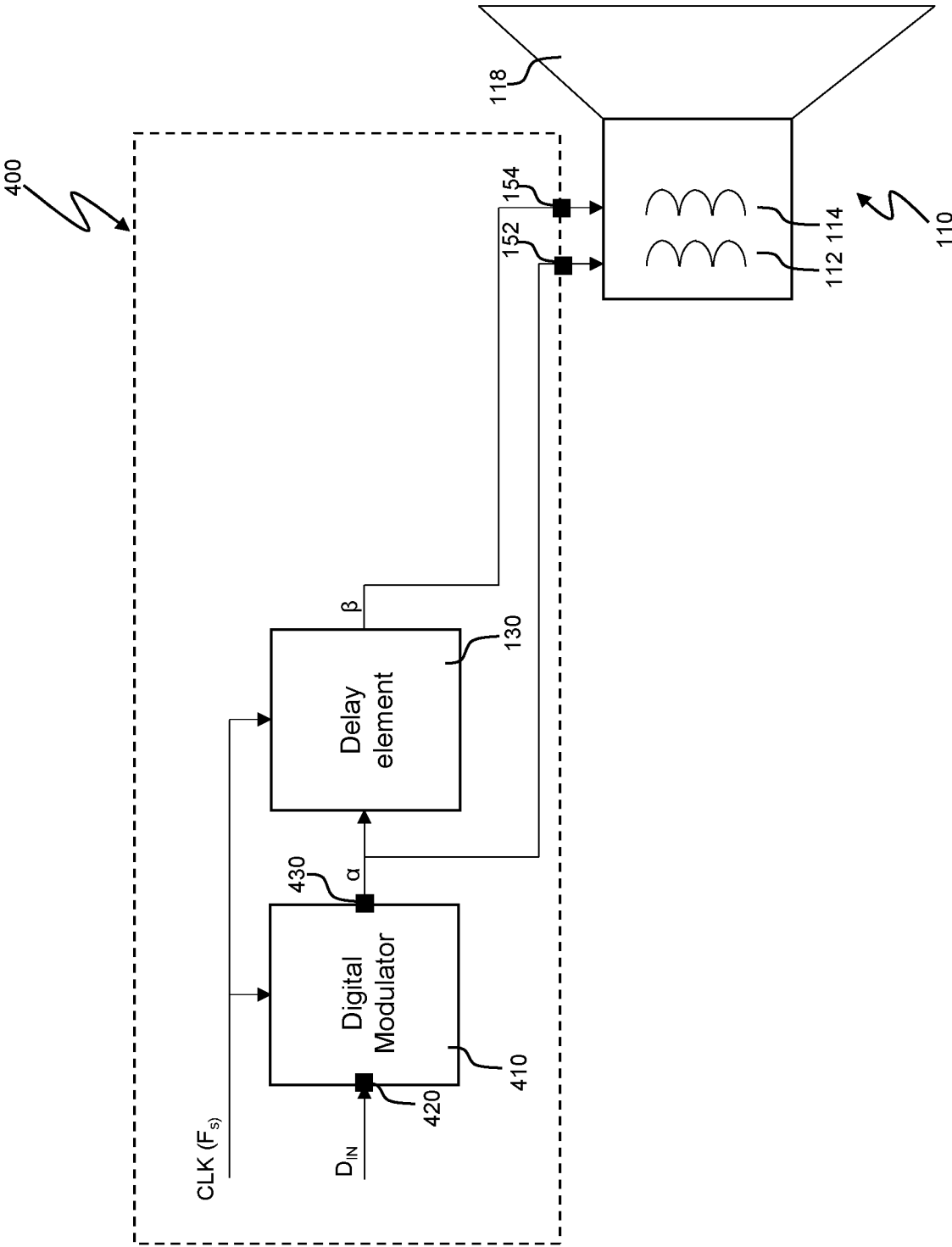


Figure 4

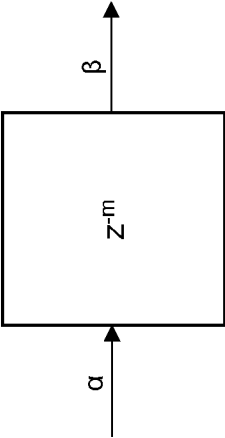


Figure 5

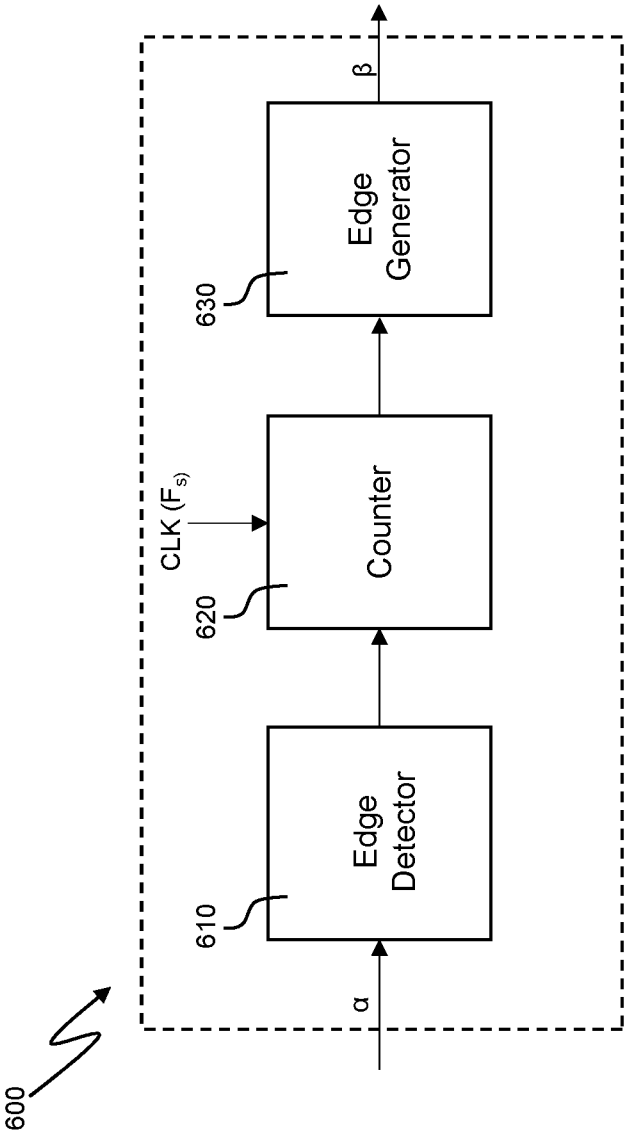


Figure 6

700 ↗

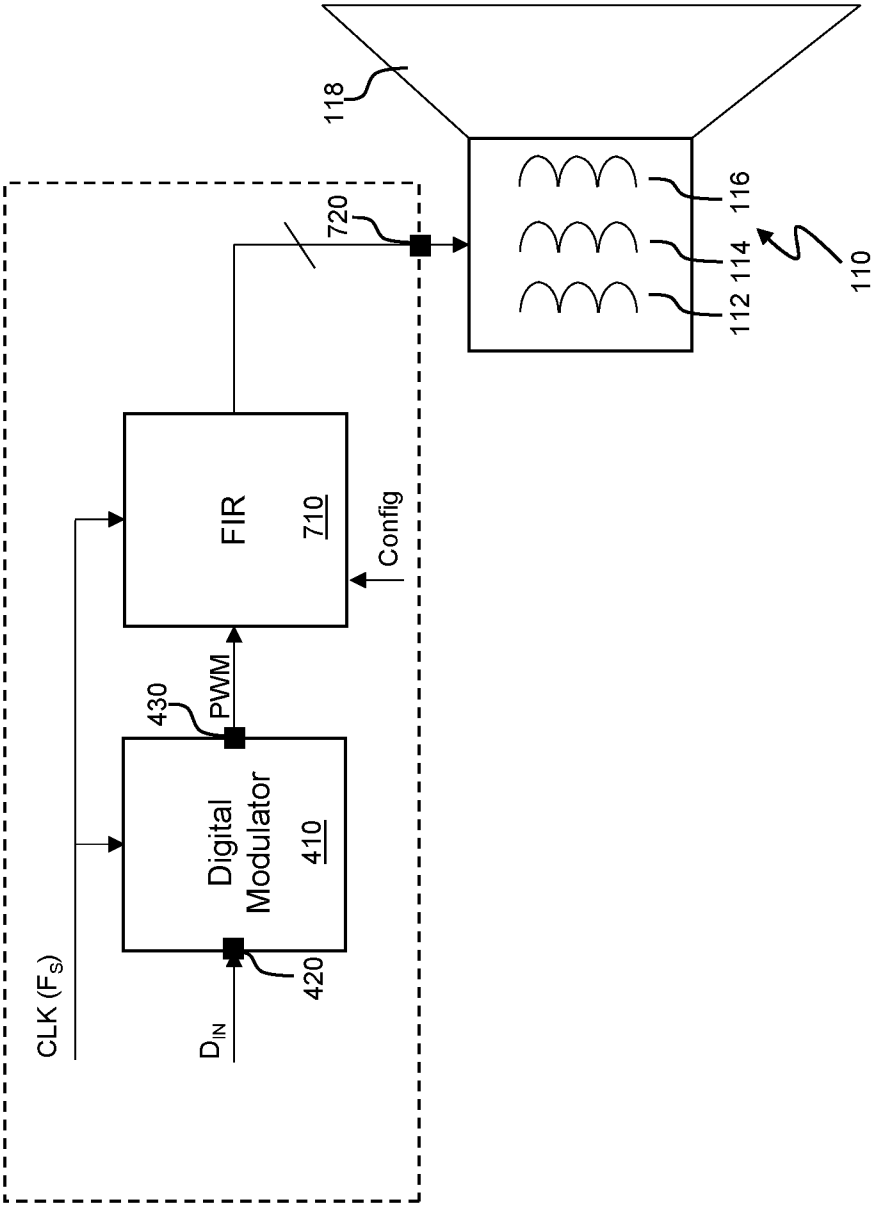


Figure 7

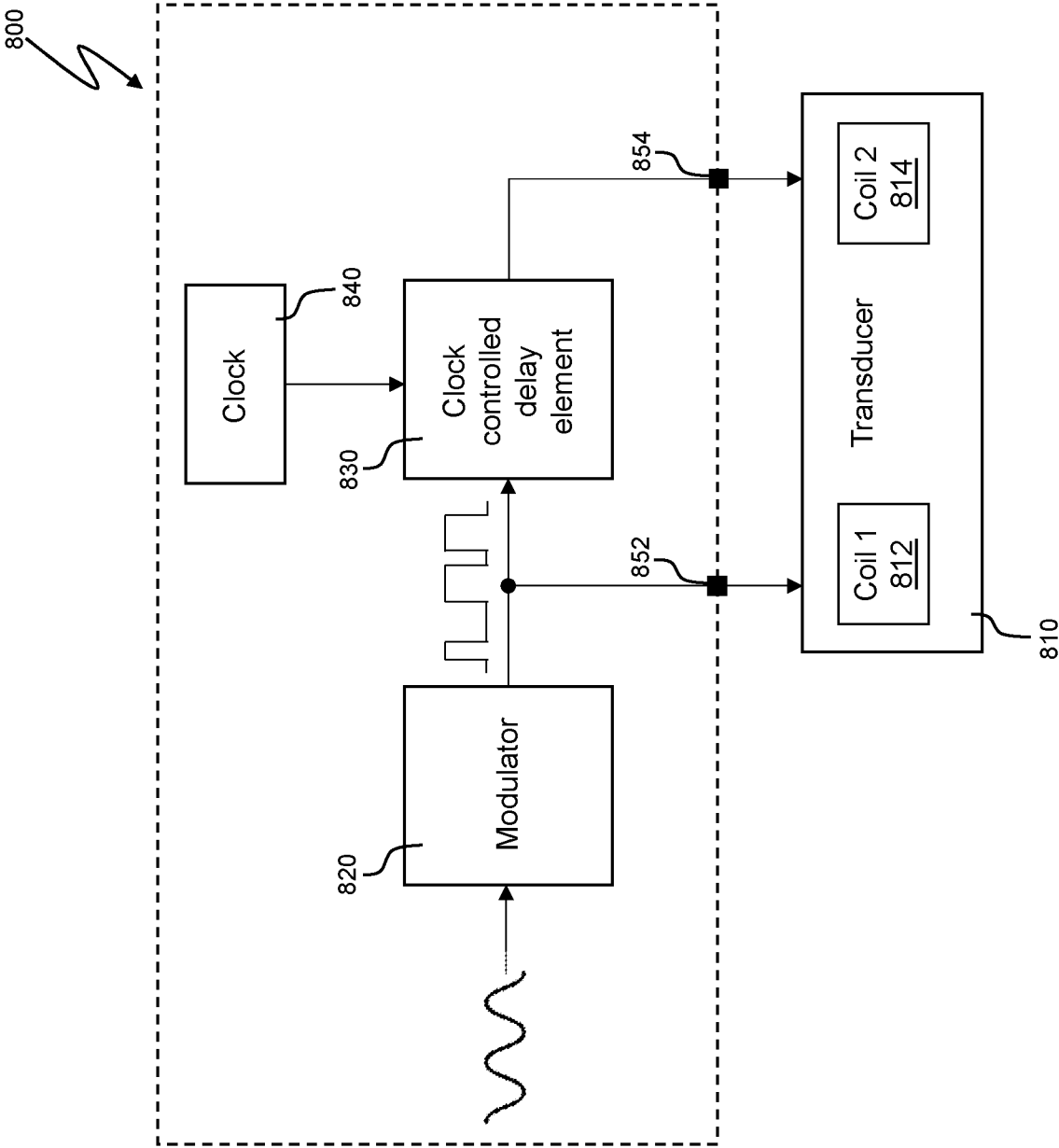


Figure 8

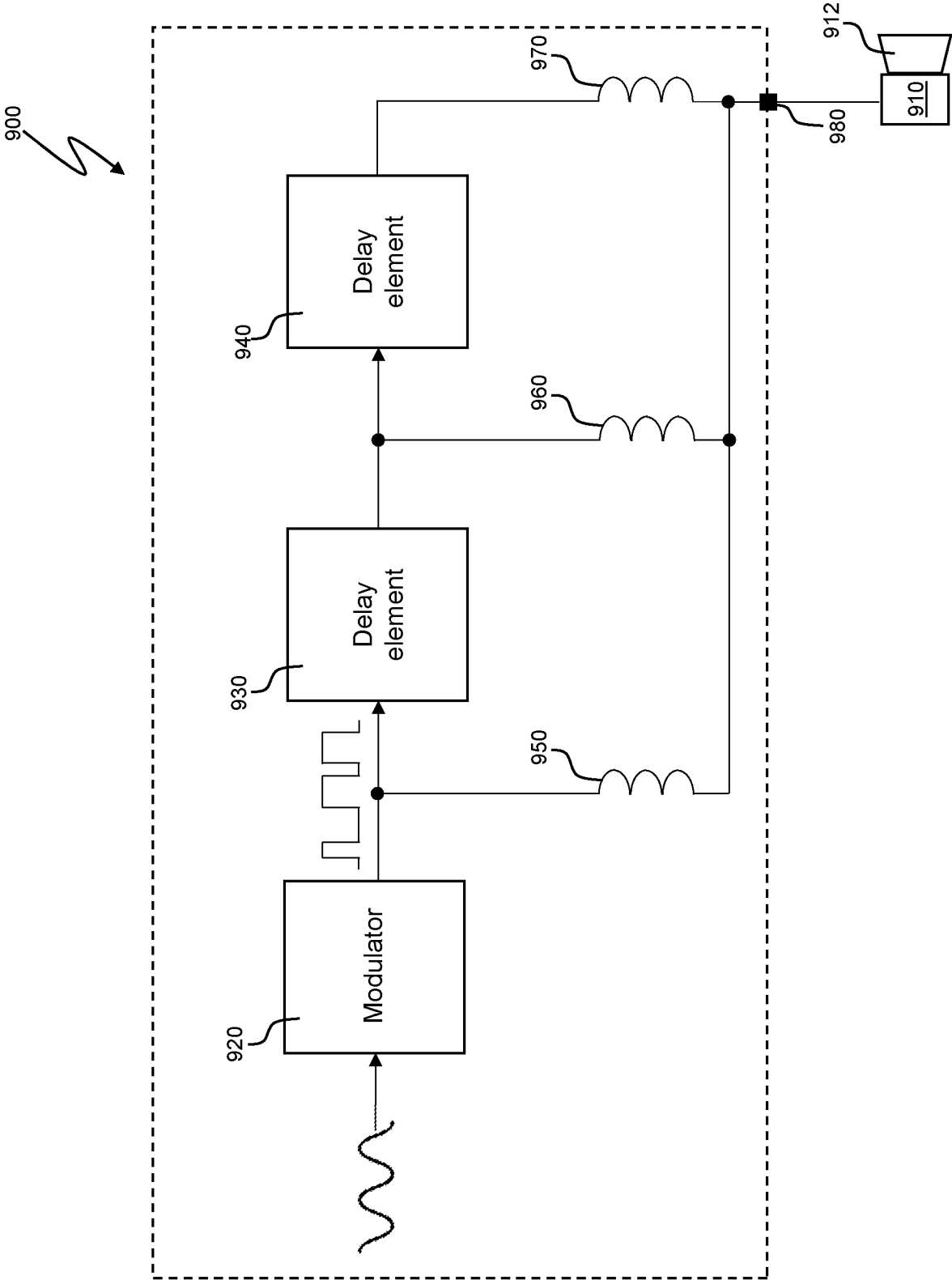


Figure 9

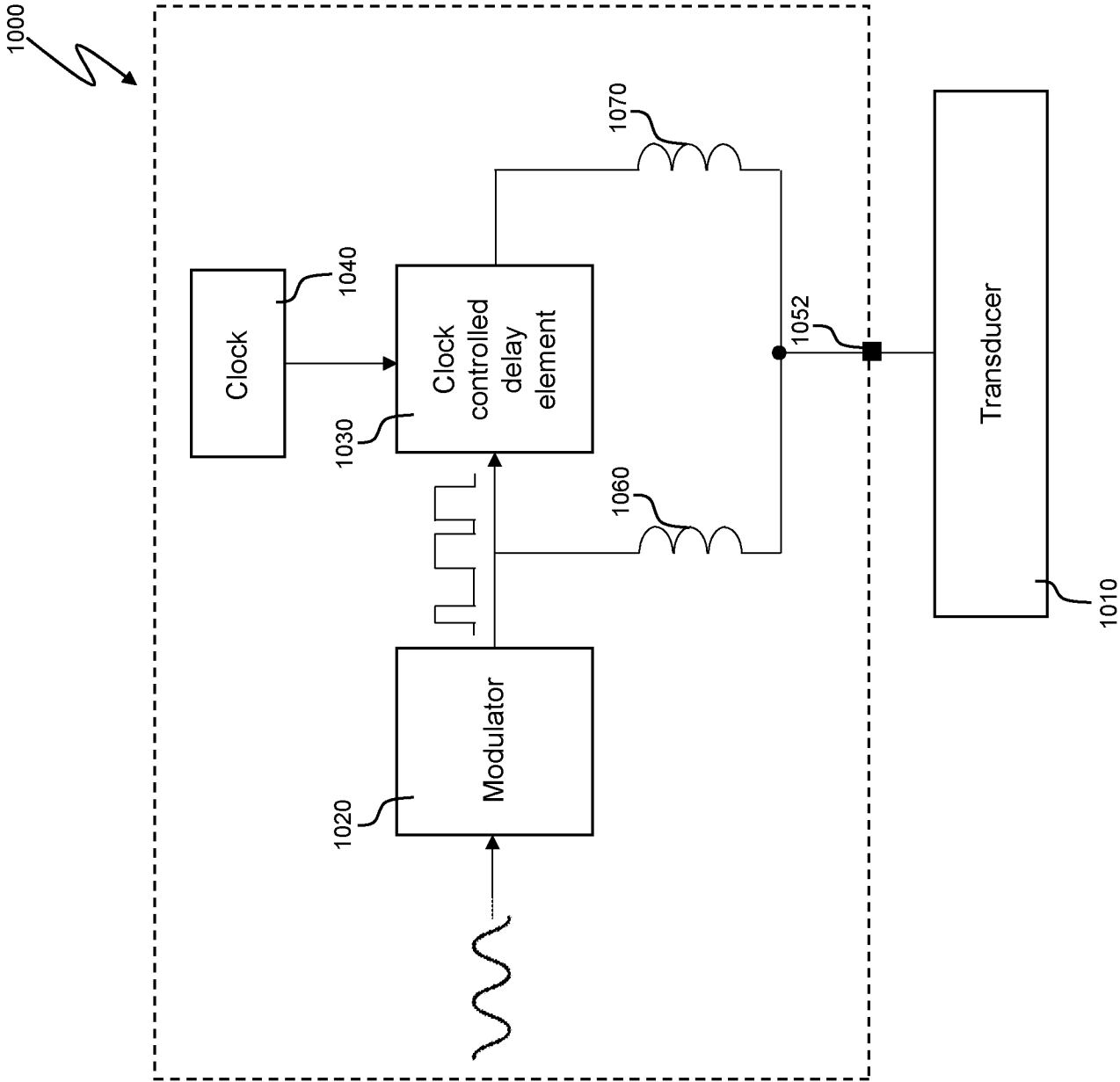


Figure 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2021/050178

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04R1/00 H04R3/04 H03F3/217
ADD. H04R9/04 H04R9/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04R H03F H03M H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, COMPENDEX, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP H04 355599 A (MATSUSHITA ELECTRIC IND CO LTD) 9 December 1992 (1992-12-09)	1-6,9, 17-19, 21-23
Y	paragraphs [0002], [0008] - [0010]; figures 1-3	7
Y	----- US 2013/342254 A1 (MAZUMDER KALLOL [US] ET AL) 26 December 2013 (2013-12-26) paragraphs [0015] - [0027]; figures 1-3	7
A	----- EP 0 167 157 A2 (HEWLETT PACKARD CO [US]) 8 January 1986 (1986-01-08) page 17, lines 18-34; figure 16 -----	5-7



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

18 March 2021

Date of mailing of the international search report

18/05/2021

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Radomirescu, B-M

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB2021/050178

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of Item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-7, 9, 17-19, 21-23

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-7, 9, 17-19, 21-23

Digitally Controlled Delay for Loudspeaker Driver System

2. claims: 8, 10-13, 20

FIR Filtering in a Loudspeaker Driver System

3. claims: 14-16

Loudspeaker Driver System Based on Controlled PWM

4. claims: 24-28

Loudspeaker Driver System for PWM audio signals

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2021/050178

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
JP H04355599	A	09-12-1992	NONE	

US 2013342254	A1	26-12-2013	NONE	

EP 0167157	A2	08-01-1986	EP 0167157 A2	08-01-1986
			HK 54593 A	11-06-1993
