PATENT SPECIFICATION (11) 1 573 652

1 573 652

(21) Application No. 17054/77 (22) Filed 25 Apr. 1977 (19)

(31) Convention Application No. 2618225 (32) Filed 26 Apr. 1976 in

(33) Fed. Rep. of Germany (DE)

(44) Complete Specification Published 28 Aug. 1980

(51) INT. CL. [3] G06G 7/02 //
G01S 7/30
G06G 7/19

(52) Index at Acceptance
G4G 2F2 S
H4D 36X 402 40X 460

(54) IMPROVEMENTS IN OR RELATING TO MULTIPLEX ANALOGUE VOLTAGE STORES

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Féderal Republic, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:-

The invention relates to multiplex analogue voltage stores, for the input storage and read out of analogue voltage samples which are fed consecutively via a common input line to individual storage elements, and are consecutively withdrawn from the individual storage elements via a common output line; the input and output of each storage element being connected to said common lines via respective input and output switch stages, one of each for each storage element, each input switch stage being controlled by a first register, and each output switch stage being controlled by a second register.

In radar systems using moving target transit time filters, a signal delayed by the scan period T is compared with an undelayed signal so that echo signals emanating from moving targets are isolated and available for study, whereas echo signals from stationary targets are substantially suppressed.

When the range measuring zone of a radar device is split into a plurality of range channels, this signal comparison must be effected in such a way that the signals from each one range zone are in each case only compared with earlier signals of that same range zone, so that with m range channels it is necessary to provide at least m separate storage elements, in which the relevant scan samples can be stored.

As it is not possible to effect a simultaneous input to and read-out from the same storage element, the difficulty arises as will be explained in further detail hereinafter, that voltage values from different range channels may need to be fed into any one storage element. On account of the different threshold voltage values of the individual switches that are used for the selective input and read-out, different interference voltages constantly occur in the individual scan samples.

The same problems arise in digital filters or other general multiplex systems, when m channels must be processed in a multiplex operation using individual storage devices. In the case of correlators such as are used for auto-correlation circuits, delayed and undelayed signals need to be compared with one another, so that such problems also occur in these circuits.

One object of the present invention is to provide a circuit arrangement of the type mentioned in the introduction in which the adverse influence of these disturbing residual charges is substantially eliminated.

The invention consists in a multiplex analogue voltage store including a plurality of storage elements, the inputs of which are connected in succession to a common input line via respective switching stages controlled by a common input register, and the outputs of which are connected in succession to a common output line via respective switching stages controlled by a common output register, wherein said common input line carries a plurality of interleaved channel signal samples, one sample of each of said channel signals constituting a sampling cycle and a sample of each respective signal appearing in the same relative position in each sampling cycle, wherein the samples of any one of said signals are stored in the same storage element in each cycle, and wherein the number of said storage elements is at least equal to the number of signals to be sampled in each cycle.

The invention will now be described with reference to the drawings, in which:-

Figure 1 is a schematic and simplified circuit diagram of a storage device for analogue

signals;

Figure 2 is a set of explanatory waveforms for a case where a constant exchange of the storage positions takes place;

Figure 3 is a set of explanatory waveforms for the case of input to the same storage element for each signal channel in each cycle;

Figure 4 is a simplified schematic circuit diagram of one exemplary embodiment of the invention in the form of a moving target filter for a radar device; and

Figure 5 is a graph illustrating the attenuation characteristic of the filter shown in Figure 4.

In the circuit arrangement shown in Figure 1, an input terminal SE for a series of consecutive scan samples that are to be stored in the form of analogue voltage values is connected to a common input line. In this example of the invention it has been assumed that 64 different scan samples arrive consecutively. For example, in a radar device the signals could be the contents of 64 range channels, i.e. the total coverage zone is divided into 64 range elements of equal size. However, it is also possible that one may be concerned with a multiplex channel transmission system with 64 channels, in which case 64 consecutive samples will occur in each frame cycle, after which the first channel appears again, in accordance with the frame period, commencing with sample 1.

The common input line from the terminal SE is connected to 64 electronically controllable switching stages FE1 to FE64, which are preferably in the form of field effect transistors. These input switches FE1 to FE64 are controlled via a common input register ER. At the start of a cycle this input register is fed with a start pulse at a terminal BE, so that, commencing with the switch FE1, the various switches FE1 to FE64 are selectively switched conductive in a consecutive manner. The input register RE has a first pulse train input CIE (clock 1) and a further drive input C2E (clock 2). Shift pulses are fed to the inputs C1E and C2E in known manner for a shift register, and these shift pulses actuate the input register RE in such manner that the switches FE1 to FE64 are each individually operated for a specific length of time. Accordingly, the consecutively arriving samples A1 to A64 pass into respectively associated storage elements C1 to C64. At the end of a cycle each of these storage elements thus contains an analogue voltage sample which emanates from a different radar range-gate or multiplex channel for example.

A sequential read-out of the analogue voltage samples which have been stored in the storage elements C1 to C64 is controlled by a common output register AR, which is constructed and operated in the same way as the input register ER, having a start input BA and two separate control inputs for clock pulse trains C1A and C2A. The read-out of the voltage samples A1 to A64, which have been stored in analogue form, from the individual storage elements C1 to C64 is carried out in the same sequence as that used for the write-in, via respective field effect transistors FA1 to FA65, which are consecutively opened in order to read out the voltage samples one at a time.

Devices known as "Serial Analog Memories" abbreviated as SAM and made by the Reticon company, of Mountain View California, can be used as store modules in the circuit illustrated in Figure 1, for example.

During read-out it should be taken into consideration that it is not possible to effect read-out from any one storage element at the instant at which input-storage is being carried out. Thus when the switch FE2 is opened to allow the amplitude sample A2 to be fed into the storage element C2, the switch FA2 must be closed, and read-out must be carried out with a specified delay relative to the write-in. Otherwise if simultaneous write-in and read-out occurs, the resulting signal distortions would be extremely undesirable.

Figure 2 is an explanatory timing diagram which illustrates the time sequence of the input-storage and output-storage for 63 channels in a store containing 64 storage elements, which is a known form of operation. The uppermost waveform shows scan samples at the input SE of Figure 1 that belong to one single channel A1; the signal sample A11 being of moderate positive value, the signal sample A12 being of moderate negative value, and sample A13 of larger negative value. The samples occur spaced in time by the period T, which represents the frame period of the operating cycle. Thus A11 is fed into storage element C1, and the next signal from that channel is the sample A12, which is fed into the storage element C64. Sample A13 will be stored in storage element C63, the next in C62, and so on. It has been assumed that read-out is to be effected with a shift of one storage position, so that during the write-in of sample A11 into the storage position C1, a sample A21 of the second channel in the cycle sequence is read out from the storage position C2,i.e. at each instant read-out occurs from a storage element one position before the position at which write-in is occurring. As the storage device C2 is thus discharged at this instant, it is consequently prepared for the write-in of the next sample. Accordingly, as the second sample A12 of the first channel is being fed into the storage position C64, the storage position C1 is being discharged and the sample A22 of the second channel read out. During the write-in of the first channel sample A13 into the storage position C63, the sam-

ple A23 of the second channel is being read out from the storage position C64. It will thus be seen that the read-out signals for each channel occur with a period duration T, and thus have the same frame sequence as the input cycle. The maximum period of time *tc* which is available for the read-in to a store position and read-out from a storage position is given by the relationship T/n; where *n* is the number of utilizable storage positions and in the present example is the number of channels, i.e. 63, which is one less than the number of storage positions. If the storage element C1 is considered, it will be seen that the sample A11 was firstly stored in the storage element C1, in accordance with the timing plan shown in Figure 2. The next sample A12 belongs to the first channel passes into the storage element C64, and the next sample A13 from the same channel passes into the storage element C63. Thus samples from different channels are consecutively stored in each individual storage elements. This leads to undesired disturbances, which result from the fact that, both during write-in and during read-out, potential shifts occur which originate from the threshold voltages of the switching transistors FE and FA in their conductive states, which transistors can be considered as transfer resistances. As the individual output switches FA1 to FA64 and input switches FE1 to FE64 in the Figure 1 embodiment must be assumed to have mutually differing characteristics, due to manufacturing tolerances, as a result of the rotary storage principle, the samples of a specific channel are subject to constantly changing interference voltages.

Figure 3 is a timing plan for the write-in and read-out of the individual samples in a store such as that shown in Figure 1 when adapted to operate in accordance with the invention, and so avoid the above-described interference. For simplicity in comparison, the store is assumed to be that described with reference to Figure 1, with 64 storage positions but the system operates with a frame cycle having a number of $m = 64$ channels, so that any one storage position always holds a sample from the same channel in each cycle, as shown for the store position C2, which successively holds the samples A21, A22 and A23 of the second channel in the three illustrated cycles. As read-out must be from a different position to that being written into any instant, when sample A21 of the second channel is being written into store position C2, the sample A11 of the first channel is read out from the store position C1, but is fed via a delay device VE which introduces a delay τ and as there is a shift of only one store position between read-in and read-out in each case, the delay τ has a duration of T/m, where *m* is the number of channels in each cycle. To adapt the store shown in Figure 1 to operate in accordance with the invention, an exemplary embodiment is formed by the addition of the delay device VE in the common output line after terminal SA, to feed a signal to terminal SA' in which the channel samples read out are in step with each subsequent sample being read in at that instant for that particular one of the *m* channels.

Thus, an improvement is achieved in an embodiment constructed in accordance with the invention, as the same storage element is always used for the same channel, and thus the respective samples of any one channel are subject to the same interference voltage in each cycle. In an embodiment employing a difference of *k* storage elements between write-in and read-out, the time delay in the device VE must amount to $k.t_c$.

Figure 4 schematically illustrates a complete moving target filter of a pulse Doppler radar device, in which a plurality of storage circuits VS corresponding to the storage arrangement shown in Figure 1 are provided. Store VS1 with a delay device VE1 form part of an input stage ES constituting a first moving target filter. Store VS2, with delay device VE2, together with store VS3 and its delay device VE3 serve a dual function, operating as part of a digital filter HS and as part of a double-transit time moving target filter CA. Each store introduces a negative delay of T-τ, which is corrected by the addition of a positive delay τ. A common clock generator CG controls read and write operations for all the stores. Load resistors R link the units, and potentiometers PM1 and PM2 set coefficients in the digital filter HS. This filter can incorporate analogue-digital converters to give fully digital coded operation, but in the embodiment shown operates as an analogue calculating filter, with a sample output of analogue form for each respective channel. At input E1 a video signal obtained after coherent demodulation of the radar receiver signal is fed to store VS1 and to a non-inverting input of a subtraction stage ST1. The output of the store VS1, subjected to a total delay of (T-τ) + τ, and therefore in step at the stage ST1, is fed to an inverting input of this stage. Thus the input stage ES represents a simple moving target filter canceller or MT1 filter with samples from successive cycles of the same range channel of the pulse Doppler radar fed to the stage ST1. Interference voltages which are governed by the differing threshold voltages of the switches FE1 and FE64 and FA1 to FA64, and which possess a respective constant value in each channel, are schematically indicated as a parasitic input Ustl represented by an arrow.

This input stage ES, in the form of a simple transit time moving target filter, is followed by a scan filter (calculator filter) HS, which

consists of a subtraction stage ST2 and the two storage circuits VS2 and VS3 with their respective delay devices VE2 and VE3. This is a double recursive filter stage, which improves upon the simple high-pass filter characteristics of the preceding canceller circuit ES, so giving a more favourable filter curve. As already mentioned, the coefficients in the recursive stage are set by the potentiometers PM1 and PM2.

As in the input stage ES, in the following filter stage HS, parasitic interference voltage components Ust2 and Ust3 occur in the individual storage circuits VS2 and VS3. A line branches off from the output of the subtraction circuit ST2 and leads to the one input of a subtraction stage ST3. The same input is also connected to the output of the delay device VE3 which follows the storage circuit VS3. The second input of the stage ST3 is connected to the output of the delay device VE2 of the storage circuit VS2. It should be noted that the storage circuits VS2 and VS3 and their associated delay devices are doubly exploited, serving not only as effective delay devices for the doubly recursive filter HS, but also as delay devices for the double transit time moving target filter CA, completed by the subtraction stage ST3.

The interference voltage components Ust1 and Ust2 which occur in the storage stages VS1 and VS2, as already mentioned, each possess quite specific values for each channel. Generally speaking these are additional d.c. voltage values which possess a specific value in respect of each channel. These interference voltages behave similarly to fixed target echo signals, and are considerably weakened by the transit time moving target filter CA. Generally speaking, this means that any remaining interference voltage components can be eliminated by a following transit time moving target filter (which can also consist of one stage). However, this functions only for such time as the interference voltages for each channel remain identical from one sample to the next sample, i.e. when the samples of the same channel pass across the same switches (as in Fig. 3) and not (as in Fig. 2) constantly across different switches.

A simple numerical example will be considered by way of explanation. For example, if constant value fixed target signals of 5V are processed, and a voltage loss of 0.1V occurs through the switches, e.g. FE1 and FA2 in Fig. 1, then consecutive samples no longer fully cancel one another out in the stage ST1, because +5V is compared with -4.9V. Thus, a permanent difference of +0.1V remains as a residual voltage, in all the samples of the fixed target. This disturbing residual voltage Ust1 is suppressed by a following transit time fixed target filter CA, in the manner of a fixed target echo signal. A suppression is effected similarly for the value Ust2. The remaining interference voltages Ust3 have amplitude values so small that there is virtually no disturbing influence in practical operation.

Figure 5 graphically illustrates the resultant filter characteristics of the filter circuit shown in Figure 4, with the standardized frequency f/fs plotted on the abscissa, where fs = scan frequency = the pulse train repetition frequency of the radar device and attenuation is plotted on the ordinate.

WHAT WE CLAIM IS:-

1. A multiplex analogue voltage store including a plurality of storage elements, the inputs of which are connected in succession to a common input line via respective switching stages controlled by a common input register, and the outputs of which are connected in succession to a common output line via respective switching stages controlled by a common output register, wherein said common input line carries a plurality of interleaved channel signal samples, one sample of each of said channel signals constituting a sampling cycle and a sample of each respective signal appearing in the same relative position in each sampling cycle, wherein the samples of any one of said signals are stored in the same storage element in each cycle, and wherein the number of said storage elements is at least equal to the number of signals to be sampled in each cycle.

2. A store as claimed in Claim 1, in which each read-out signal is fed via a delay device which has a delay period equal to a given whole-numbered multiple of the duration of any one channel sample, said given whole-number being that number of store positions between that one store which is read-out and a subsequent store which is being written into at that instant, and being at least one.

3. A store as claimed in Claim 2, in which the analogue storage of the samples, followed by said delay is utilised in a feed-back circuit to provide a digital filter effect.

4. A store as claimed in Claim 2, in which the analogue storage of the samples, followed by said delay, is utilised to form a circuit having a correlator characteristic.

5. A multiplex analogue voltage store substantially as described with reference to Figures 1 and 3.

6. A doppler radar device in which a moving target filter is formed using a store as claimed in any preceding claim.

7. A radar device as claimed in Claim 6, having moving target filters substantially as described with reference to Figure 4.

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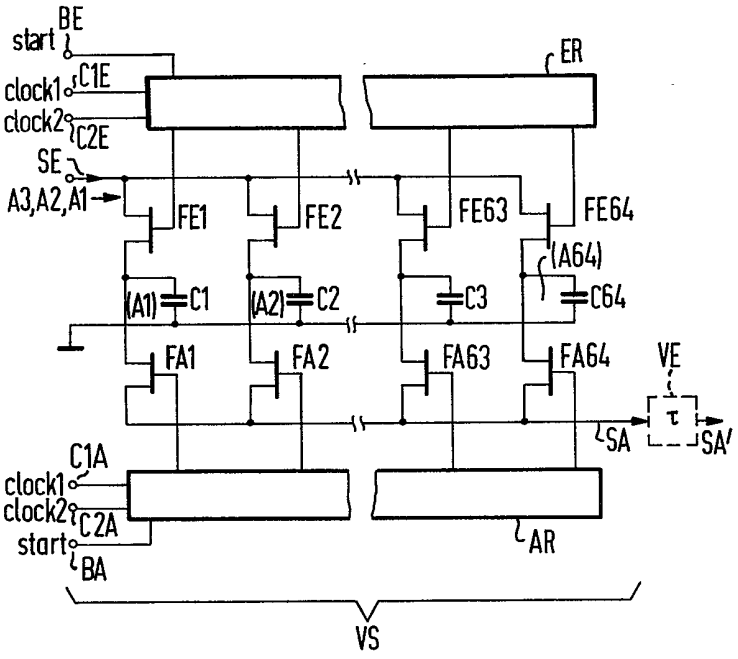
Printed for Her Majesty's Stationery Office,
by Croydon Printing Company Limited, Croydon, Surrey, 1980.
Published by The Patent Office, 25 Southampton Buildings,
London, WC2A 1AY, from which copies may be obtained.

Fig.1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C1E
clock2
C2E
SE
A3,A2,A1
ER
FE1
FE2
FE63
FE64
(A64)
(A1)
C1
(A2)
C2
C3
C64
FA1
FA2
FA63
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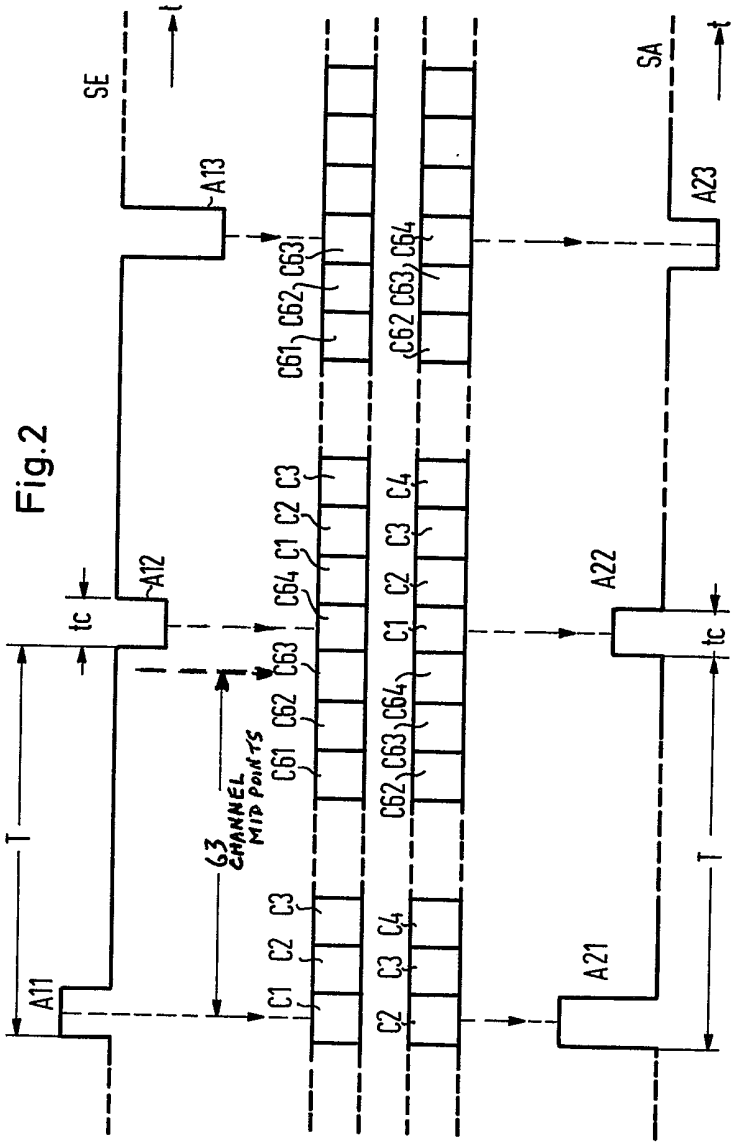
VE
τ
SA
SA'
C1A
clock1
clock2
C2A
start
BA
AR
VS

Fig.2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t
A13
A12
tc
A11
T
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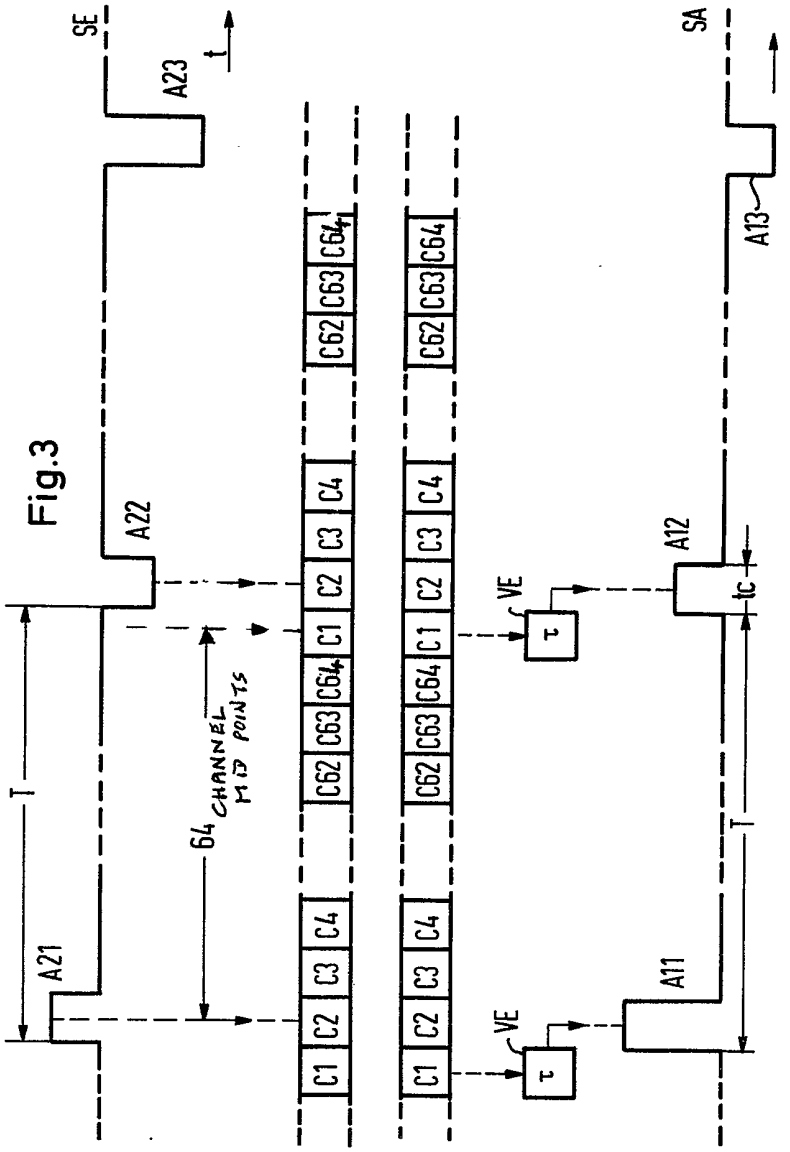
C1 C2 C3 C4
SA
A23
A22
A21

Fig.3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A23
t
A22
A21
T
64 CHANNEL MID POINTS
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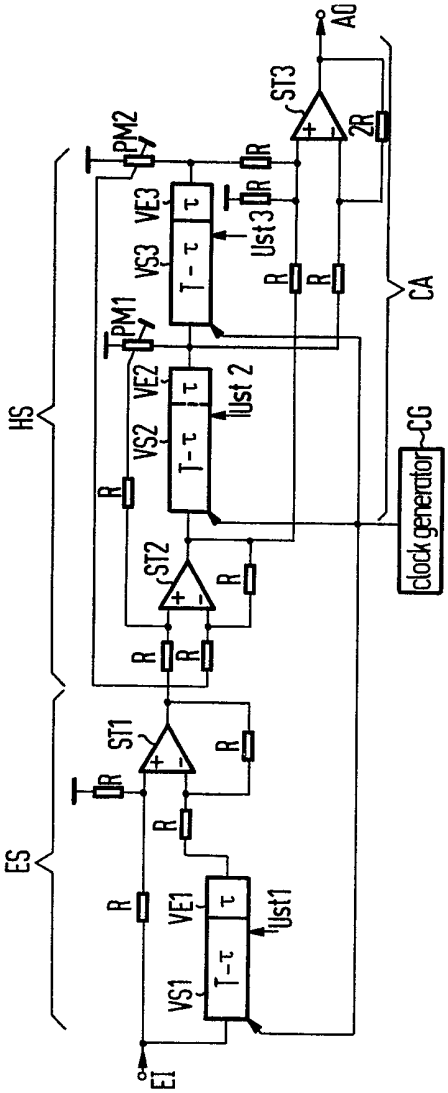
VE
τ
SA
A13
A12
tc
A11

Fig. 4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ST3
2R
PM2
R
VE3
τ
T-τ
VS3
Ust3
R
R
CA
PM1
VE2
τ
T-τ
VS2
Ust 2
HS
R
CG
clock generator
ST2
R
R
R
ST1
R
R
R
ES
VE1
τ
T-τ
VS1
Ust1
E1

Fig.5