United States Patent

Matejka

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[54] **PLURAL CHANNEL SYSTEM WHEREIN THE INPUT SIGNALS ARE UNALTERED IF WITHIN STANDARD LIMITS, BUT ARE AVERAGED, IF OUTSIDE LIMITS**

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Nov. 10, 1970 Germany.....P 20 55 084.9

[52] **U.S. Cl.** .....**307/219,** 307/237, 307/304, 328/117, 328/171, 340/146.1 BE

[51] **Int. Cl.**.....**G06f 11/08,** G08b 29/00, H03k 5/08

[58] **Field of Search**.....307/204, 219, 235, 251, 237, 307/279, 304; 328/116, 117, 137, 139, 147, 148, 149, 150, 156, 169, 171, 172; 340/146.1 BE; 235/153

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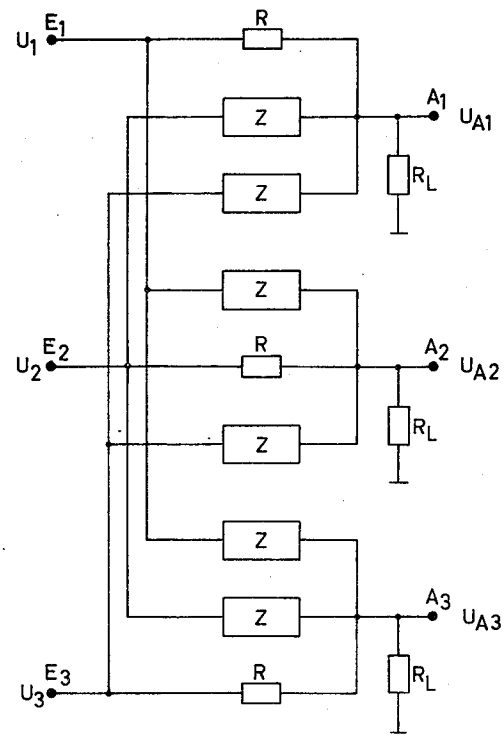
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Primary Examiner—Herman Karl Saalbach
Assistant Examiner—L. N. Anagnos
Attorney—Darbo, Robertson & Vandenburgh

[57] **ABSTRACT**

A control apparatus has redundant input signals from which an output signal is produced. In part it comprises three inputs to which the respective input signals are applied and three outputs. There are three resistors of known value with each connecting a respective input and a respective output. There are six resistance devices each connecting a respective input with one of the remaining outputs between which there is not one of the resistors. The resistance devices comprise a voltage sensitive double-pole whose resistance substantially equals said known value below a selected threshold voltage but which becomes very great above said threshold voltage. The threshold voltage is selected to be sufficiently greater than the normal input voltage to represent a malfunction situation.

11 Claims, 10 Drawing Figures



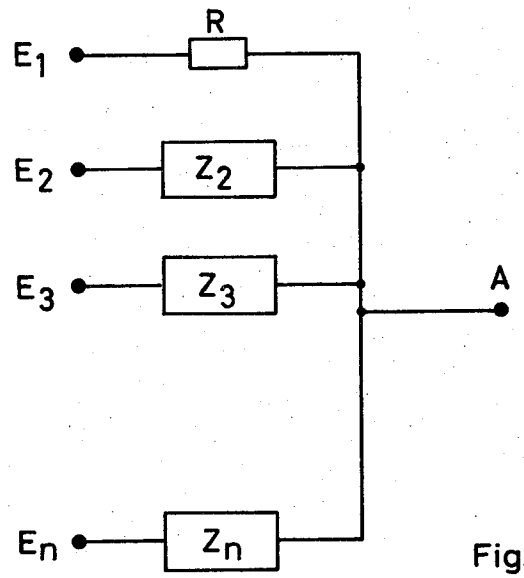


Fig. 1

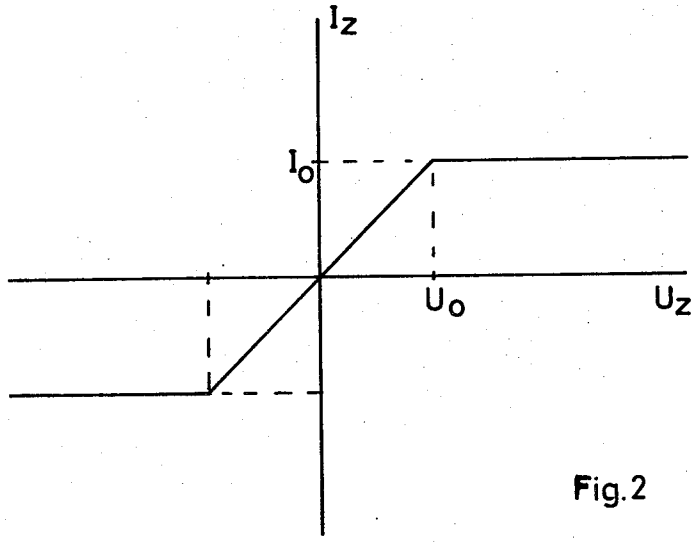


Fig. 2

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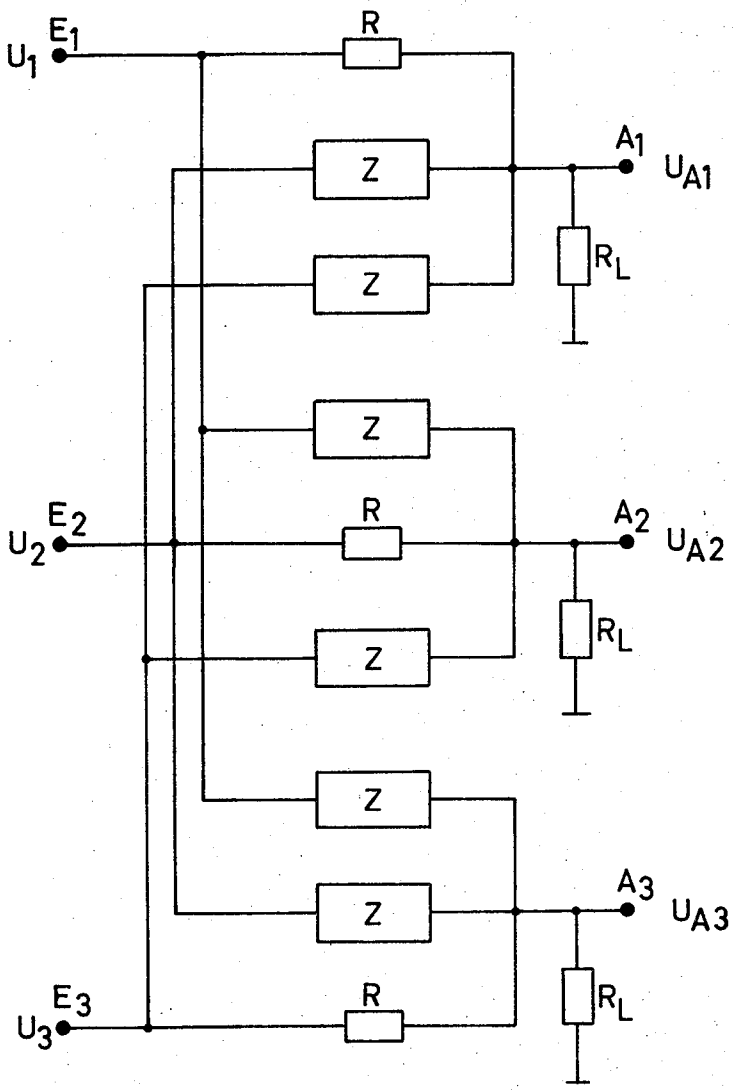


Fig. 3

INVENTOR

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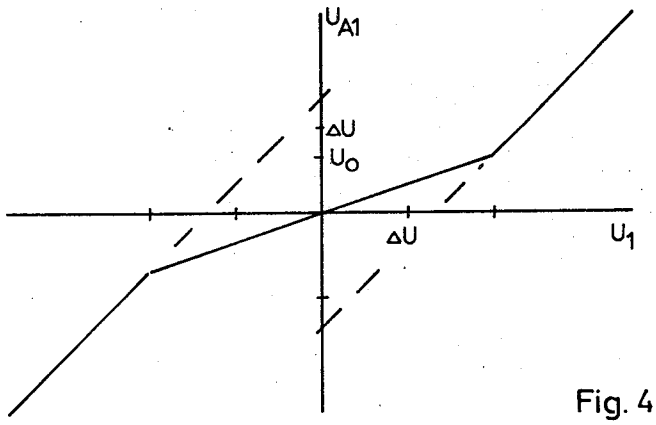


Fig. 4a

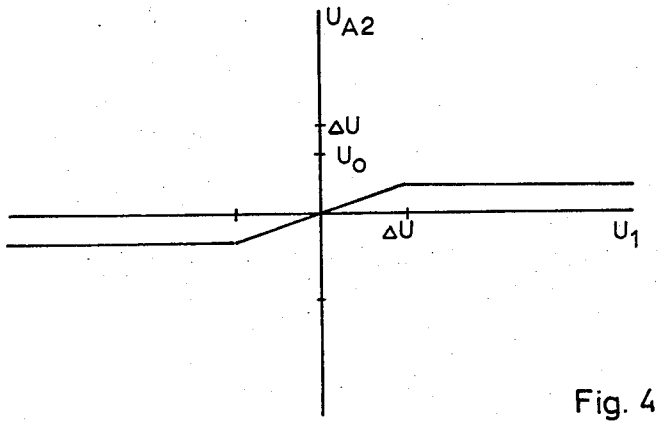


Fig. 4b

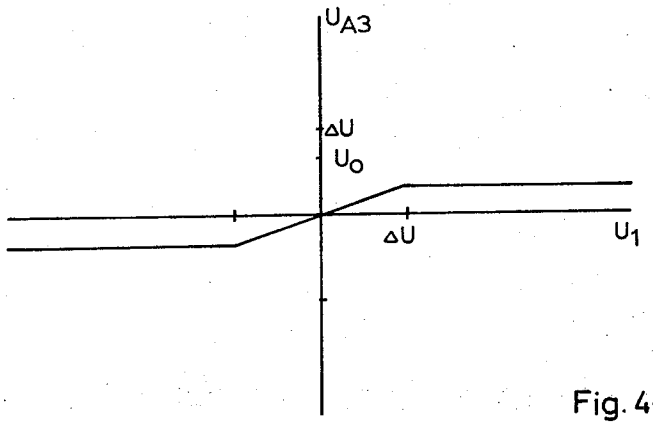


Fig. 4c

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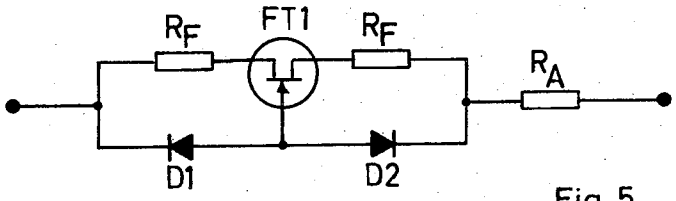


Fig. 5

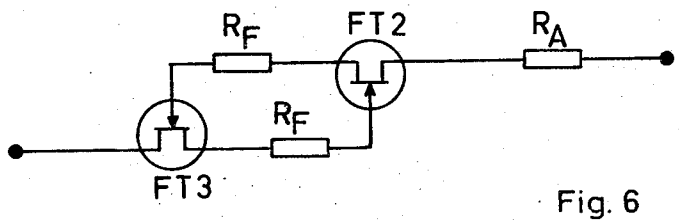


Fig. 6

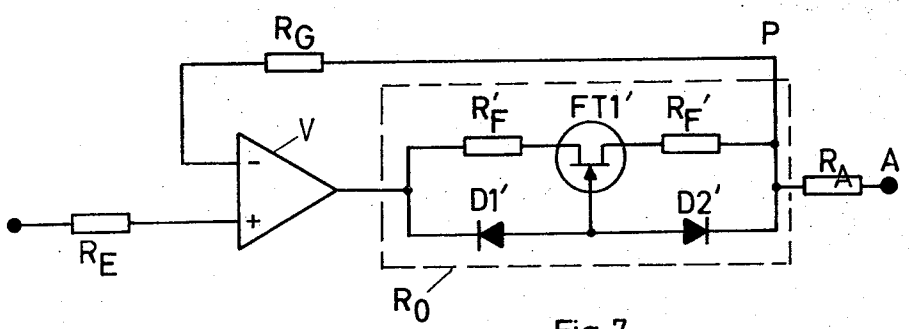


Fig. 7

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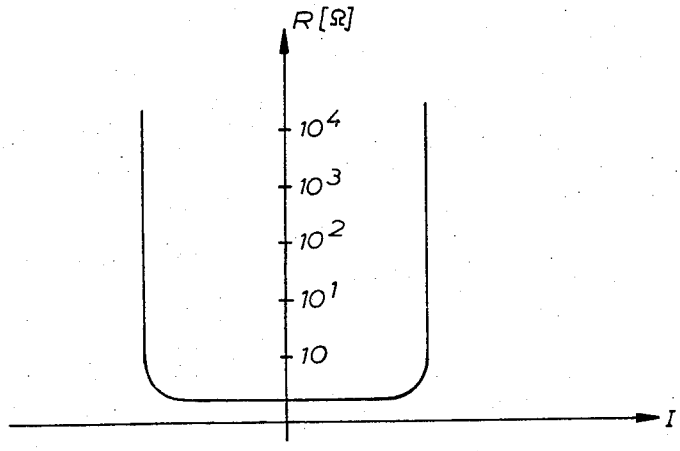


Fig. 8

INVENTOR

Matyka

PLURAL CHANNEL SYSTEM WHEREIN THE INPUT SIGNALS ARE UNALTERED IF WITHIN STANDARD LIMITS, BUT ARE AVERAGED, IF OUTSIDE LIMITS

BACKGROUND AND SUMMARY OF THE INVENTION

This invention relates to a circuit arrangement for forming the mean value of several input voltages, in which the input voltages are applied through resistor branches to a common load resistor at which the mean value output voltage appears, and in which at least a part of the resistor branches is controlled in dependence on the difference between the output voltage at the load resistor and the respective input voltage in such a manner that this input voltage will be suppressed, if it deviates by more than a given extent from the output voltage.

More specifically, this invention relates to a circuit arrangement for synchronizing signals in redundant systems comprising a plurality of signal inputs and a plurality of signal outputs, in which each signal input is connected with all of the signal outputs through one resistor branch each.

Circuit arrangements of the type indicated are required in apparatus, in which for reasons of safety, measured value transmitters and signal channels are provided in multiple number; for instance, in automatic pilots in which one and the same control signal is generated by three signal circuits independent of each other. Due to tolerances of the components used, these signals always show slight signal differences. These signal differences which are not due to shortcomings of the components complicate an error recognition by monitoring devices. An error is considered to exist if the signal differences exceed a pre-established fixed value. It may therefore be expedient within a multiplied signal chain to evaluate the signals once or several times. In prior art arrangements (for example, see Ser. No. 858,737, filed Sept. 17, 1969, entitled SIGNAL SELECTION CIRCUIT, the disclosure of which is incorporated by reference) this is accomplished by circuits which select from three input signals the signal of the mean amplitude, thus, of the amplitude having a magnitude between that of the two other signals. As these circuits, however, automatically suppress an error signal, they must be equipped with additional arrangements for error recognition so that an error, if it occurs, does not remain concealed. These additional arrangements for error recognition require quite a considerable amount of apparatus.

Moreover, there are prior art circuit arrangements in which a mean value is formed from several input voltages (in the meaning of an arithmetic mean). The input voltages are applied through resistor branches to a common load resistor across which the mean value output voltage appears. In this connection, provisions are made that each of the resistor branches is controlled in dependence on the difference between the output voltage at the load resistor and the associated input voltage in such a manner that a particular input voltage will be suppressed if it deviates by more than a given extent from the output voltage. This given extent corresponds to the signal tolerances. A signal which deviates by more than this given extent from the mean value, is considered as an error signal and is suppressed.

It is an object of this invention to provide a circuit arrangement for forming the mean value of several input voltages, in which input voltages which deviate by more than a given extent from the output voltage, are suppressed.

It is another object of this invention to effect such a suppression of the "out of place" input voltages in a contactless manner.

It is an object of this invention to provide a circuit arrangement for synchronizing, thus equalizing several signals, in which such a synchronization is effected so long as the signal deviations of several signals (deviations within the range of permissible tolerances) do not exceed a pre-established fixed value, but a signal whose deviation exceeds the fixed value of the permissible tolerances is transferred as unfalsified as possible. With such a circuit arrangement for synchronization it is then possible to restrict the signal monitoring to a few points in the signal flux, thereby leading to a substantial saving of components.

According to this invention, provision is therefore made that the voltage-controlled resistor branches include voltage-sensitive double-poles whose resistance becomes very great above a voltage threshold.

In a further modification of this invention a synchronizing circuit of the type mentioned in the beginning is designed in such a manner that each signal input is connected with an associated signal output through a voltage insensitive resistor and with all of the other signal outputs through voltage sensitive double-poles whose resistance values below a threshold value of the voltage applied thereto are equal to the said voltage in-sensitive resistor and above this threshold value become very great.

DESCRIPTION OF THE DRAWINGS

FIG. **1** shows the application of *n* input signals to an output.

FIG. **2** shows the characteristic of the double-poles used in the circuit of FIG. **1**.

FIG. **3** shows a complete circuit arrangement for three input signals and three output signals.

FIGS. **4***a* to **4***c* show the three output voltages in dependence on one input voltage.

FIG. **5** illustrates one embodied form of a double-pole applicable to the invention.

FIG. **6** illustrates another embodied form of a double-pole.

FIG. **7** illustrates a third embodied form of a double-pole.

FIG. **8** shows the characteristic of a cold conductor for use with the invention.

DESCRIPTION OF SPECIFIC EMBODIMENTS

The following disclosure is offered for public dissemination in return for the grant of a patent. Although it is detailed to ensure adequacy and aid understanding, this is not intended to prejudice that purpose of a patent which is to cover each new inventive concept therein no matter how others may later disguise it by variations in form or additions or further improvements. The claims at the end hereof are intended as the chief aid toward this purpose, as it is these that meet the requirement of pointing out the parts, improvements, or combinations in which the inventive concepts are found.

FIG. 1 shows the used basic circuit for n input signals. An input signal U_1 is applied at input E_1 and transferred to output A through branch resistor R. Similarly, the inputs $E_2 \ldots E_n$ receive input signals $U_2 \ldots U_n$ which go to the common output A through voltage sensitive double-poles $Z_2 \ldots Z_n$. In order that the operation of the illustrated basic circuit is functionally correct, the double-poles must have the characteristic illustrated in FIG. 2. The characteristic shows that the double-poles are voltage sensitive. For a voltage

$$U_z < U_o$$

applied across the double-pole, the double-pole resistance shall be

$$R_z = R$$

For a voltage

$$U_z > U_o$$

applied across the double-pole, however, the current through the double-pole shall be limited to the value

$$I_z = I_o.$$

The double-pole voltage U_o is selected in accordance with the permissible signal deviation ΔU of the input voltages. For the current I_o it applies that the current must be greater than the required maximum output current of the circuit arrangement. From these data, the (FIG. 1) resistance

$$R = U_o/I_o$$

is calculated.

FIG. 3 illustrates a complete circuit arrangement for three input signals U_1, U_2 and U_3 and three output signals U_{A1}, U_{A2} and U_{A3}. In this case, the basic circuit illustrated in FIG. 1 is provided with three inputs E_1, E_2 and E_3 and is used three times to obtain three outputs A_1, A_2 and A_3. There is a resistor R connecting each input with a respective output. The connections between the remaining inputs and outputs is provided by voltage sensitive double-poles Z.

In FIGS. 4*a*, 4*b* and 4*c* the three output voltages U_{A1}, U_{A2} and U_{A3} are illustrated in dependence on an excessive input voltage U_1. It was determined that up to the signal deviation ΔU, the double-poles have the resistance R. From this condition U_o is obtained. Under the condition $U_1 = \Delta U$, $U_2 = U_3 = 0$

$$U_o = 2/3\ \Delta U$$

For n inputs

$$U_o = (N - 1/n) \cdot \Delta U$$

is obtained.

FIGS. 4*a* to 4*c* show that the output signals of the circuit arrangement are identical up to a signal deviation of ΔU. If the signal deviation exceeds the value ΔU at the input E_1 (FIG. 3), then the output signals U_{A2} and U_{A3} will no longer be influenced by it (FIGS. 4b and 4c). The maximum signal deviation at the outputs A_2 and A_3 based on the signal deviation at the input E_1 is $\Delta U/3$. At the output A_1 appears the voltage $2\ \Delta U/3$ up to a value of $U_1 = 2\ \Delta U$, whereas signal deviations beyond that and reduced by the constant value $2\ U_o$ become fully effective at the output A_1. Since the circuit regarding input and associated output is always designed identically, the identical results are obtained for the two other inputs.

The preceding considerations were made without a load. The permissible load current is maximally I_o. It effects an output signal offset by maximally $0.5\ U_o$ at the outputs for an input signal deviation smaller than ΔU. For input signal deviations greater than ΔU (in the case of an error signal), it effects an output signal offset by maximally U_o. Thus, the following situation is obtained:

As long as the signal deviations are below a preestablished threshold value (hence, are due to the permissible tolerances of the components), a mean value formation is effected so that at all of the three signal outputs the same signals occur and can be processed further in the succeeding channels. If a signal is "out of place", i.e. exceeds the permissible tolerance, this signal will become fully effective at a respective one of the outputs, apart from a certain shift in amplitude, while being suppressed as an error signal at all other outputs. Thus, at the latter outputs the error signal is discounted and a mean value formation is effected so that in these channels identical signals within the permissible tolerances can be processed. In the channel of said respective one output the error signal occurs. This error signal becomes effective in a similar manner also in the succeeding synchronizing circuits. Thus it is possible to provide an arrangement for error recognition at a specific point of the signal channels and to eliminate the error signal at the same time. However, it is not necessary to provide such an arrangement for error recognition in each individual synchronizing circuit.

The voltage sensitive double-poles (e.g. Z of FIG. 3) are obtainable from the following components:

1. Cold Conductors

See FIG. 8. A cold conductor is a temperature-dependent resistor which is of very low resistance below the Curie-temperature and has a high positive temperature coefficient above the Curie-temperature. The resistance of a cold conductor can be varied by means of the current flowing therethrough. As the variation in resistance is effected via the by-pass of temperature, also the ambient temperature influences the break of the characteristic. It is therefore that a stabilization of the ambient temperature be provided. In order to be able to adjust the magnitude of the resistance of the double-pole to the necessary value, a balancing resistor must be connected in series with the cold conductor.

2. Circuit Arrangements with Field Effect Transistors

The circuit illustrated in FIG. 5 employs a symmetrical field effect transistor FT1 as the main component of a voltage-sensitive double-pole such as might be used in each resistor branch Z. The symmetrical field effect transistor has a pair of preceding and succeeding resistors R_F. Its base is connected through diodes D_1, D_2 with the free end of the resistors. A balancing resistor R_A is in series-connection in this circuit to make up the remainder of the total resistance R. This double-pole circuit also has the necessary characteristic. Herein, the low resistance range is substantially determined by the properties of the field effect transistor FT1. To make up the required resistance R, the balancing resistor R_A is used. The adjustment of the current limita-

tion I_0 is accomplished by means of the resistors R_F. Advantageously, field effect transistors with low drain-source resistance ($r_{DS\ on}$) and small "pinch-off" voltage are used.

Another circuit including field effect transistors is shown in FIG. 6, in which the double-pole of each resistor branch Z comprises a pair of field effect transistors (FT2, FT3) connected back-to-back (antiparallelly) by resistors R_F. The grid of each field effect transistor is connected through a resistor R_F with the cathode of the other transistor. A balancing resistor R_A is arranged in series-connection in this circuit to make up the total resistance R. Herein, the current I_0 is adjusted with the resistors R_F, the resistance R with the resistor R_A.

3. Circuits with Operational Amplifiers

If very accurate values for R and I_0 are to be provided, the use of four-pole circuits, the transfer characteristic of which corresponds to that of the double-poles, are recommended. In these circuits, operational amplifiers are preferably used. An example for such a circuit to form a resistor branch is shown in FIG. 7. Utilizing a field effect transistor double-pole of the type discussed in connection with FIG. 5, its input is connected to the output of an operational amplifier V. The output P of the double-pole is connected to the input of the amplifier by a feedback resistor R_G providing negative feedbacks. The branch input E is connected by a resistor to the amplifier input by a resistor R_E. The branch output A is connected to P by a resistor R_A which serves to make up the desired total resistance R. The FIG. 5 double-pole (FT1, R_F, R_F, D_1 and D_2) provides current limiting in the series circuit between input E and output A.

Of course, also other circuit arrangements are known which can be used herein to provide current limitation, a condition being that the current limitation is effective in a bipolar manner. The negative feedback of the amplifier according to the current limiting circuit is derived at the point P and is applied via the feedback resistor R_G to the inverting point (input) of the amplifier. The input signal U is also applied to the non inverting point via the input resistor R_E. Due to the negative feedback the source impedance is very small and can be neglected, when the amplifier is operated on its characteristic. Then, the source impedance at the output point A of the arrangement is determined only by the resistance R_A which connects the point P with the point A. Therewith, the resistance R_A can be selected in accordance with the requirements of the circuit arrangement of the invention and generally corresponds to the resistance R.

It may also be mentioned that the wiring of the operational amplifier can substantially be selected as desired. Thus, special frequency characteristics also can be achieved.

I claim:

1. In an apparatus for forming the mean value of several input voltages in synchronizing signals in redundant systems including a plurality of system inputs and a plurality of system outputs, and a plurality of branches each having an individual input and having a common output with resistor means in each branch, there being one of said branches between each system input and each system output respectively, the improvement comprising:

a first of the branches connected to each one of the system inputs having a said resistor means comprising a voltage insensitive resistor of a given magnitude, each said first branch connecting a respective system input with a respective system output, the remaining branches connected to each system output each comprising a voltage sensitive double-pole whose resistance value becomes very great above a predetermined voltage threshold and below said voltage threshold is substantially equal to said given magnitude.

2. In an apparatus as set forth in claim 1, wherein each voltage sensitive double-pole includes a field effect transistor having three connections a first of which is a base connection, a diode and a resistor connected in series between the first and a second of the transistor connections with a first juncture therebetween, a diode and a resistor connected in series between the first and a third of the transistor connections with a second juncture therebetween, a balancing resistor, said junctures and said balancing resistor being connected in series between the branch output and the branch input.

3. In an apparatus as set forth in claim 2 including an operational amplifier having an input and an output connected in the series circuit between the branch input and output, the amplifier output being connected to the first juncture, a negative feedback circuit including a resistor connecting the second juncture with the amplifier input, and a resistor connecting the amplifier input to the branch input.

4. In an apparatus as set forth in claim 1, wherein each voltage sensitive double-pole includes a pair of field effect transistors connected back-to-back by a pair of resistors and in series with a balancing resistor between the branch input and the branch output.

5. In an apparatus as set forth in claim 1, wherein the double-pole includes a cold conductor.

6. In an apparatus for forming the mean value of several input voltages and comprising a plurality of signal inputs, a common signal output, resistor means connected between each of said signal inputs and said common signal output and having a substantially linear resistance characteristic in the normal operating range, and a load resistor connected to said common output, whereby the signal obtained at said common signal output under normal operating conditions is proportional to the arithmetic mean value of said input voltages, the improvement comprising:

at least all but one of said resistor means having a voltage sensitive over-all resistance, which becomes very large above a predetermined voltage threshold defined by the upper end of said normal operating range.

7. In an apparatus as set forth in claim 6, wherein said all but one of said resistor means is a voltage sensitive double pole.

8. In an apparatus as set forth in claim 7, wherein each voltage sensitive double-pole includes a field effect transistor having three connections a first of which is a base connection, a diode and a resistor connected in series between the first and a second of the transistor connections with a first juncture therebetween, a diode and a resistor connected in series between the first and a third of the transistor connections with a second juncture therebetween, a balancing resistor, said junctures and said balancing resistor being connected in series between the branch output and the branch input.

9. In an apparatus as set forth in claim 8 including an operational amplifier having an input and an output connected in the series circuit between the branch input and output, the amplifier output being connected to the first juncture, a negative feedback circuit including a resistor connecting the second juncture with the amplifier input, and a resistor connecting the amplifier input to the branch input.

10. In an apparatus as set forth in claim 7, wherein each voltage sensitive double-pole includes a pair of field effect transistors connected back-to-back by a pair of resistors and in series with a balancing resistor between the branch input and the branch output.

11. In an apparatus as set forth in claim 7, wherein the double-pole includes a cold conductor.

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