United States Patent

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[72] Inventor **Peter F. Aemmer**
Urdorf, Switzerland

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[73] Assignee **Westinghouse Electric Corporation**
Pittsburgh, Pa.
a corporation of Pennsylvania

[54] **DIGITAL ARITHMETIC SYSTEM FOR COMPUTATION OF SQUARE ROOTS AND SQUARES EMPLOYING A RATE MULTIPLIER**
9 Claims, 6 Drawing Figs.

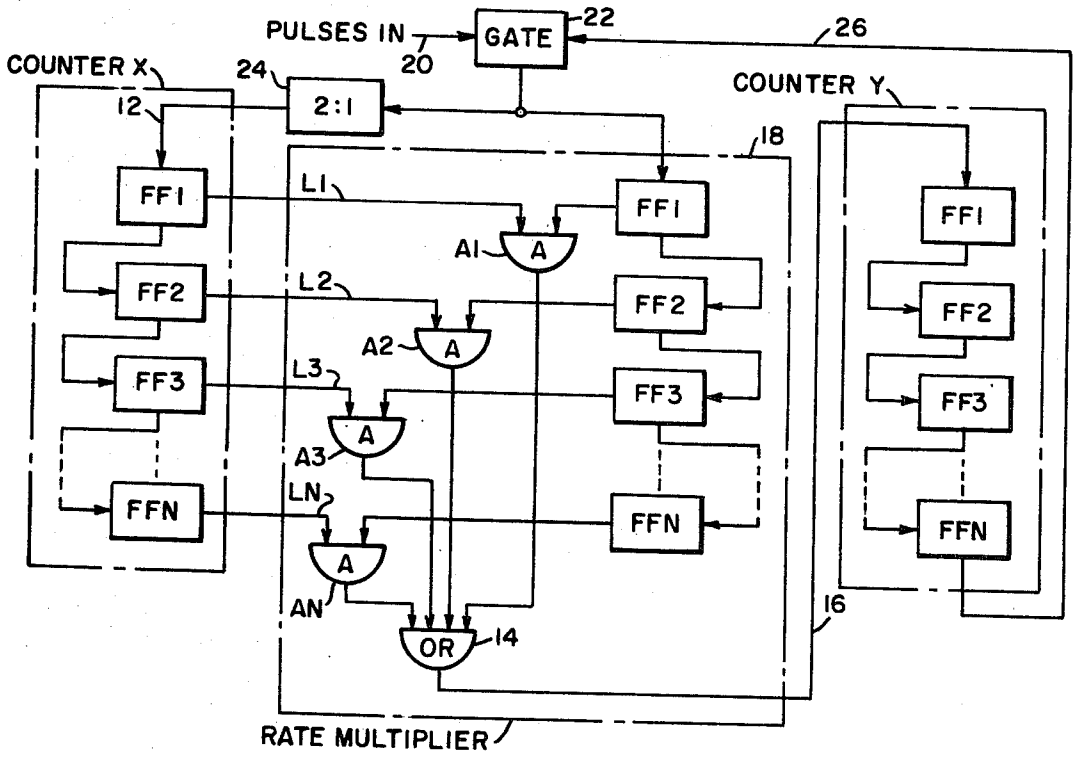
[52] **U.S. Cl.** **235/150.3,** 235/158, 235/193.5
[51] **Int. Cl.** **G06f 7/38,** G06f 7/20
[50] **Field of Search** 235/158, 150.3, 150.31, 150.5, 193.5, 92, 50, 24; 328/142; 307/220, 233

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Primary Examiner—Eugene G. Botz
Assistant Examiner—Joseph F. Ruggiero
Attorneys—F. H. Henson and R. G. Brodahl

ABSTRACT: Described is a digital system, employing only two binary counters and a rate multiplier, capable of extracting the square root of an unknown variable or raising the unknown variable to the power of two. The system is much simpler and less expensive than prior art systems for achieving the same function.



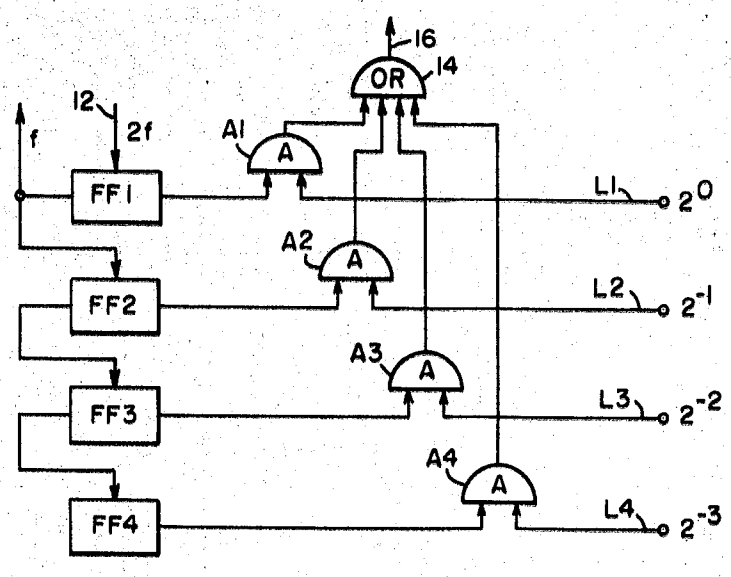


FIG. 1.

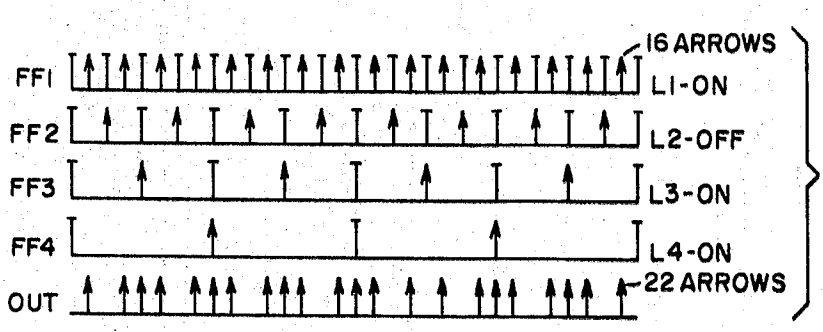


FIG. 1A.

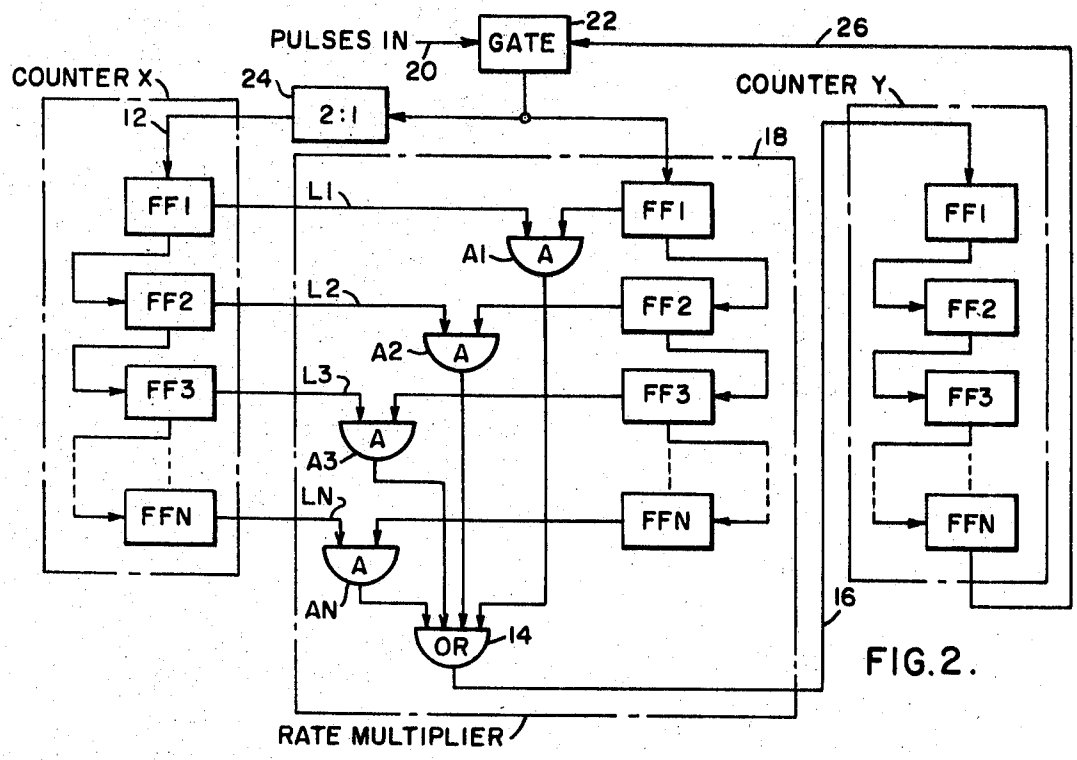


FIG. 2.

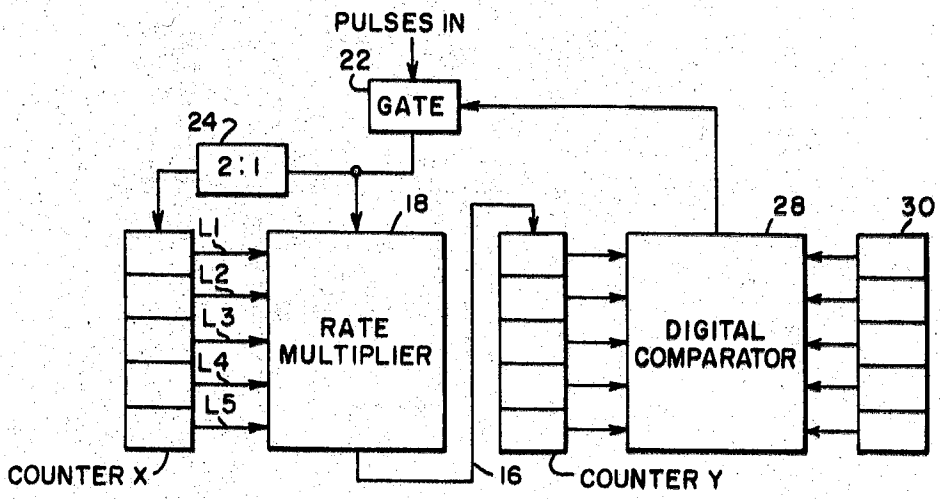


FIG. 3.

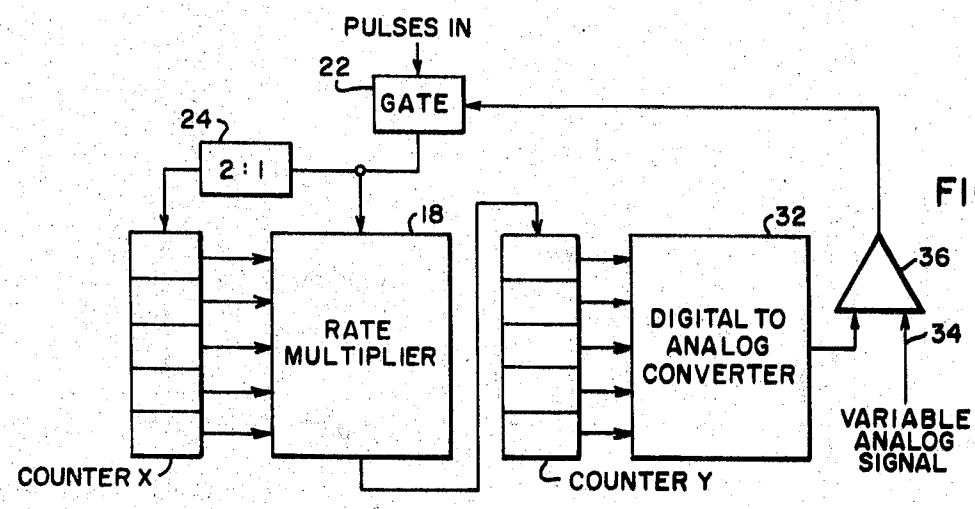


FIG. 4.

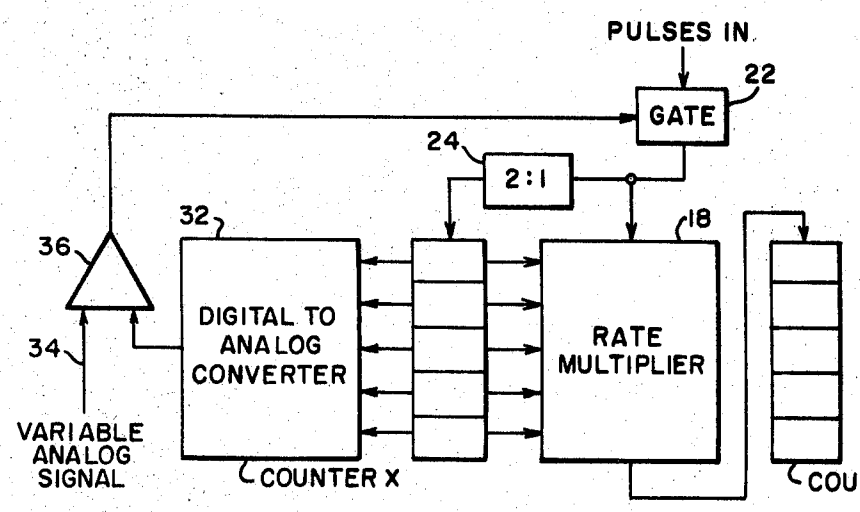


FIG. 5.

DIGITAL ARITHMETIC SYSTEM FOR COMPUTATION OF SQUARE ROOTS AND SQUARES EMPLOYING A RATE MULTIPLIER

BACKGROUND OF THE INVENTION

As it is known, digital methods are becoming increasingly more important in instrumentation systems. Applications may range from digital read-out of analogue sensor signals to the automatic conversion of sensor readings into meaningful engineering and performance quantities. Despite the current popularity of software oriented techniques, it is frequently not economically feasible to install a general-purpose, stored-program digital computer if full use cannot be made of its capacities. With the continuing rapid progress of semiconductor technology, on the other hand, it is now becoming more and more attractive to resort to previously uneconomical hardware systems for performing special-purpose arithmetic operations.

SUMMARY OF THE INVENTION

As an overall object, the present invention seeks to provide new and improved hardware systems for performing special-purpose arithmetic operations.

More specifically, an object of the invention is to provide a new and improved special-purpose circuit for extracting the square root of an unknown variable or for raising the unknown variable to the power of two.

Still another object of the invention is to provide circuitry for computation of square roots and squares employing only a rate multiplier and two binary counters.

In accordance with the invention, a source of pulses is applied to the input of a rate multiplier and is also divided by two in a frequency divider, the output of the frequency divider being applied to a first binary counter. The rate multiplier consists, essentially, of a binary counter in which the output from one side of each of its cascaded flip-flops is combined in an AND circuit with a corresponding output from an associated one of the flip-flops in the first binary counter. The output of the rate multiplier, derived from an OR circuit connected to the aforesaid AND gates, is then fed to the input of a second binary counter. With this arrangement, the count stored in the first counter will always be the approximate square root of the count stored in the second counter.

The above and other objects and features of the invention will become apparent from the following detailed description taken in connection with the accompanying drawings which form a part of this specification and in which:

FIG. 1 is a schematic circuit diagram of a four-bit rate multiplier of the type utilized in the present invention;

FIG. 1A comprises waveforms illustrating the operation of the rate multiplier shown in FIG. 1;

FIG. 2 is a block diagram of one embodiment of the invention;

FIG. 3 is a block diagram of another embodiment of the invention;

FIG. 4 is a block diagram of another embodiment of the invention combined with a digital-to-analogue converter; and

FIG. 5 is a block diagram of still another embodiment of the invention also combined with a digital-to-analogue converter.

With reference now to the drawings, and particularly to FIG. 1, the details of a rate multiplier are shown. It includes a counter comprising a plurality of bistable flip-flops FF1, FF2, FF3 and FF4 connected in cascade. Applied to the input of the counter via lead 12 is a source of pulses having a frequency $2f$. One side of each of the flip-flops FF1 through FF2 is connected to an AND gate A1, A2, A3 or A4 along with digital signals on leads L1, L2, L3 and L4 respectively. The signals on leads L1 through L4 may be derived, for example, from a multiplier register, not shown. The signal on lead L1, when ON, represents the bit 2^0; the signal on lead L2, when ON, represents the bit 2^{-1}; the signal on lead L3, when ON, represents the bit 2^{-2}; and the signal on lead L4, when ON, represents the bit 2^{-3}.

The operation of the rate multiplier of FIG. 1 is illustrated by the waveforms of FIG. 1A wherein the arrows stand for pulses coming out of the right sides of the flip-flops connected to the AND circuits A1 through A4 and the T's stand for pulses coming out of the other side of the flip-flops. Stated in other words, the arrows may be considered as the leading edges of pulses coming out of the right sides of the flip-flops. In the example given, signals on leads L1, L3 and L4 are ON while the signal on lead L2 is OFF. As 32 pulses of frequency $2f$ are applied to the counter via lead 12, 16 pulses will be produced at the right side output of flip-flop FF1; eight pulses will be produced at the output of flip-flop FF2; four pulses will be produced at the output of flip-flop FF3; and two pulses will be produced at the output of flip-flop FF4. It will be noted, moreover, that the leading edges of none of the pulses represented by the arrows in FIG. 1A overlap. Thus, if all of the signals on leads L1 through L4 were ON, 30 pulses would be applied to an OR gate 14 which is the sum of all of the pulses or arrows in the four waveforms shown in FIG. 1A. Since, however, the signal on lead L2 is OFF, those pulses at the output of flip-flop FF2 are not applied to the OR gate 14; and, consequently, only 22 pulses appear at the output lead 16 of the OR gate 14.

From a consideration of the circuit of FIG. 1, and the waveforms of FIG. 1A, it will be appreciated that the number of pulses appearing at the output of the OR circuit 14 will be equal to one-half the number of input pulses applied to flip-flop FF1 times a multiplying factor, M, which is a number equal to the sum of the values represented by the ON binary digits applied to leads L1 through L4. In the example given where ON signals are on leads L1, L3 and L4 only:

$$M = 2^0 + 2^{-1} + 2^{-3} = 1 + \tfrac{1}{2} + \tfrac{1}{8} = 1\tfrac{3}{8}$$

y reference to FIG. 1A, it can be seen that the sum of 22 pulses at the output of OR circuit 14 is equal to 1 ⅜ times the 16 pulses at the output of flip-flop FF1, these 16 pulses being one-half the number of input pulses of frequency $2f$ applied to the flip-flops via lead 12. Note also that the multiplying factor, M, will always be between zero and 1.999, regardless of the number of flip-flops.

With reference now to FIG. 2, one embodiment of the present invention is shown which again includes a rate multiplier 18 in which elements corresponding to those shown in FIG. 1 are identified by like reference numerals; although the flip-flops extend from FF1 to FFN where N is any desired number depending upon the magnitude of the maximum number to be squared. In this case, the leads L1—LN are connected to one side of each of the flip-flops FF1 through FFN of counter X. The output of the rate multiplier, in turn, is applied through lead 16 to the input of counter Y, again comprising a plurality of cascaded flip-flops FF1 through FFN. A source of pulses on lead 20 is applied through gate circuit 22 to the input of rate multiplier 18. This same source of pulses is applied through a two-to-one scaler 24 or frequency divider to the input of the counter X.

Let us assume, for example, that it is desired to derive the square root of a predetermined number. This number is entered into the counter Y and the counter caused to count down. When the counter Y reaches zero, a signal on lead 26 disables the gate 22; and the content of the counter X is now the square root of the predetermined number originally entered into counter Y. This can be explained as follows:

The input-output relationship of the rate multiplier 18 is:

$$df_2 = X \cdot df_1$$

where:

df_2 = change in the number of output pulses from the rate multiplier;

df_1 = change in the number of input pulses applied to the rate multiplier;

X = multiplying factor of rate multiplier. (This will vary as the count of the X counter varies).

The content of the X register, at any instant of time, is equal to the multiplying factor of the rate multiplier **18** and will be equal to:

$$X = \tfrac{1}{2}\int df_1$$

or

$$df_1 = 2d\,X$$

The content of the Y register will be:

$$Y = \int df_2$$

or

$$df_2 = dY$$

By eliminating f_1 and f_2 from the foregoing equations, we obtain the following:

$$dY = 2X dX$$

By integrating both sides, we obtain:

$$Y - Y_o = X^2 - X_o^2$$

where X_o and Y_o are the respective contents of the X and Y registers prior to integration. If both the X and Y registers are initially set to zero, the equation becomes:

$Y = X^2$ with the result that the content of the X register is always the approximate square of the content of the Y register.

In the embodiment of the invention shown in FIG. **2**, the counter X is initially cleared or set to zero while the counter Y is preset with the number which is to be square rooted. The output pulses from the rate multiplier then cause the counter Y to count down until the content of the counter Y is zero, whereupon the pulse on lead **26** will disable the gate **22**. At this time, the content of the counter X will be the approximate square root of the number originally stored in counter Y.

As will be understood, it is not necessary to provide a gate **20**; and both the counter X as well as the counter Y can initially be set to zero. In this manner, at any time, the content of the counter X will be the square root of the content of the counter Y.

In FIG. **3** another embodiment of the invention is shown wherein elements corresponding to those of FIG. **2** are identified by like reference numerals. In this case, the output of counter Y is compared in a digital comparator **28** with the output of a third register or counter **30**, the arrangement being such that when the count of the Y counter, comprising the square of the count of counter X, reaches the count of the counter **30**, the gate **20** is disabled.

Besides being applicable as a convenient method of computing the square root of a digital variable within a sequentially organized special-purpose digital computer, the system of the invention lends itself particularly well to applications in the field of digital instrumentation.

The embodiments of the invention shown in FIGS. **4** and **5** are examples of the system being combined with a digital-to-analogue converter **32**. In FIG. **4**, for example, the analogue-to-digital converter is connected to the output of counter Y; and the output of the digital-to-analog converter **32**, in turn, is compared with a variable analogue signal on lead **34** in differential amplifier **36** such that the gate **22** will be disabled when the analogue output of converter **32**, corresponding to the square of the count in X counter, matches the variable signal on lead **34**. In FIG. **5**, the system is similar except that the digital-to-analogue converter **32** is now connected to the X counter such that the analogue signal at its output is proportional to the square root of the signal in the Y counter. Under equilibrium conditions, in either case, the counter which is connected to the analogue-to-digital converter contains the digital equivalent of the analogue variable, whereas the opposite counter contains the numerical equivalent of the respective square or square root.

Two different modes of operation of the invention can be distinguished. These are a discrete and a quasi-continuous mode. In the discrete mode, the counters X and Y are periodically or aperiodically preset to zero and then released until the system regains equilibrium. Then the result is sampled and stored away. In the quasi-continuous mode, on the other hand, a feedback loop is continuously closed and the servoloop is tracking the analogue input variable. The result is continuously available in the respective register. Obviously, the quasi-continuous mode is much faster than the discrete mode. However, it also requires more logic to provide for tracking in both directions. Also, it is much more sensitive to outside interferences, because errors caused by erroneous pulses tend to accumulate.

Although the invention has been shown in connection with a certain specific embodiment, it will be readily apparent to those skilled in the art that various changes in form and arrangement of parts may be made to suit requirements without departing from the spirit and scope of the invention.

I claim:

1. In a digital arithmetic system for computing square roots and squares, the combination of a rate multiplier capable of producing a number of output pulses equal to the number of input pulses applied thereto times a multiplying factor, first and second counters, means for applying input pulses to said rate multiplier, means for applying input pulses to said first counter at a frequency rate one-half the frequency rate of pulses applied to said rate multiplier, means for connecting said first counter to said rate multiplier whereby the multiplying factor of said rate multiplier, will be a function of the count stored in said first counter, and means for applying output pulses from said rate multiplier, to the input of said second counter whereby the number of pulses applied to said second counter will be the approximate square of the count stored in said first counter.

2. The system of claim **1** wherein the said rate multiplier comprises a plurality of flip-flop units connected in cascade, a plurality of AND circuits corresponding in number to the number of flip-flop units, means connecting one output side of each flip-flop in said rate multiplier to an input terminal of an associated one of said AND circuits, said first counter also comprising a plurality of flip-flop units connected in cascade, means connecting one side of each flip-flop of said first counter to an input terminal to an associated one of said AND circuits, and means connecting the outputs of said AND circuits to an OR circuit, the output of the OR circuit being the output of said rate multiplier.

3. The system of claim **2** wherein said AND circuits have two input terminals only, one of said terminals being connected to an associated flip-flop in said first counter and the other of said terminals being connected to an associated flip-flop in said rate multiplier.

4. The system of claim **1** wherein pulses are applied to said rate multiplier and said first counter through a gate circuit and wherein said second counter is preset to a number whose square root is to be derived, and means for disabling said gate circuit when said second counter counts down to zero whereby the count of said first counter when the gate circuit is disabled will comprise the square root of the number to which said second counter was preset.

5. The system of claim **1** wherein pulses are applied to said rate multiplier and said first counter through a gate circuit and wherein said first and second counters are initially set to zero and count up, a digital comparator connected to said second counter, a register having a digital output representing a number whose square root is to be determined also connected to said comparator whereby the comparator will produce an output when the count of the second counter matches the digital output of said register, and means for applying said output from the digital comparator to said gate circuit whereby the gate circuit will be disabled when the count of said second counter matches the digital output of said register.

6. The system of claim 1 wherein said multiplying factor is in the range between zero and 1.999.

7. The system of claim 4 wherein the output of said second counter is applied to a digital-to-analogue converter, the output of the digital-to-analogue converter being compared with a variable analogue, and means for disabling said gate circuit when the output of said digital-to-analogue converter matches said variable analogue.

8. The system of claim 4 wherein the count stored in said first counter is applied to a digital-to-analogue converter and the output of said digital-to-analogue converter is compared with a variable analogue signal, and means for disabling said gate circuit when said variable analogue signal matches the output of said digital-to-analogue converter.

9. The system of claim 4 wherein input pulses are applied through said gate circuit directly to said rate multiplier and through a frequency divider to said first counter.