(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 967 723 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
29.12.1999 Bulletin 1999/52

(51) Int. Cl.[6]: **H03K 19/173**

(21) Application number: **98122505.5**

(22) Date of filing: **27.11.1998**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **28.05.1998 US 85826**

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(54) Programmable pin designation for semiconductor devices

(57) The invention allows the programmer to designate one or more pins on a semiconductor device as either address pins, which are in addition to a predetermined set of address lines or as alternate I/O pins. The object of the invention is to provide the programmer with the capability of defining with preciseness the particular size of the address bus needed for a specific application. The invention is comprised of a programming port, optional programing logic, configuration logic, selection logic and a set of pins that may be configured as per the programmer's requirements. The invention is to exist on a single, monolithic semiconductor device.

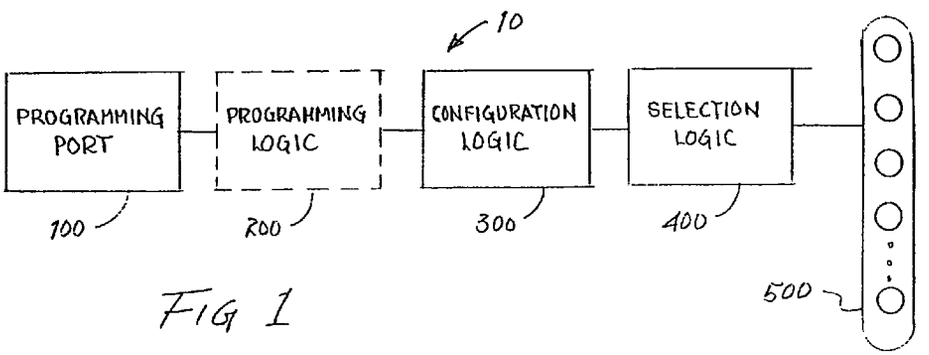

FIG 1

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention:

[0001] This invention relates generally to semiconductor device pin designation. Specifically, the present invention relates to the ability of the user to programmably designate one or more semiconductor device pins to perform an expanded and flexible set of address functions, as well as other I/O functions.

2. Description of the Prior Art:

[0002] The current state of the art describes semiconductor devices such as microprocessors and microcontrollers that have bi-directional I/O ports to a common pin that are capable of performing one function when in the input mode and a second function when in the output mode.

[0003] The current state of the art also describes semiconductor devices such as microprocessors and microcontrollers that are capable of using a particular pin as either an address pin or a data pin, depending on state of the device with respect to the memory access cycle. For example, a microprocessor capable of driving a 16 bit wide data bus is likely to have 16 pins that function as data I/O. The microprocessor has an internal capability that allows the same 16 pins to drive an address bus. If additional addressing capability is needed, then additional pins must be dedicated to fulfill this need. Under the prior art, the internal architecture of address pin assignments is defined by the semiconductor manufacturer and cannot be modified by the user.

[0004] The prior art, as found in U.S. Patent 5,686,844, "INTEGRATED CIRCUIT PINS CONFIGURABLE AS A CLOCK INPUT PIN AND AS A DIGITAL I/O PIN OR AS A DEVICE RESET PIN AND AS A DIGITAL I/O PIN AND METHOD THEREFOR," describes semiconductor devices with the capability of configuring integrated circuit (IC) pins as clock/reset signals or other digital I/O.

[0005] Other schemes have described a multifunctional pin approach for test circuits, which purport to test multiple segments of memory simultaneously. See U.S. Patent 4,495,603, "TEST SYSTEM FOR SEGMENTED MEMORY." However, this prior art describes the introduction of a "logic box" which contains little more than tri-state buffers that generate read and write test clocks for segmented memory devices. Furthermore, there is no suggestion that these test circuits or "logic boxes" are integral to the processing unit and thus are not programmable for customizing the I/O function of the processing unit.

[0006] U.S. Patent 5,473,758, "SYSTEM HAVING INPUT OUTPUT PINS SHIFTING BETWEEN PROGRAMMING MODE AND NORMAL MODE TO PROGRAM MEMORY WITHOUT DEDICATING INPUT OUTPUT PINS FOR PROGRAMMING MODE," claims a common set of processing unit I/O pins to function in either a programming mode (e.g. programming non-volatile memory) or a normal mode (e.g. executing program memory).

[0007] Thus, a problem is created that manifests itself as either insufficient or excessive addressing capability, depending on the programmer's application. Furthermore, the prior art does not anticipate a flexible addressing capability that may be programmed for the specific application of the semiconductor device.

[0008] Therefore, a need existed to provide a semiconductor device where the number of address pins required to meet the design specification may be programmably designated.

SUMMARY OF THE INVENTION

[0009] It is an object of the present invention to provide a system that will permit the user to designate the function of one or more semiconductor device pins.

[0010] It is another object of the present invention to provide a system that will permit the user to program the designation of semiconductor device pins as either address pins or standard I/O pins.

[0011] It is another object of the present invention to provide a system that will allow the user to permanently program a semiconductor device for the purpose of designating the function of the semiconductor device pins.

[0012] It is another object of the present invention to provide a system that will allow the user to alterably program a semiconductor device for the purpose of designating the function of the semiconductor device pins.

[0013] It is another object of the present invention to provide a system that is capable of encoded designation of semiconductor device pins.

[0014] It is still another object of the present invention to provide a system that is capable of non-encoded designation of semiconductor device pins.

[0015] In accordance with one embodiment of the present invention, a system for programably designating semiconductor pins comprises a programming port, configuration logic, selection logic and at least one pin, which may be programmably designated to perform one of a plurality of I/O functions. This embodiment may further comprise a plurality of semiconductor pins, which are predesignated and unalterable, to perform memory address functions. Furthermore, in this embodiment, the above elements and features are co-located on a single, monolithic semiconductor device.

[0016] In accordance with another embodiment of the present invention, a system for programmably designating semiconductor pins comprises a programing port, programing logic, configuration logic, selection logic and at least one pin which may be programmably designated to perform one of a plurality of I/O functions. This embodiment may further comprise a plurality of semi-

conductor pins, which are predesignated and unalterable, to perform memory address functions. This embodiment may further comprise of decoding pin designation assignments from an encoded format. Furthermore, in this embodiment, the above elements and features are co-located on a single, monolithic semiconductor device.

[0017] The foregoing and other objects, features, and advantages of the invention will be apparent from the following, more particular, description of the preferred embodiments of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018]

Figure 1 is a block diagram of the present invention.
Figure 2 is a diagram of one embodiment of the selection logic.
Figure 3 is a diagram of another embodiment of the selection logic with decoding capability.
Figure 4 is a diagram of an application of the present invention illustrating expanded address functions and chip select.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0019] Referring to Figure 1, a block diagram of the present invention 10 is shown. The programmable pin designation for semiconductor devices 10 [hereinafter "system"] is comprised of a programming port 100, optional programming logic 200 (shown in dashed lines to indicate an optional, not a required, element), configuration logic 300, selection logic 400 and at least one pin 500, which may be programmably designated to perform one of a plurality of I/O functions. The system is further comprised of a plurality of semiconductor pins which are predesignated and unalterable, to perform a memory address function. These pins are shown in figure 4 as AD_m:AD_0, which is a diagram demonstrating several applications of the invention. In the preferred embodiment, the elements described above are co-located on a single, monolithic semiconductor device.

[0020] The importance of the invention is to provide a semiconductor device such as a microcontroller, microprocessor or other devices capable of performing memory access with a flexible, programmable method of selecting the precise address range required for the application. The objective of the invention is to optimize the number of semiconductor pins needed for memory address functions and quasi-address functions such as chip select.

[0021] The programming port 100 may be either a serial or parallel I/O port of various formats, standards and protocols which are well known to those skilled in the art. The programming port has several functions. The port 100 accepts semiconductor pin configuration data from a programming device that is beyond the scope of the invention, but is well known to those skilled in the art of computer science. The port 100 may also output the current configuration of the semiconductor pins to external devices. Also, the port 100 may be used for test purposes.

[0022] In one embodiment, the configuration data is transmitted via the programming port directly to the configuration logic 300 where it is stored. In an alternative embodiment, the configuration data is read by the programming logic 200, which may be a processing unit. The configuration data is interpreted by the programing logic 200. The interpretted form of the configuration data is stored in the configuration logic 300.

[0023] The configuration logic 300 may include one of a number of implementations. In one embodiment, the configuration logic 300 may be a simple register or a location within a programmable volatile or non-volatile memory array. Thus, in this embodiment, the configuration data stored in the configuration logic may be modified at the discretion of the programmer. Alternatively, the configuration logic may encompass one time only programmable logic such as a programmable read only memory (PROM) or other types of fusible devices known to those skilled in the art.

[0024] Referring to figures 1, 2, and 3, wherein like numerals represent like elements, the selection logic 400 is shown. The selection logic provides the decision mechanism for designating semiconductor pin functions. The selection logic 400 is comprised of a series of multiplexers 410 in the preferred embodiment. In another embodiment, the selection logic includes both the series of multiplexers 410 and one or more decoders 420.

[0025] Figure 1 shows that the selection logic 400 provides the bridge between the data stored in the configuration logic 300 and the semiconductor pins 500. Figure 2 shows a non-encoded form of the selection logic 400 where there is one to one mapping between each bit of the configuration logic 300 and the select input for each multiplexer 410. Figure 3 shows an encoded form of the selection logic 400 where the configuration data is stored in an encoded format. The encoded data is then decoded by decode logic 420 and then coupled to the select inputs of the multiplexers 410.

[0026] The inputs of the multiplexers 410 are either expanded address lines or other I/O functions performed by a semiconductor device. The outputs of the multiplexers 410 are connected to the semiconductor pins 500, either directly or through a buffer.

[0027] Referring to figure 4, a typical application of the present invention 10 is shown. The present invention 10 is embodied in block 20, which represents a processing unit such as a microprocessor or microcontroller. The application also illustrates memory device 30 and peripheral device 40. The address latch 50 is also illustrated.

[0028] AD_m:AD_0 in block 20 represents a predesignated set of pins with an address function. In this example, these pins may be coupled to the data bus in addition to driving the address bus. However, in other embodiments the predesignated set of address pins may not be multiplexed with the data bus function, thus obviating the requirement for the address latch 50. The predesignated nature of the address function of the semiconductor pins corresponding to AD_m:AD_0 may not be altered or modified by the programmer.

[0029] The memory device 30 and peripheral device 40 have addressable memory locations which exceed that provided for by the range defined by AD_m:AD_0. Therefore, addition memory addressing capability is required. The programmer defines the expanded addressing as A_n:A_{m+1}, where $n \geq m+1$. This data is stored in the configuration logic 300 and the selection logic 400 determines the semiconductor pin 500 assignments (figures 1-3).

[0030] Also in this application, because there may be redundancy in addressable memory locations as between memory device 30 and peripheral device 40, chip select logic is shown. Chip select logic is represented in block 20 as $ADDR_x$ and $ADDR_y$. By designating these pins as chip selects in the same manner as described above for expanded address pins, the appropriate memory/peripheral device is accessed. Thus, the present invention allows for flexible designation of IC pins for addressing, which precisely matches the addressing requirements of the design specification. Those pins not used for addressing are available for other I/O functions.

[0031] Although the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that changes in form and detail may be made therein without departing from the spirit and scope of the invention.

Claims

1. A system for programmably designating semiconductor device pins comprising, in combination:

   a programing port for receiving a plurality of pin designation instructions;
   configuration logic coupled to the programing port for storing the plurality of pin designation instructions;
   selection logic coupled to the programing port for selecting the function of at least one pin designation; and
   at least one pin coupled to the selection logic and that is programably designated to perform one of a plurality of I/O functions.

2. The system in accordance with Claim 1 further comprising a plurality of pins with a predesignated address function.

3. The system in accordance with Claim 2 further comprising programing logic coupled to the programing port for interpreting the plurality of pin designation instructions.

4. The system in accordance with Claim 3 wherein the programing port, the configuration logic, the selection logic, the at least one pin and the plurality of pins with the predesignated address function are all located on a single, monolithic semiconductor device.

5. The system in accordance with Claim 1 wherein the programming port for receiving a plurality of pin designation instructions is a serial port.

6. The system in accordance with Claim 1 wherein the programing port for receiving a plurality of pin designation instructions is a parallel port.

7. The system in accordance with Claim 1 wherein the configuration logic is comprised of at least one register.

8. The system in accordance with Claim 1 wherein the configuration logic is comprised of a fusible device.

9. The system in accordance with Claim 1 wherein the configuration logic is comprised of non-volatile memory.

10. The system in accordance with Claim 1 wherein the selection logic is comprised of at least one multiplexer.

11. The system in accordance with Claim 1 wherein the at least one pin may be designated as an address pin.

12. The system in accordance with Claim 2 wherein the at least one pin may be designated as an address pin that expands an addressable memory range beyond that provided by the plurality of address pins with the predesignated address function.

13. The system in accordance with Claim 1 wherein the at least one pin may be designated as a chip select pin.

14. The system in accordance with Claim 2 wherein the at least one pin may be designated as a chip select pin that provides for expanding an addressable memory range beyond that provided by the plurality of address pins with the predesignated address function.

15. The system in accordance with Claim 3 wherein the programming logic is comprised of a processing unit that interprets the plurality of pin designation instructions and stores a plurality of pin designation commands within the configuration logic.

16. The system in accordance with Claim 15 wherein the plurality of pin designation commands are encoded commands.

17. The system in accordance with Claim 3 wherein the selection logic is comprised of at least one multiplexer.

18. The system in accordance with Claim 17 wherein the selection logic is further comprised of decoding logic for decoding the plurality of pin designation commands.

19. A method for programmably designating semiconductor pins comprising the steps of:

providing a plurality of pin designation instructions to a programming port;
providing at least one configuration register to store the plurality of pin designation instructions received from the programming port;
providing selection logic that is controlled by the pin designation instructions stored in the at least one configuration register for selecting one of a plurality of I/O functions; and
providing at least one pin coupled to the selection logic and that is programmably designated to perform one of the plurality of I/O functions.

20. The method in accordance with Claim 19 further comprising the step of providing a plurality of pins with a predesignated address function.

21. The method in accordance with Claim 20 further comprising the step of providing programming logic coupled to the programming port for interpreting the plurality of pin designation instructions.

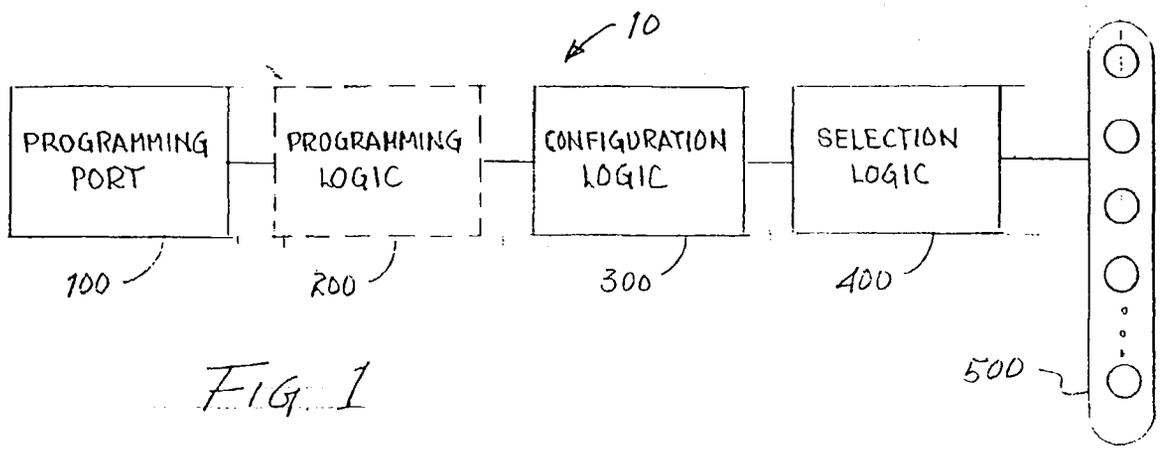

10
PROGRAMMING PORT
PROGRAMMING LOGIC
CONFIGURATION LOGIC
SELECTION LOGIC
100
200
300
400
500

FIG. 1

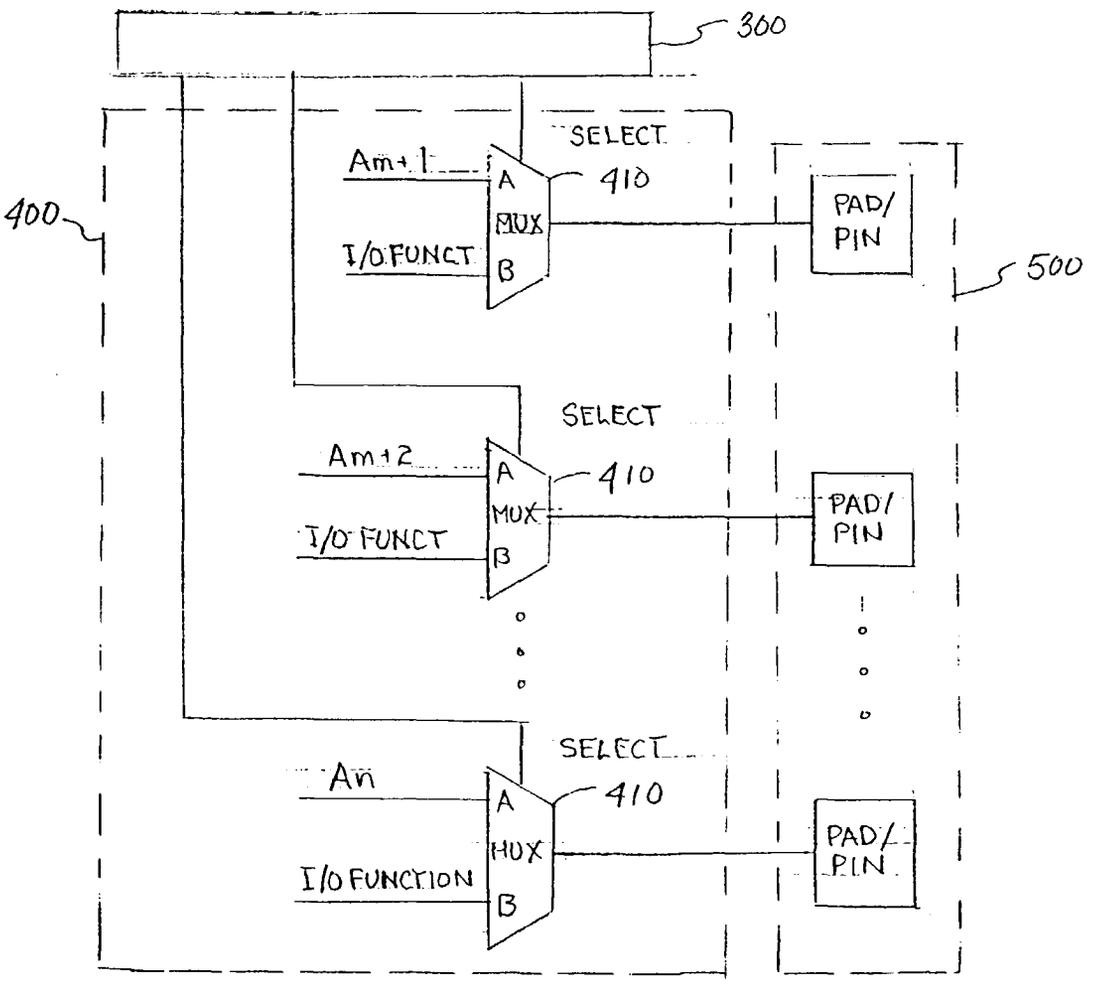
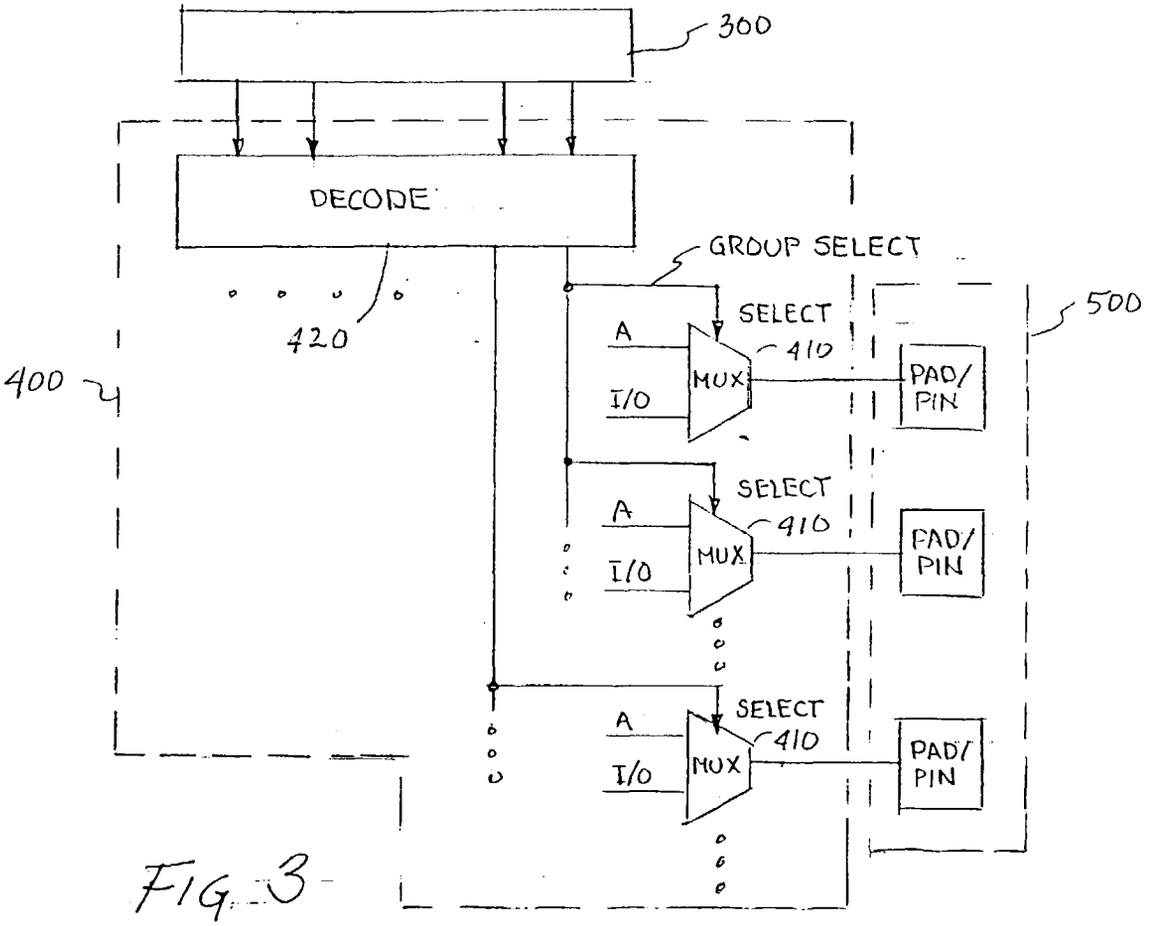

300
400
500
SELECT
Am+1
I/O FUNCT
A
MUX
B
410
PAD/ PIN
SELECT
Am+2
I/O FUNCT
A
MUX
B
410
PAD/ PIN
SELECT
An
I/O FUNCTION
A
MUX
B
410
PAD/ PIN

FIG. 2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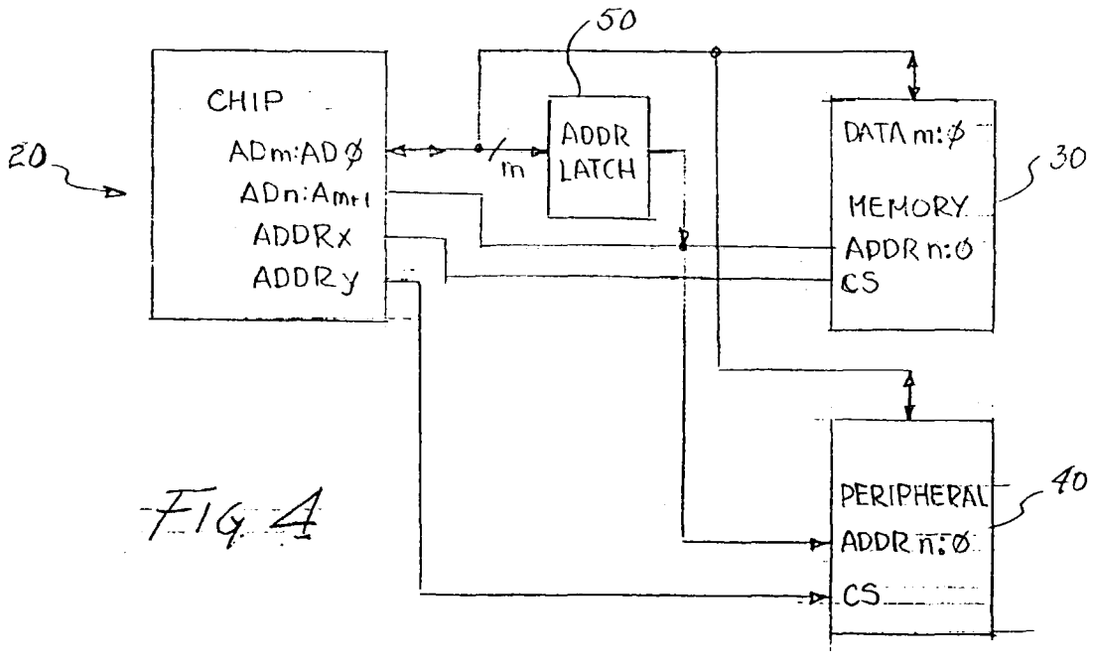
DECODE
GROUP SELECT
420
400
500
SELECT
410
A
I/O
MUX
PAD/
PIN

FIG. 3


50
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ADn:Am+1
ADDRx
ADDRy
m
ADDR
LATCH
DATA m:∅
MEMORY
ADDR n:0
CS
30
PERIPHERAL
ADDR n:∅
CS
40

FIG. 4