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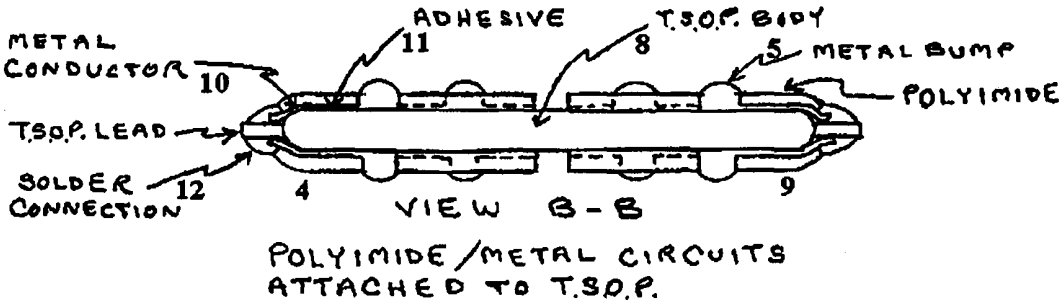

(57) Abstract

A structure and process are disclosed in which IC chip–containing layers are stacked to create electronic density. Each layer is fabricated by forming one or more flexible circuit (4, 9) around a TSOP (8). Each flexible circuit (4, 9) contains conductors (10) which are disposed to connect with TSOP leads, transpose signals to or from various locations on the top or bottom of the TSOP (8), and/or terminate in ball grid contacts (5) for connection to other layers in the stack. The flexible circuits (4, 9) are bonded to the TSOP (8) such that ball grid contacts (5) are exposed on the top and bottom of the TSOP (8), and the ball grid array contacts (5) on the bottom of the lowest layer are disposed to facilitate connection with a PCB or other circuitry.

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IC STACK UTILIZING FLEXIBLE CIRCUITS WITH BGA CONTACTS

Background of the Invention

This invention relates to the stacking of layers containing IC (integrated circuit) chips, thereby obtaining high density electronic circuitry. In general, the goal of the present invention is to combine high circuit density with reasonable cost. A unique aspect of this invention is that it stacks IC layers as TSOP's (thin small outline packages) in a footprint smaller than the TSOP footprint itself. Cost reduction is accomplished by relatively low cost forming of individual layers and the ability to incorporate off-the-shelf prepackaged and pre-tested IC's into stacks.

Another aspect of successful stacking of chip-containing layers is the ability of the BGA (ball grid array) interconnection to cheaply provide a large number of non-common (non-bussed) connections between individual layers themselves and the substrate to which the stack is attached.

The prior art contains several examples where a flexible circuit is used to interconnect unpackaged chips. Yamaji Patent No. 5,394,303 shows a structure in which a flexible film with wiring layers is wrapped around a semiconductor chip, providing an increase in the number of terminals and a second surface for interconnections. McMahon Patent No. 5,362,656 shows a structure in which a flexible circuit is used to route signals from interconnections with the top surface of the chip to ball connectors below the chip substrate. Paurus et al. Patent No. 5,448,511 and Kimura Patent No. 5,313,416 disclose schemes for creating a memory stack by interconnecting a series of memory

devices or memory IC chips on a fan-folded flexible circuit board which carries the signals from the various IC chips to each other and out the bottom of the stack to the main PCB. Behelen et al. Patent No. 5,598,033 shows a structure in which a flexible circuit is used to interconnect a semiconductor IC die to BGA contacts on another die displaced laterally, so that two stacks of dice can be interconnected in a zigzag manner.

What is not available in the prior art is a stack of IC chip-containing TSOP layers which are fully tested individually prior to stacking, can connect layers in the stack with each other and with the bottom surface of the stack using BGA's, and can provide custom interconnections including the separate connection of individual layer signals to the bottom of the stack. The current invention allows a large I/O count for mixed IC stacking or wide data paths, such as the assembly of wide word memory from layers of memory IC's having smaller word widths. Additionally, the current invention allows stacks having a smaller footprint than their constituent TSOP's, and allows them to be produced at low cost.

Summary of the Invention

This application discloses a version of a fully pre-tested IC-containing layer, which can be stacked and electrically connected by ball grid array contacts on each level of the stack. This application further discloses a method for starting with a standard TSOP package and manufacturing an IC-containing layer with ball grid array contacts ready for stacking with other layers

in order to provide a dense electronic package.

The TSOP leads are trimmed close to the TSOP body. At this point, the edges of the TSOP body may be mechanically rounded to improve the bending radius of the applied flexible circuit. A flexible circuit containing conductors with exposed sections prepared for joining with the TSOP leads, and other exposed sections prepared with bumps suitable for use as ball grid contacts is fabricated, with the conductors arranged so as to give the desired connections. Using an appropriately shaped heated fixture, the flexible circuit is formed into such a shape that it will slip over one of the leaded edges of the TSOP. The flexible circuit is then bonded to the TSOP such that the appropriate exposed conductors of the flexible circuit contact the trimmed leads of the TSOP. The assembly is then dipped into high-melting-temperature solder in order to accomplish a soldered connection between the trimmed TSOP leads and the contacting exposed conductors of the bonded flexible circuit.

Each layer is completed before stacking. Ordinarily, pre-tested TSOP's can be used, eliminating the requirement for testing. For special applications, additional testing may conveniently be accomplished by testing the ball grid array layer using a production-testing fixture which contacts the ball grid contacts. Functional testing may include:

Testing at extreme temperatures (e.g., minus 55°C to plus 125°C);

Burned in (both temperature and bias); and

Environmentally screened (i.e., temperature cycle, thermal shock, humidity, bias)

The availability of the full top and bottom surfaces of the layer for ball grid terminals, the ability to transpose connections to different ball grid contact positions by arranging the geometry of the conductors in the flexible circuit, and the large number of vertical interconnections, allow for a very high input/output (I/O) count to accommodate the needs of the stacked IC's.

Further, this application discloses stacked IC-containing devices having a smaller footprint than the original TSOP's used to make them, and methods for stacking the IC-containing layers to produce stacked IC-containing devices.

Brief Description of the Drawings

Figure 1 shows a side view of a standard TSOP and a TSOP with the leads trimmed.

Figure 2 shows a side view of the TSOP after rounding of the package edges.

Figure 3 shows a partial view of a flexible polyamide/metal conductor circuit.

Figure 4 shows an exploded view of a severed conductor in the polyamide hole.

Figure 5 shows a side view of flexible circuit of figure 3 before hot forming, and the same circuit after hot forming around the TSOP.

Figure 6 shows a top view and side view of the BGA/TSOP assembly complete with two flexible circuits formed and bonded to it.

Figure 7 shows an example four-high stack of BGA/TSOP assemblies with their BGA contacts joined with solder connections.

Figure 8 shows two layers of a flexible circuit and illustrates the ability to make unique contact to upper layers in a stack.

Detailed Description

This invention consists of a stack of semiconductor IC's electrically and mechanically interconnected in the vertical direction. The end user of this stack will connect it to a substrate such as a printed circuit board (PCB). The vertical placement of IC's will save considerable substrate area as opposed to the conventional horizontal placement of an equivalent number of IC's on the substrate.

Each layer within the stack will consist of an off-the-shelf commercially available IC **1** in a thin small outline package (TSOP) processed in such a manner as to route the TSOP's electrical input/output (I/O) connections from the leads on the sides or the ends of the package to an array of metallic bumps or a ball grid array (BGA) on both the top surface and the bottom surface of the TSOP package. The routing process consists of the following steps:

Trim the TSOP's leads close to the TSOP body to approximately .015". A trimmed TSOP **2** is illustrated in Figure 1.

The edges of the TSOP package may be optionally rounded **3** to

reduce the bending radius of the polyimide/conductor circuit to be applied in step 7. A rounded TSOP package **3** is illustrated in Figure 2. Fabricate a polyimide/metal conductor circuit **4** as shown in figure 3 containing conductors with ends that, through vias in the polyimide, terminate on metal balls or bumps **5** (achieved by electroplating or other methods). There is a hole in the polyimide **6** exposing a conductor element **7** near their mid-section where the conductor is intended to be joined with the TSOP leads on one side or end of the package. A second circuit will be fabricated to contact the leads on the opposite side or end of the TSOP package.

Using an appropriate fixture, sever the conductors **7** exposed in holes in the polyimide as shown in Figure 4.

Using an appropriate heated fixture resembling the approximate shape of the TSOP, hot form the polyimide/metal conductor circuit into such a shape that it will slip over one of the leaded edges of the TSOP **8** as shown in Figure 5. A second polyimide/conductor circuit similarly formed **9** will slip over the second leaded edge of the TSOP.

Apply a thermosetting epoxy adhesive to the top and bottom sides of the TSOP and partially cure the adhesive.

Slide the hot formed polyimide/metal conductor circuits over each side of the TSOP such that the trimmed TSOP leads penetrate the polyimide holes in the circuit and contact the severed metal conductors **10**.

Using an appropriate fixture to hold the assembly in place, cure the epoxy adhesive **11** as shown in Figure 6.

Dip the edges of the TSOP having leads into a high melting temperature solder **12** to accomplish an electrical connection between the TSOP trimmed leads and the severed and formed metal conductors within the polyimide/metal conductor circuit as shown in Figure 6.

At this point the TSOP's electrical connections have been re-routed from the leads on the sides or ends of the body to a BGA on the top surface and/or the bottom surface of the TSOP's. It should be noted that not all bumps or balls **5** in the BGA are to be connected to a TSOP lead. Some conductors will use the space between leads simply to connect a ball or bump on the top TSOP surface with a ball or bump on the bottom TSOP surface. When the TSOP's are stacked, this allows for independent electrical connection from the bottom of the stack to individual TSOP's in the stack.

The processed TSOP's are now ready for stacking which is accomplished by printing or dispensing a high melting point solder part to the BGA locations on the top surface and/or the bottom surface of the processed TSOP's and then reflowing the solder paste in a convection or vapor phase reflow furnace (see figure 7). The solder **14** used in stacking and in connecting the polyimide/conductor circuit to the TSOP leads should have a melting point higher than the temperature the end user will use to connect the stack to the substrate.

What is unique about this invention is that it stacks TSOP's in a footprint smaller than the TSOP footprint itself and that the BGA interconnection between the layers of the stack provides for a large number of non-common

(non-bussed) connections between individual layers themselves and individual layers and the substrate to which the stack is attached.

Figure 8 demonstrates how electrical contact **14** can be made vertically in the stack so as to connect each TSOP's pin 1 in common and bring it to the base of the stack. It also demonstrates how the pin 2 of a layer 1 TSOP **15** and pin 2 of a layer 2 TSOP **16** can each be brought out separately to different locations at the base of the stack. This re-route scheme continues for multiple layers of the stack enabling the ability to expand memory depth and memory width beyond that of the TSOP's in the stack and to stack IC's (other than memory) in the stack.

From the foregoing description, it will be apparent that the device and method disclosed in this application will provide the significant functional benefits summarized in the introductory portion of the specification.

The following claims are intended not only to cover the specific embodiments disclosed, but also to cover the inventive concepts explained herein with the maximum breadth and comprehensiveness permitted by the prior art.

What is claimed is:

1. A stack of IC chip-enclosing layers, comprising:

an IC-containing layer comprising:

a TSOP containing one or more IC chips and having I/O terminals thereon; and

a flexible circuit, with exposed solderable contacts for connection to the TSOP terminals and ball grid contacts for connection with other layers in the stack, formed to fit over each terminal-bearing side of the TSOP; and

a second IC-containing layer with ball grid contacts, supported on top of the lower layer and connected to the first layer via their respective ball grid contacts.

2. The structure of claim 1 in which:

additional IC chip-containing layers are supported and connected on the top of the second layer.

3. The structure of claim 1 in which:

the ball grid contacts on the upper surface of one or more layers do not all electrically connect with the corresponding ball grid contacts on the lower surface of the layer.

4. The structure of claim 1 in which:

flat bump connectors are used instead of ball grid connectors.

5. The structure of claim 1, in which:

one or more terminal-bearing sides of the TSOP in one or more layers are mechanically rounded to increase the bending radius of the flexible circuit.

6. A method of manufacturing an IC-containing layer ready for stacking with other layers in order to provide a dense electronic package, comprising the steps of:

fabricating a flexible circuit with its electrical conductors disposed to provide the desired connector geometry for connection of a TSOP with other layers;

forming the flexible circuit so that it fits over a lead-bearing side of a TSOP; and

bonding the flexible circuit to the TSOP so as to align exposed conductors of the flexible circuit in solderable contact with the TSOP leads.

7. The method of claim 6 which also comprises:

fabricating, forming, and bonding a second flexible circuit over the other lead-bearing side of a TSOP

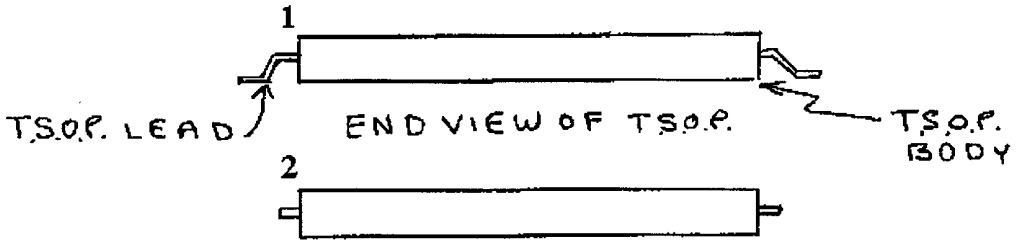
8. The method of claim 7 in which the flexible circuits provide a ball grid array covering the entire top and bottom of the layer.

9. The method of claim 6 which also comprises:
stacking a plurality of the layers; and
electrically interconnecting conductors in each layer with conductors in the adjacent layer.

10. The method of claim 9 in which pre-tested TSOP's are utilized.

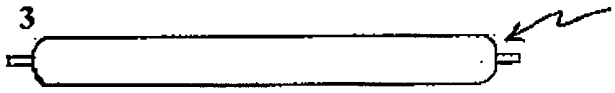
11. The method of claim 9 which also comprises:
testing, prior to stacking, for performance of the circuitry of each layer to establish the layer as a known good element.

12. The method of claim 11 in which the performance testing includes testing at extreme temperatures, testing through thermal cycles and thermal shock, and testing for performance under humidity conditions.



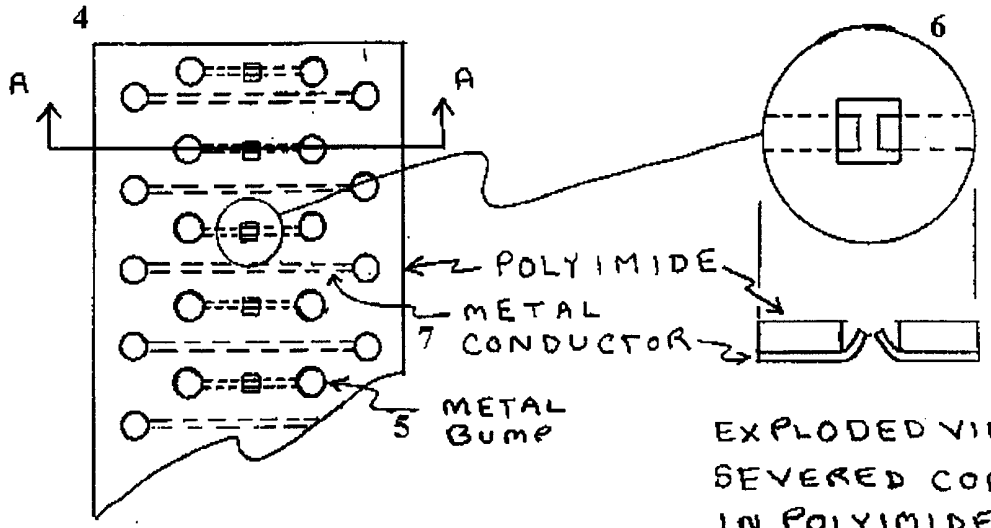
END VIEW OF TSOP. WITH LEADS TRIMMED

FIGURE 1



END VIEW OF T.S.O.P. AFTER EDGE ROUNDING (OPTIONAL)

FIGURE 2

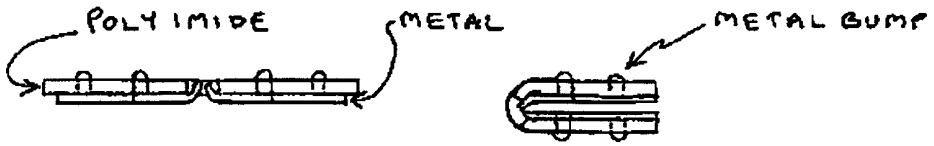


PARTIAL VIEW OF POLYIMIDE/METAL CONDUCTOR CIRCUIT

FIGURE 3

EXPLODED VIEW OF SEVERED CONDUCTO IN POLYIMIDE HOLE

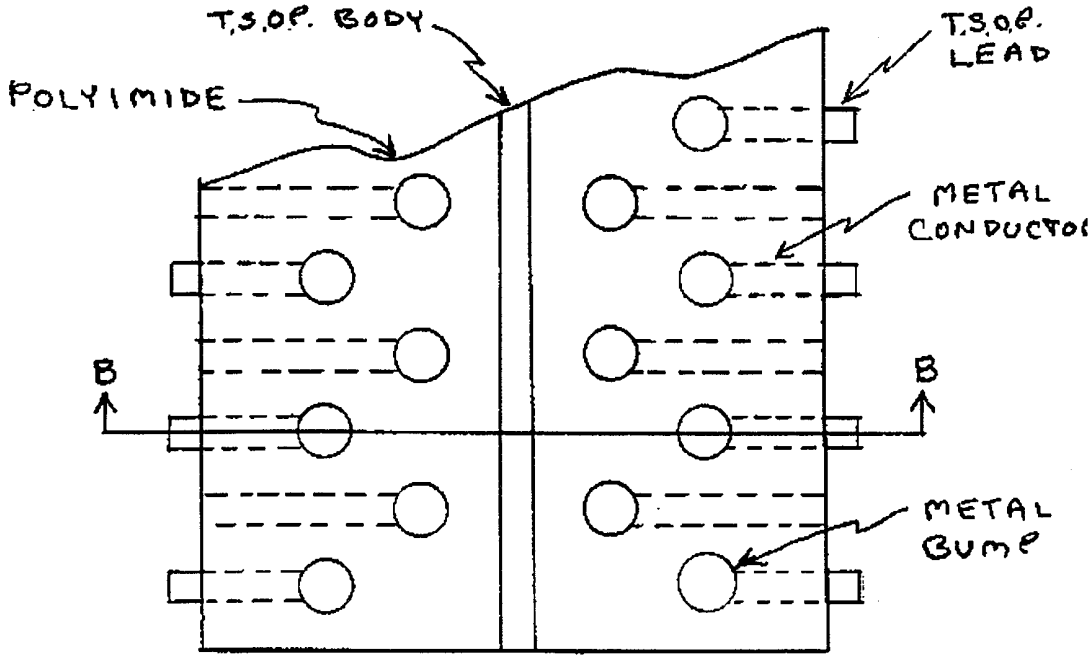
FIGURE 4

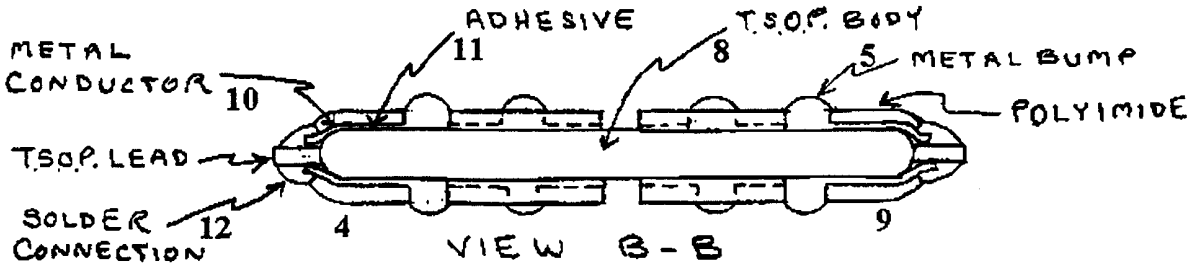


VIEW A-A FROM FIGURE 3 BEFORE HOT FORMING

VIEW A-A FROM FIGURE 3 AFTER HOT FORMING

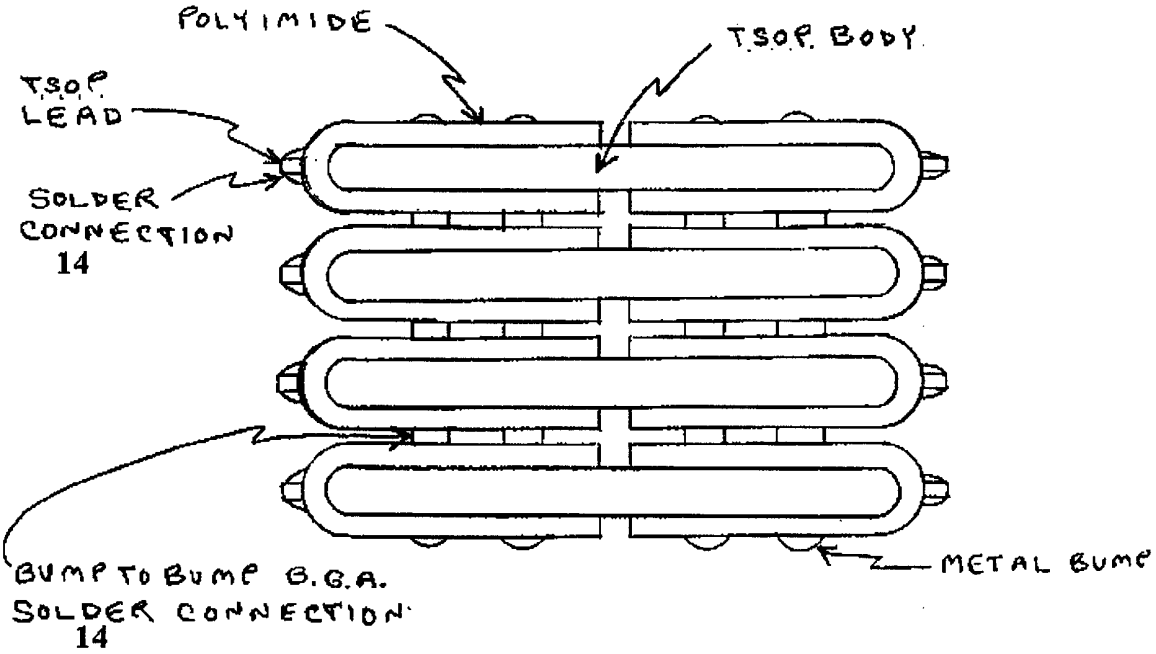
FIGURE 5





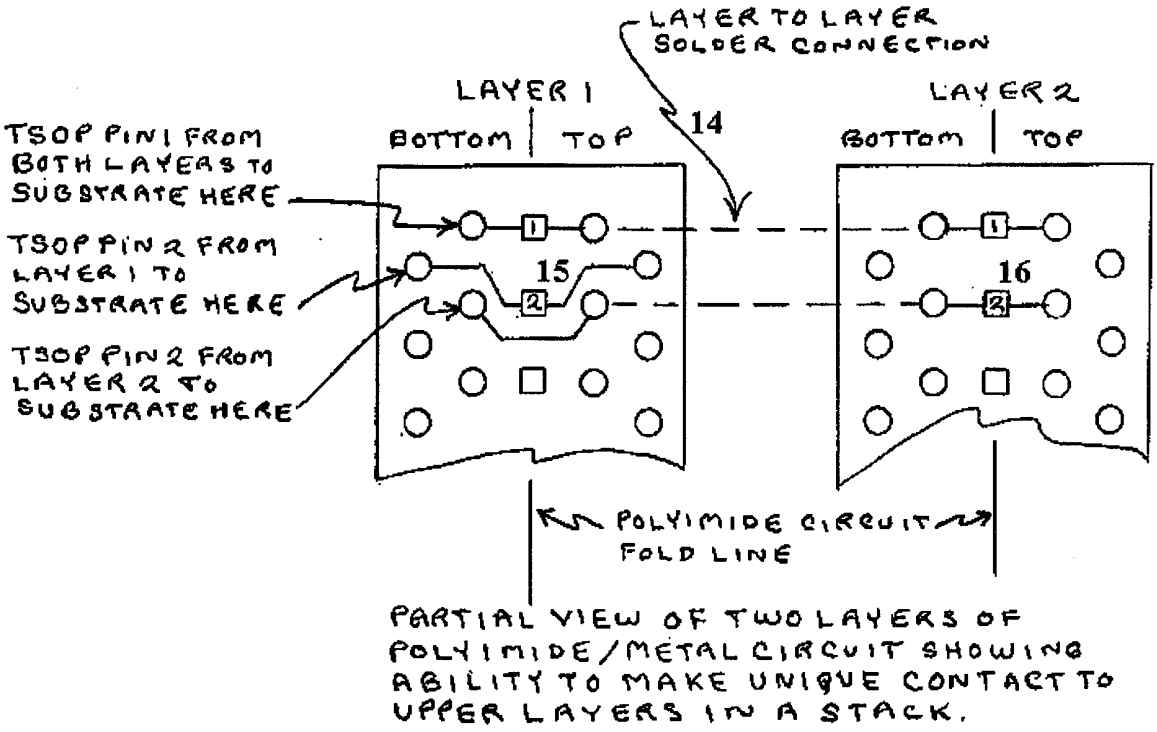
POLYIMIDE/METAL CIRCUITS ATTACHED TO T.S.O.P.

FIGURE 6



FOUR HIGH STACK OF T.S.O.P. ASSEMBLIES WITH B.G.A.'S SOLDER CONNECTED

FIGURE 7



PARTIAL VIEW OF TWO LAYERS OF POLYIMIDE/METAL CIRCUIT SHOWING ABILITY TO MAKE UNIQUE CONTACT TO UPPER LAYERS IN A STACK.

FIGURE 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/13171

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H05K 1/11; H01L 23/12
US CL :257/686, 777; 361/749, 803; 439/67
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/686, 777; 361/749, 776, 803; 439/67, 77

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,P	US 5,835,359 A (DiFRANCESCO) 10 NOVEMBER 1998 (10.11.98), Fig. 7D, col.13, line 18-col.14, line 3.	1,6
A,P	US 5,776,797 A (NICEWARNER, JR. et al.) 07 JULY 1998 (07.07.98), Fig. 7.	1,6
A	US 5,598,033 A (BEHLEN et al.) 28 JANUARY 1997 (28.01.97), Fig. 4.	1-12
A	US 5,394,303 A (YAMAJI) 28 FEBRUARY 1995 (28.02.95), Fig. 8.	1,6
A	US 3,492,538 A (FERGUSSON) 27 JANUARY 1970 (27.01.70), Figs. 1 and 2.	1,6
A	US 3,221,286 A (FEDDE) 30 NOVEMBER 1965 (30.11.65), Figs. 2 and 3.	1,6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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