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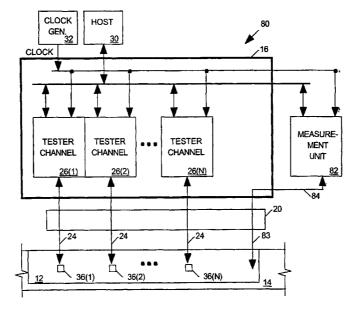
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(54) Title: SYSTEM FOR CALIBRATING TIMING OF AN INTEGRATED CIRCUIT WAFER TESTER



(57) Abstract: A timing calibration system for a wafer level integrated circuit (IC) tester is disclosed. To adjust a compare calibration delay of each tester channel, an interconnect system sequentially connects the tester channels to interconnect areas on a "calibration" wafer instead of to the IC on the wafer to be tested. Each interconnect area provides a path linking a channel to be calibrated to a spare channel. With the programmable drive delay of the channel being calibrated and the programmable compare and compare calibration delays of the spare channel set to standard values, the drive calibration delay of the channel being calibrated is adjusted so it sends a test signal edge to the spare channel close to when the spare channel samples it.



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Documentat	ion searched other than minimum documentation to the extent t	hat such documents are included	in the fields searched
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i	e actual completion of the international search 11 February 2002	Date of mailing of the in 19/02/2002	oternational search report
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