



(43) International Publication Date
8 September 2017 (08.09.2017)

- (51) International Patent Classification:
G06F 1/32 (2006.01) *G06F 1/26* (2006.01)
- (21) International Application Number:
PCT/US2017/016767
- (22) International Filing Date:
7 February 2017 (07.02.2017)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
15/060,326 3 March 2016 (03.03.2016) US
- (71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).
- (72) Inventors: **ARDANAZ, Federico**; 1293 NE Morning Sun Drive, Hillsboro, Oregon 97124 (US). **EASTEP, Jonathan**; 925 NW Hoyt Street, Apt. 435, Portland, Oregon 97209 (US). **GRECO, Richard**; 1360 SW Turner Road, West Linn, Oregon 97068 (US).
- (74) Agent: **JORDAN, B. Delano**; Jordan IP Law, LLC, c/o CPA Global, 900 Second Avenue South, Suite 600, Minneapolis, Minnesota 55402 (US).

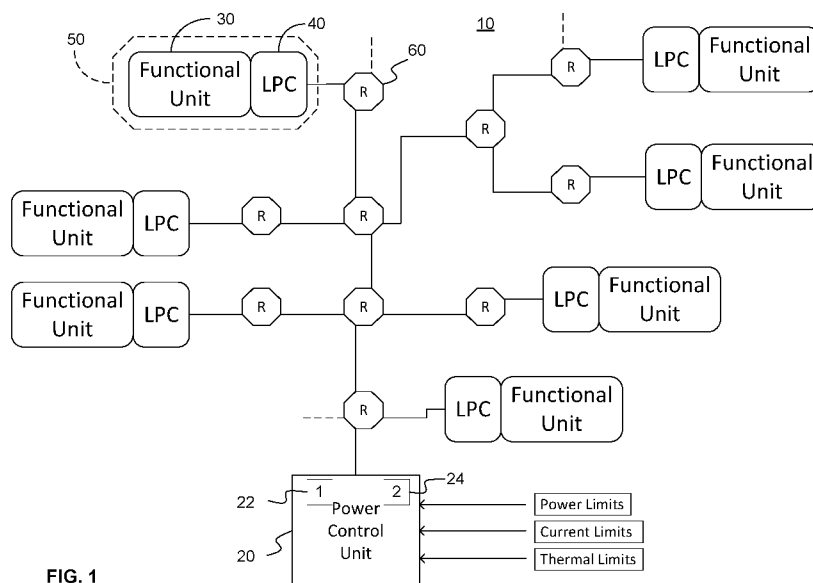
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- with amended claims (Art. 19(1))

(54) Title: HIERARCHICAL AUTONOMOUS CAPACITANCE MANAGEMENT



(57) Abstract: Apparatus and methods may provide for a central power control unit to grant a power allowance to each of a plurality of computer components and to allocate a shared power pool locally accessible to each of the plurality of computer components when one or more of the plurality of components needs to exceed its granted power allowance.

HIERARCHICAL AUTONOMOUS CAPACITANCE MANAGEMENT

CROSS-REFERENCE TO RELATED APPLICATIONS

5 The present application claims the benefit of priority to U.S. Non-Provisional Patent Application No. 15/060,326 filed on March 3, 2016.

GOVERNMENT INTEREST STATEMENT

10 This invention was made with Government support under contract number H98230-13-D-0124 awarded by the Department of Defense. The Government has certain rights in this invention.

TECHNICAL FIELD

15 Embodiments generally relate to power allocation in computer systems. More particularly, embodiments relate to power allocation using granted power levels and shared power pools.

BACKGROUND

20 The scale and performance of large computer systems may be limited by power constraints. For example, power delivery systems may have limits in the amount of current that they can supply. Dynamic Voltage-Frequency Scaling (DVFS) may be used to adjust hardware performance to varying levels of demand. When dynamically selecting voltage and frequency points, a design may require a guarantee that the power delivery current limit is not exceeded. Maximum current may depend
25 on the voltage-frequency decision and the dynamic capacitance (C_{dyn}) of the circuits/components. For circuits/components exhibiting a wide dynamic capacitance range, ensuring that no current violation occurs may limit the maximum operating frequency, which in turn may limit performance.

30 To maximize performance, different operation modes may be established for circuits/components such that different dynamic capacitance limits are enforced. Set dynamic capacitance levels may enable circuits/components to operate at higher frequencies than they would otherwise as long as the workload being performed does not exceed the set dynamic capacitance level. When a circuit/component needs to exceed its set dynamic capacitance level, the circuit/component may a) request a

higher set dynamic capacitance level and b) throttle its pipeline as needed to ensure that the dynamic capacitance level comports with the set level until a new, higher dynamic capacitance level is granted. Throttling the pipeline, however, may reduce both performance and energy efficiency.

5 Workload dynamic capacitance characteristics may vary rapidly for real workloads. In computers with large numbers of central processing units (CPUs) or with individual CPUs having multiple cores, it may be impractical for a central power control unit to reevaluate granted dynamic capacitance levels and make DVFS adjustments at the rate necessary to achieve high performance and efficiency. That is,
10 a centralized power control system may scale poorly with respect to the number of entities that it controls and the time scale of the workload phases to be managed.

BRIEF DESCRIPTION OF THE DRAWINGS

The various advantages of the embodiments will become apparent to one
15 skilled in the art by reading the following specification and appended claims, and by referencing the following drawings, in which:

FIG. 1 is an illustration of an example of power allocation according to an embodiment;

FIG. 2 is an illustration of an example of power allocation according to a
20 further embodiment;

FIG. 3 is an illustration of an example of an agent used in the power allocation of FIG. 2;

FIG. 4 is a graph of an example of granted and shared power by a central power control unit according to an embodiment; and

25 FIG. 5 is a flowchart of an example of a method of conducting power allocations according to an embodiment.

DESCRIPTION OF EMBODIMENTS

Turning now to the drawings in detail, FIG. 1 depicts a power allocation
30 system 10 that may grant power levels and/or dynamic capacitance (C_{dyn}) levels (e.g., power allowances). The power level/dynamic capacitance level is granted to each functional unit 30 (e.g., computer component) within the system 10. The functional units 30 may include system components such as, for example, a central processing

unit (CPU, e.g., host processor), a core of a central processing unit (for a CPU with multiple cores), a memory component, a network interface component, a chipset, a system circuit, or any other system element that draws current from a power supply. A central power control unit 20 may include a first portion 22 that grants the power level/dynamic capacitance level. A second portion 24 of the central power control unit 20 may allocate power to a shared power pool that may be accessed by the functional units 30 through local power control units (LPCs) 40, to be discussed in more detail below. The first portion 22 and the second portion 24 of the central power control unit 20 may be collocated within the central power control unit 20 and may represent different logical operations of the central power control unit 20 or they may be physically separate locations or components within the central power control unit 20. Each functional unit 30 and a local power control unit 40 may form an agent 50 within the illustrated system 10. The central power control unit 20, the functional unit 30, and the local power control unit 40 may be integrated as a system on a chip (SoC).

The system 10 may optionally form a part of a distributed computing system. The expression “distributed computing system” may relate to a system with interconnected processors that communicate and coordinate their actions in order to achieve a common goal. In one example, a distributed computing system may utilize component groups to handle work according to various computational topologies and architectures. For example, an application may be divided into various tasks that may be subdivided into groups of related subtasks (e.g., threads), which may be run in parallel on a computational resource. Related threads may be processed in parallel with one another on different components as “parallel threads,” and the completion of a given task may entail the completion of all of the related threads that form the task. Alternatively, parallel threads may be processed on different cores in the same CPU.

The shared power pool allocated by the second portion 24 of the central power control unit 20 may be quickly accessed by one or more functional units 30 when there is a need to exceed the granted power level/dynamic capacitance level more rapidly than a new grant request would take to process. In this manner, the functional units 30 may not need to throttle their respective dynamic capacitance levels while waiting for a grant of a new dynamic capacitance level by the central power control unit 20.

The illustrated system 10 has a topology in which the agents 50 are interconnected through routers 60 such that local power control units 40 may bidirectionally communicate with one another and with the central power control unit 20. The depicted topology is for illustration purposes only and any topology such as, for example, a ring, star, mesh, etc. or combination thereof.

The system 10 may be configured as a hierarchical virtual ring 100 as depicted in FIG. 2. The virtual ring 100 may include, for example, three rings 80 of four agents 50. In this embodiment, the allocated shared power pool is distributed in the form of power credits that may be distributed from the central power control unit 20 to the local power control units 40 of agents 50. The local power control unit 40 of each agent 50 may support a power credit input port 52 (Inp_{Even}) and a power credit output port 54 (Out_{Even}). Dynamic available power credits are received through input ports. An agent 50 may request additional power credits that will pass through the power credit input port 52 until the functional unit 30 of that agent no longer requires supplemental power. When received power credits are not needed by the agent 50, they may be forwarded to the next agent 50 in the ring. That is, a functional unit 30 may relinquish power credits when the granted power is sufficient to support its operations.

An exemplary power credit message may include: a source agent ID whose size is system dependent; a destination agent ID whose size is system dependent; a number of credits as an unsigned integer of at least one bit; a generation tag that is an unsigned integer of at least one bit; a minimum number of hops as an unsigned integer with a system dependent size; and a number of hops as an unsigned integer with a system dependent size.

Two input ports may be defined based on the message source-agent IDs: an even input port 52 and an odd input port 56 (Inp_{Odd}). Similarly, two output ports may be defined based on the message source-agent IDs: an even output port 54 and an odd output port 58 (Out_{Odd}). The illustrated local power control unit 40 of the agent 50 defines four control registers for power credit routing: InputEvenID, InputOddID, OutputEvenID, and OutputOddID. Unused power credits received through the even input port 52 may be forwarded through the odd output port 58. Conversely, unused power credits received through the odd input port 56 may be forwarded through the even output port 54.

Two types of agents 50 may be established based on the configuration of the agent input and output ports: cross agents and bypass agents. Cross agents populate all four routing control agents with valid agent IDs (e.g., all four types of input and output ports 52, 54, 56, and 58). Bypass agents may only configure one input port
5 (e.g., even input port 52) and its complementary output port (e.g., odd output port 58).

When an agent 50 no longer needs one or more previously absorbed power credits, it may inject the credit(s) back into the ring 80 using either the even or odd output port (54 and 58, respectively). The output port selected to inject the power credit may be based on a local power control unit control register that may be either
10 statically defined or dynamically adjusted by the central power control unit 20.

Turning to FIG. 3, an agent 50 is depicted in more detail. Each agent 50 may implement logic to self-regulate its power consumption while at the same time establishing whether to request a higher or lower power level/dynamic capacitance level from the central power control unit 20. The illustrated agent 50 includes a local
15 power control unit 40 and a functional unit 30 that includes at least a core logic component 105 and, optionally, throttler logic 110, and a power oracle 120. As described above, the functional unit 30 may be selected from a variety of computer components (including processor cores) and is the component for which power may be allocated by the central power control unit 20 (FIGs. 1 and 2). The throttler logic
20 110 may be configured to dynamically cap the activity of the core logic to avoid drawing more than the allowed amount of current. The power oracle 120 may use a throttling level indication to increase or decrease power allocation through power requests to the local power control unit 40.

A power delivery subsystem 130 may provide current consumption telemetry
25 which may require a power (watts) to current (amps) conversion in the local power control unit 40. If the power delivery subsystem 130 provides power consumption telemetry, then conversion between power and current may be bypassed. If the power delivery subsystem 130 provides neither power nor current telemetry, a digital estimation of current or power may be implemented based on core logic 105
30 telemetry.

The power oracle 120 may use a throttle level and current gap to determine power requirements for core logic component 105. If the throttle level is greater than or equal to the maximum throttle level, then a power request may be made for an amount of power equal to the current power plus a power delta where the power delta

is estimated based on the temporary current gap between the core logic component 105 demand and the current limit (as set by the central power control unit 20. When the core logic component 105 is consuming substantially less current than allocated by the central power control unit 20, power credits are released by the illustrated local
5 power control unit 40 back into a ring such as, for example, the ring 100 (FIG. 2). Power credits may be released according to the formula: if $(\text{current limit} - \text{current draw}) > \text{surplus threshold}$ then $\text{power request} = \text{current power} - \text{red coefficient} * \text{power delta}$ where the red coefficient is a tunable parameter used to adjust the aggressiveness of the release of power credits back into the ring.

10 The local power control unit 40 may include allowance exchange logic 140 that communicates with even input port 52 and a granted power allowance member 150 and pool allowance member 160. The granted allowance member 150 may store information related to the granted power allowance while the pool allowance member 160 may track power credit information. Members 150 and 160 communicate with a
15 converter 170 which in turn communicates with the throttle logic 110 to regulate power.

Turning to FIG. 4, the ratio between granted power to components and a shared power pool is depicted in graph 200. The amount of available power that is granted by the central power control unit to the components vs. the shared power pool
20 to be managed by the local power control units 40 may be a static design choice or adjusted dynamically by a central power control unit heuristic. In one aspect, an inversely proportional allocation may be used. For inversely proportional allocation, the shared power pool may be inversely proportional to a power limit applied with respect to a maximum power of the system. Using this heuristic, when little power is
25 available, the power is used almost entirely to guarantee a minimum level of performance of the system while leaving a small power pool to absorb small transient power demand spikes from the functional units 30 (FIGs. 1 and 3). Conversely, when more power head-room is available, more performance flexibility is injected into the system by having a larger fraction as a shared power pool.

30 In another aspect, incremental allocation may be used. With continuing reference to FIGs. 2 and 4, in a virtual ring routing configuration, a typical latency L for a power credit message to traverse the ring and be received back by the central power control unit 20 may be calculated. The central power control unit 20 may maintain a counter of injected power credits in the last L seconds (or equivalent

cycles) as an approximate number of free power credits (FC) in the system. When $FC < \text{Minimum Credits Threshold}$, then the central power control unit 20 will deallocate some of the granted power and inject additional power credits into the shared power pool. Conversely, when $FC > \text{Maximum Credits Threshold}$, the power control unit 20 will remove power credits from the shared power pool and allocate them to the granted power.

In another aspect dynamic changing shared power may be used. In a dynamic shared power scheme, an event may require changing the overall amount of power in the shared power pool. At an arbitrary point in time, power credits may be allocated at different agents 50 or be circulating across a ring.

FIG. 5 shows an overview of a method 500 of allocating power in a computer system. The method 500 may generally be implemented in an apparatus such as, for example, the central power control unit 20 (FIG. 1), already discussed. More particularly, the method 500 may be implemented in one or more modules as a set of logic instructions stored in a machine- or computer-readable storage medium such as random access memory (RAM), read only memory (ROM), programmable ROM (PROM), firmware, flash memory, etc., in configurable logic such as, for example, programmable logic arrays (PLAs), field programmable gate arrays (FPGAs), complex programmable logic devices (CPLDs), in fixed-functionality logic hardware using circuit technology such as, for example, application specific integrated circuit (ASIC), complementary metal oxide semiconductor (CMOS) or transistor-transistor logic (TTL) technology, or any combination thereof. For example, computer program code to carry out operations shown in method 500 may be written in any combination of one or more programming languages, including an object oriented programming language such as JAVA, SMALLTALK, C++ or the like and conventional procedural programming languages, such as the "C" programming language or similar programming languages.

With continuing reference to FIGs. 1, 2, and 5, illustrated processing block 510 provides for granting a power allowance to each of a plurality of computer components such as a functional unit 30. The grant may be of a power level or in the form of a dynamic capacitance level for the component.

Illustrated processing block 520 allocates a shared power pool that is part of the total power that may be allocated by the central power control unit 20. This shared power pool may allow local access by functional units 30 to power without the

need to request a new power level/dynamic capacitance level from the central power control unit 20.

5 Illustrated block 530 distributes power credits from the shared power pool when one or more components/functional units 30 needs to exceed its granted power allowance.

10 In an example of power credit distribution, the central power control unit 20 may maintain a valid “credit generation tag” unsigned integer. This value may be zero at rest and increments each time the shared power pool amount changes (with wrap around). Credits injected into the system 10 by the central power control unit 20 may be tagged with the current generation value. Central power control unit generation tag changes may be broadcasted to all local power control units 40. The local power control unit 40 may clear any allocated shared power when a new generation tag is received. Power credit messages received through the input ports may be dropped if their generation tag does not match the latest generation tag
15 broadcast by the central power control unit 20. Latency between generation tag wrapping around may be larger than the worst case latency for the system broadcasting a new generation tag to all the local power control units 40 plus any power credit messages in a ring moving from one agent 50 to the next.

20 When multiple agents 50 require additional power from the shared power pool, the determination of agents that receive power credits may depend on timing and ring routing. To increase fairness across agents on the usage of shared power, the central power control unit 20 may inject a credit message into the system with the “hops” field set to zero and the “minimum hops” field set to a random value between zero and N-1 where N is the number of agents 50 in the virtual ring. When an agent
25 50 receives a credit message, it may only absorb the credit message if the field “hops” is equal to or larger than the “minimum hops”. When a credit message is forwarded by an agent 50, the field “hops” is incremented. This mechanism may ensure that a randomized agent is the first agent to have the opportunity to absorb a power credit rather than a routing-dependent sequence of agents. When allocated credits are re-
30 injected into the ring by an agent, the field “hops” is cleared and “minimum hops” is set to zero.

In an alternative embodiment, agents may implement a periodic release of shared power pool power credits back into the ring. In such an example, a timer with a programmable delay may be armed when shared credits in an agent 50 is greater

than zero. At timer expiration, one credit may be injected back into the ring and the time rearmed. Use of a timer may guarantee some degree of recirculation of shared power from the shared power pool after it is initially allocated.

Additional Notes and Examples:

5 Example 1 may include a computer system comprising a plurality of computer components, a central power control unit to grant a power allowance to each of the plurality of computer components and to allocate a shared power pool locally accessible to each of the plurality of computer components when one or more of the plurality of components needs to exceed its granted power allowance, and one or
10 more local power control units in communication with each of the plurality of components to manage the shared power pool.

 Example 2 may include the computer system of example 1, wherein the one or more local power control units is configured to distribute power credits to the plurality of components from the shared power pool.

15 Example 3 may include the computer system of example 1, further comprising logic within each of the plurality of components to request a higher power allowance from the central power control unit for the component.

 Example 4 may include the computer system of example 3, wherein the request for a higher power allowance is in the form of a request for an increase in a
20 dynamic capacitance level of the component.

 Example 5 may include the computer system of example 1, further comprising a communication path among the one or more local power control units and the central power control unit to carry messages between the local power control units and the central power control unit and among the local power control units.

25 Example 6 may include a power control apparatus comprising a first power control portion to grant a power allowance to each of a plurality of computer components, and a second power control portion to allocate a shared power pool locally accessible to each of the plurality of computer components when one or more of the plurality of components needs to exceed its granted power allowance.

30 Example 7 may include the power control apparatus of example 6, wherein the shared power pool comprises power credits issued by the second power control portion to local power control units.

 Example 8 may include the power control apparatus of example 6, wherein the first power control portion is configured to change a dynamic capacitance of one

or more of the plurality of computer components in response to a request from one or more of the plurality of computer components.

Example 9 may include the power control apparatus of example 7, wherein the power control apparatus includes logic to inject additional power credits or remove power credits to balance component power requirements.

Example 10 may include a method to access power in a computer system comprising granting a power allowance to each of a plurality of computer components, allocating a shared power pool, and distributing power credits to one or more local power control units associated with one or more of the plurality of components when one or more of the components needs to exceed its granted power allowance.

Example 11 may include the method of example 10, wherein the one or more local power control units distributes received power credits to the one or more of the plurality of computer components.

Example 12 may include the method of example 10, further comprising requesting a higher power allowance from the central power control unit for the component.

Example 13 may include the method of example 12, wherein the requesting is in the form of requesting an increase in a dynamic capacitance level of the component.

Example 14 may include the method of example 10, further comprising communicating power credit messages between the one or more local power control units and the central power control unit.

Example 15 may include the method of example 10, further comprising communicating power credit messages among the local power control units.

Example 16 may include the method of example 10, further comprising injecting additional power credits or removing power credits to balance component power requirements.

Example 17 may include at least one computer readable storage medium comprising a set of instructions, wherein the instructions, when executed, cause a central power control unit to grant a power allowance to each of a plurality of computer components, allocate a shared power pool, and distribute power credits from the shared power pool to one or more local power control units associated with

one or more of the plurality of components when one or more of the components needs to exceed its granted power allowance.

Example 18 may include the at least one computer readable storage medium of example 17, wherein the power credits are distributed to one or more local power control units to be used by one or more computer components.

Example 19 may include the at least one computer readable storage medium of example 17, wherein the instructions, when executed, cause the central power control unit to inject additional power credits or remove power credits to balance component power requirements.

Example 20 may include the at least one computer readable storage medium of example 17, wherein the instructions, when executed, cause the central power control unit to communicate power credit messages to one or more local power control units.

Example 21 may include the at least one computer readable storage medium of example 17, wherein the instructions, when executed, cause the central power control unit to grant a higher power allowance to a computer component.

Example 22 may include the at least one computer readable storage medium of example 17, wherein the instructions, when executed, cause the central power control unit to grant a higher dynamic capacitance level to a computer component.

Example 23 may include a power control apparatus comprising means for granting a power allowance to each of a plurality of computer components, means for allocating a shared power pool, and means for distributing power credits from the shared power pool to one or more local power control units associated with one or more of the plurality of components when one or more of the components needs to exceed its granted power allowance.

Example 24 may include the power control apparatus of example 23, further comprising means to distribute the power credits to one or more local power control units to be used by one or more computer components.

Example 25 may include the power control apparatus of example 23, further comprising means to inject additional power credits or remove power credits to balance component power requirements.

Example 26 may include the power control apparatus of example 23, further comprising means to communicate power credit messages to the one or more local power control units.

Example 27 may include the power control apparatus of example 23, further comprising means to grant a higher power allowance to a computer component.

Example 28 may include the power control apparatus of example 23, further comprising means to grant a higher dynamic capacitance level to a computer
5 component.

The present embodiments may eliminate the situation in which agents must throttle their dynamic capacitance for the entire time that their dynamic capacitance would result in unsafe operation until the central power control unit responds granting a new power level/dynamic capacitance level. Using the present embodiments, agents
10 may avoid throttling as long as there is sufficient power in the pool of shared power. Overall, there may be a significant reduction in the time that dynamic capacitance throttling is used to limit current and significant increase in the time that DVFS mechanisms are used instead. Accordingly better performance and efficiency may be achieved. While the amount of shared power may be managed by a centralized entity
15 (the central power control unit), the allocation and de-allocation mechanism may be fully decentralized which avoids scalability problems associated with sole use of a central power control unit.

Embodiments are applicable for use with all types of semiconductor integrated circuit ("IC") chips. Examples of these IC chips include but are not limited to
20 processors, controllers, chipset components, programmable logic arrays (PLAs), memory chips, network chips, systems on chip (SoCs), SSD/NAND controller ASICs, and the like. In addition, in some of the drawings, signal conductor lines are represented with lines. Some may be different, to indicate more constituent signal paths, have a number label, to indicate a number of constituent signal paths, and/or
25 have arrows at one or more ends, to indicate primary information flow direction. This, however, should not be construed in a limiting manner. Rather, such added detail may be used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit. Any represented signal lines, whether or not having additional information, may actually comprise one or more signals that
30 may travel in multiple directions and may be implemented with any suitable type of signal scheme, e.g., digital or analog lines implemented with differential pairs, optical fiber lines, and/or single-ended lines.

Example sizes/models/values/ranges may have been given, although embodiments are not limited to the same. As manufacturing techniques (e.g.,

photolithography) mature over time, it is expected that devices of smaller size could be manufactured. In addition, well known power/ground connections to IC chips and other components may or may not be shown within the figures, for simplicity of illustration and discussion, and so as not to obscure certain aspects of the
5 embodiments. Further, arrangements may be shown in block diagram form in order to avoid obscuring embodiments, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the embodiment is to be implemented, i.e., such specifics should be well within purview of one skilled in the art. Where specific
10 details (e.g., circuits) are set forth in order to describe example embodiments, it should be apparent to one skilled in the art that embodiments can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

The terms “coupled” and “communicating” may be used herein to refer to any
15 type of relationship, direct or indirect, between the components in question, and may apply to electrical, mechanical, fluid, optical, electromagnetic, electromechanical or other connections. In addition, the terms “first”, “second”, etc. may be used herein only to facilitate discussion, and carry no particular temporal or chronological significance unless otherwise indicated.

Those skilled in the art will appreciate from the foregoing description that the
20 broad techniques of the embodiments can be implemented in a variety of forms. Therefore, while the embodiments have been described in connection with particular examples thereof, the true scope of the embodiments should not be so limited since other modifications will become apparent to the skilled practitioner upon a study of
25 the drawings, specification, and following claims.

CLAIMS

We claim:

- 5 1. A computer system comprising:
 a plurality of computer components;
 a central power control unit to grant a power allowance to each of the plurality
 of computer components and to allocate a shared power pool locally accessible to
 each of the plurality of computer components when one or more of the plurality of
10 components needs to exceed its granted power allowance; and
 one or more local power control units in communication with each of the
 plurality of components to manage the shared power pool.
2. The computer system of claim 1, wherein the one or more local power
15 control units is configured to distribute power credits to the plurality of components
 from the shared power pool.
3. The computer system of claim 1 or 2, further comprising logic within
 each of the plurality of components to request a higher power allowance from the
20 central power control unit for the component.
4. The computer system of claim 3, wherein the request for a higher
 power allowance is in the form of a request for an increase in a dynamic capacitance
 level of the component.
- 25 5. The computer system of claim 1 or 2, further comprising a
 communication path among the one or more local power control units and the central
 power control unit to carry messages between the local power control units and the
 central power control unit and among the local power control units.

30

6. A power control apparatus comprising:
a first power control portion to grant a power allowance to each of a plurality
of computer components; and

a second power control portion to allocate a shared power pool locally
5 accessible to each of the plurality of computer components when one or more of the
plurality of components needs to exceed its granted power allowance.

7. The power control apparatus of claim 6, wherein the shared power pool
comprises power credits issued by the second power control portion to local power
10 control units.

8. The power control apparatus of claim 6 or 7, wherein the first power
control portion is configured to change a dynamic capacitance of one or more of the
plurality of components in response to a request from one or more of the plurality of
15 components.

9. The power control apparatus of claim 7, wherein the power control
apparatus includes logic to inject additional power credits or remove power credits to
balance component power requirements.

20

10. A method to access power in a computer system comprising:
granting a power allowance to each of a plurality of computer components;
allocating a shared power pool; and
distributing power credits from the shared power pool to one or more local
25 power control units associated with one or more of the plurality of components when
one or more of the components needs to exceed its granted power allowance.

11. The method of claim 10, wherein the one or more local power control
units distributes received power credits to the one or more of the plurality of
30 components.

12. The method of claim 10 or 11, further comprising requesting a higher power allowance from the central power control unit for the component.

13. The method of claim 12, wherein the requesting is in the form of
5 requesting an increase in the dynamic capacitance level of the component.

14. The method of claim 10 or 11, further comprising communicating power credit messages between the one or more local power control units and the central power control unit.

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15. The method of claim 10 or 11, further comprising communicating power credit messages among the local power control units.

16. The method of claim 10 or 11, further comprising injecting additional
15 power credits or removing power credits to balance component power requirements.

17. At least one computer readable storage medium comprising a set of instructions, wherein the instructions, when executed, cause a central power control unit to:

20

grant a power allowance to each of a plurality of computer components;

allocate a shared power pool; and

distribute power credits from the shared power pool to one or more local power control units associated with one or more of the plurality of components when one or more of the components needs to exceed its granted power allowance.

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18. The at least one computer readable storage medium of claim 17, wherein the power credits are distributed to one or more local power control units to be used by one or more computer components.

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19. The at least one computer readable storage medium of claim 17 or 18, wherein the instructions, when executed, cause the central power control unit to inject additional power credits or remove power credits to balance component power requirements.

20. The at least one computer readable storage medium of claim 17 or 18, wherein the instructions, when executed, cause the central power control unit to communicate power credit messages to one or more local power control units.

5 21. The at least one computer readable storage medium of claim 17 or 18, wherein the instructions, when executed, cause the central power control unit to grant a higher power allowance to a computer component.

22. The at least one computer readable storage medium of claim 17 or 18,
10 wherein the instructions, when executed, cause the central power control unit to grant a higher dynamic capacitance level to a computer component.

23. A power control apparatus comprising:
means for granting a power allowance to each of a plurality of computer
15 components;
means for allocating a shared power pool; and
means for distributing power credits from the shared power pool to one or
more local power control units associated with one or more of the plurality of
components when one or more of the components needs to exceed its granted power
20 allowance.

24. The power control apparatus of claim 23, further comprising means to
distribute the power credits to one or more local power control units to be used by one
or more computer components.

25 25. The power control apparatus of claim 23 or 24, further comprising
means to inject additional power credits or remove power credits to balance
component power requirements.

AMENDED CLAIMS

received by the International Bureau on 21 jul 2107 (21.07.2017)

We claim:

- 5 1. A computer system comprising:
 a plurality of computer components;
 a central power control unit to grant a power allowance to each of the plurality
 of computer components and to allocate a shared power pool locally accessible to
 each of the plurality of computer components when one or more of the plurality of
10 components needs to exceed its granted power allowance; and
 one or more local power control units in communication with each of the
 plurality of components to manage the shared power pool.
2. The computer system of claim 1, wherein the one or more local power
15 control units is configured to distribute power credits to the plurality of components
 from the shared power pool.
3. The computer system of claim 1 or 2, further comprising logic within
 each of the plurality of components to request a higher power allowance from the
20 central power control unit for the component.
4. The computer system of claim 3, wherein the request for a higher
 power allowance is in the form of a request for an increase in a dynamic capacitance
 level of the component.
- 25 5. The computer system of claim 1 or 2, further comprising a
 communication path among the one or more local power control units and the central
 power control unit to carry messages between the local power control units and the
 central power control unit and among the local power control units.

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6. A power control apparatus comprising:

a first power control portion to grant a power allowance to each of a plurality of computer components; and

5 a second power control portion to allocate a shared power pool locally accessible to each of the plurality of computer components when one or more of the plurality of components needs to exceed its granted power allowance.

7. The power control apparatus of claim 6, wherein the shared power pool comprises power credits issued by the second power control portion to local power
10 control units.

8. The power control apparatus of claim 6 or 7, wherein the first power control portion is configured to change a dynamic capacitance of one or more of the plurality of components in response to a request from one or more of the plurality of
15 components.

9. The power control apparatus of claim 7, wherein the power control apparatus includes logic to inject additional power credits or remove power credits to balance component power requirements.

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10. A method to access power in a computer system comprising:

granting a power allowance to each of a plurality of computer components;

allocating a shared power pool; and

25 distributing power credits from the shared power pool to one or more local power control units associated with one or more of the plurality of components when one or more of the components needs to exceed its granted power allowance.

11. The method of claim 10, wherein the one or more local power control units distributes received power credits to the one or more of the plurality of
30 components.

12. The method of claim 10 or 11, further comprising requesting a higher power allowance from a central power control unit for the component.

13. The method of claim 12, wherein the requesting is in the form of requesting an increase in a dynamic capacitance level of the component.

14. The method of claim 10 or 11, further comprising communicating power credit messages between the one or more local power control units and a central power control unit.

15. The method of claim 10 or 11, further comprising communicating power credit messages among the local power control units.

16. The method of claim 10 or 11, further comprising injecting additional power credits or removing power credits to balance component power requirements.

17. At least one computer readable storage medium comprising a set of instructions, wherein the instructions, when executed, cause a central power control unit to:

grant a power allowance to each of a plurality of computer components;
allocate a shared power pool; and

distribute power credits from the shared power pool to one or more local power control units associated with one or more of the plurality of components when one or more of the components needs to exceed its granted power allowance.

18. The at least one computer readable storage medium of claim 17, wherein the power credits are distributed to one or more local power control units to be used by one or more computer components.

19. The at least one computer readable storage medium of claim 17 or 18, wherein the instructions, when executed, cause the central power control unit to inject additional power credits or remove power credits to balance component power requirements.

20. The at least one computer readable storage medium of claim 17 or 18, wherein the instructions, when executed, cause the central power control unit to communicate power credit messages to one or more local power control units.

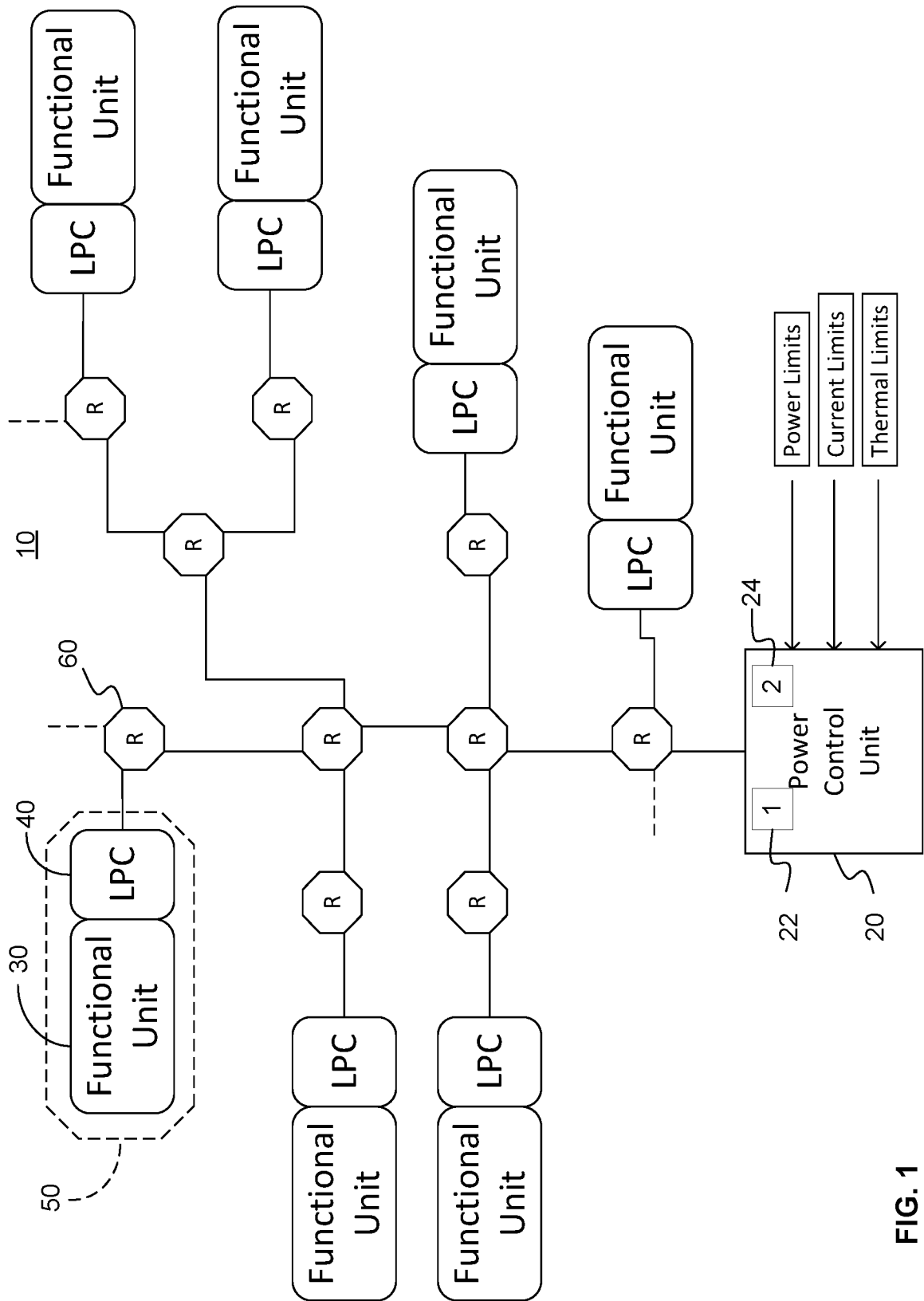
5 21. The at least one computer readable storage medium of claim 17 or 18, wherein the instructions, when executed, cause the central power control unit to grant a higher power allowance to a computer component.

10 22. The at least one computer readable storage medium of claim 17 or 18, wherein the instructions, when executed, cause the central power control unit to grant a higher dynamic capacitance level to a computer component.

23. A power control apparatus comprising:
means for granting a power allowance to each of a plurality of computer
15 components;
means for allocating a shared power pool; and
means for distributing power credits from the shared power pool to one or more local power control units associated with one or more of the plurality of components when one or more of the components needs to exceed its granted power
20 allowance.

24. The power control apparatus of claim 23, further comprising means to distribute the power credits to one or more local power control units to be used by one or more computer components.

25 25. The power control apparatus of claim 23 or 24, further comprising means to inject additional power credits or remove power credits to balance component power requirements.



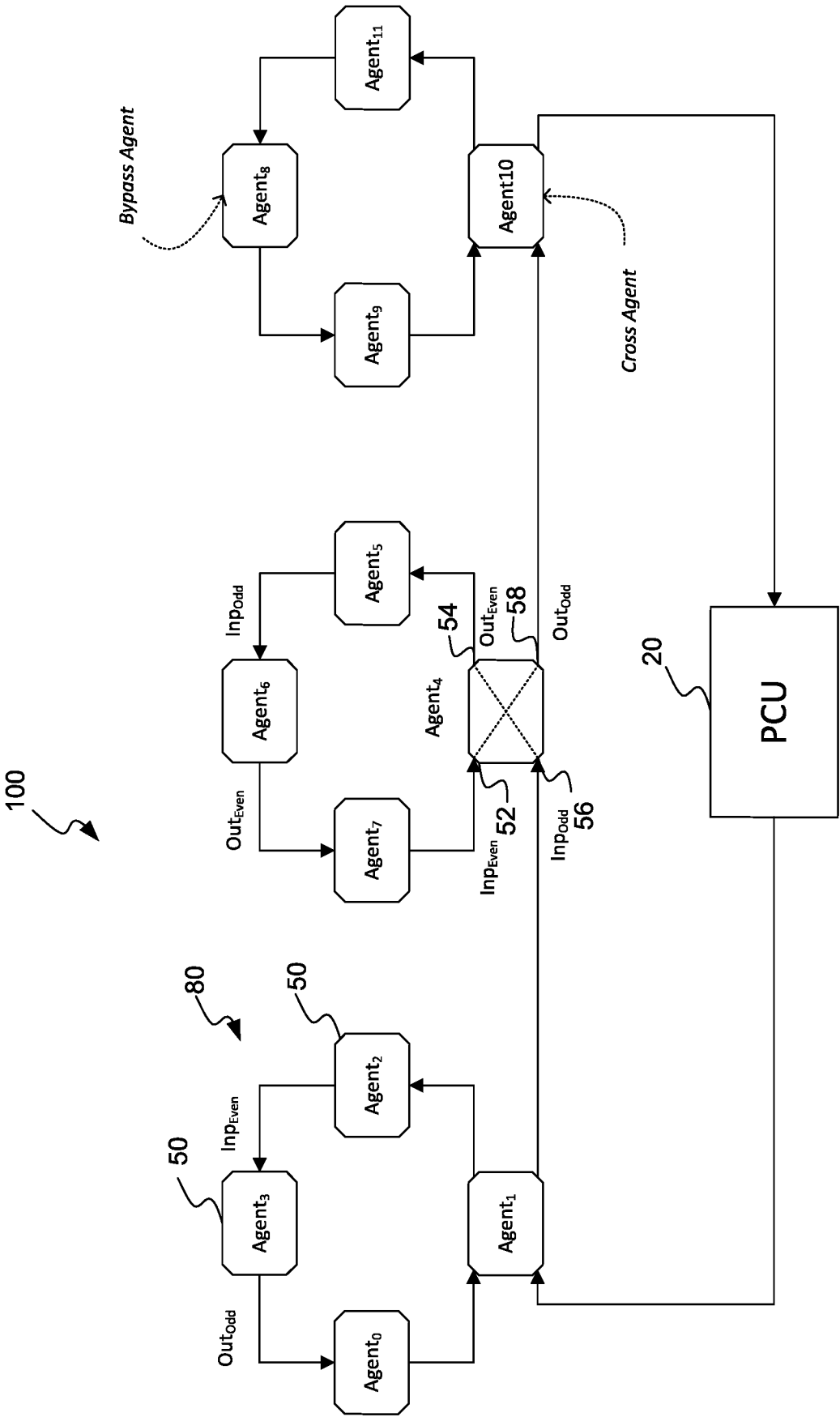


FIG. 2

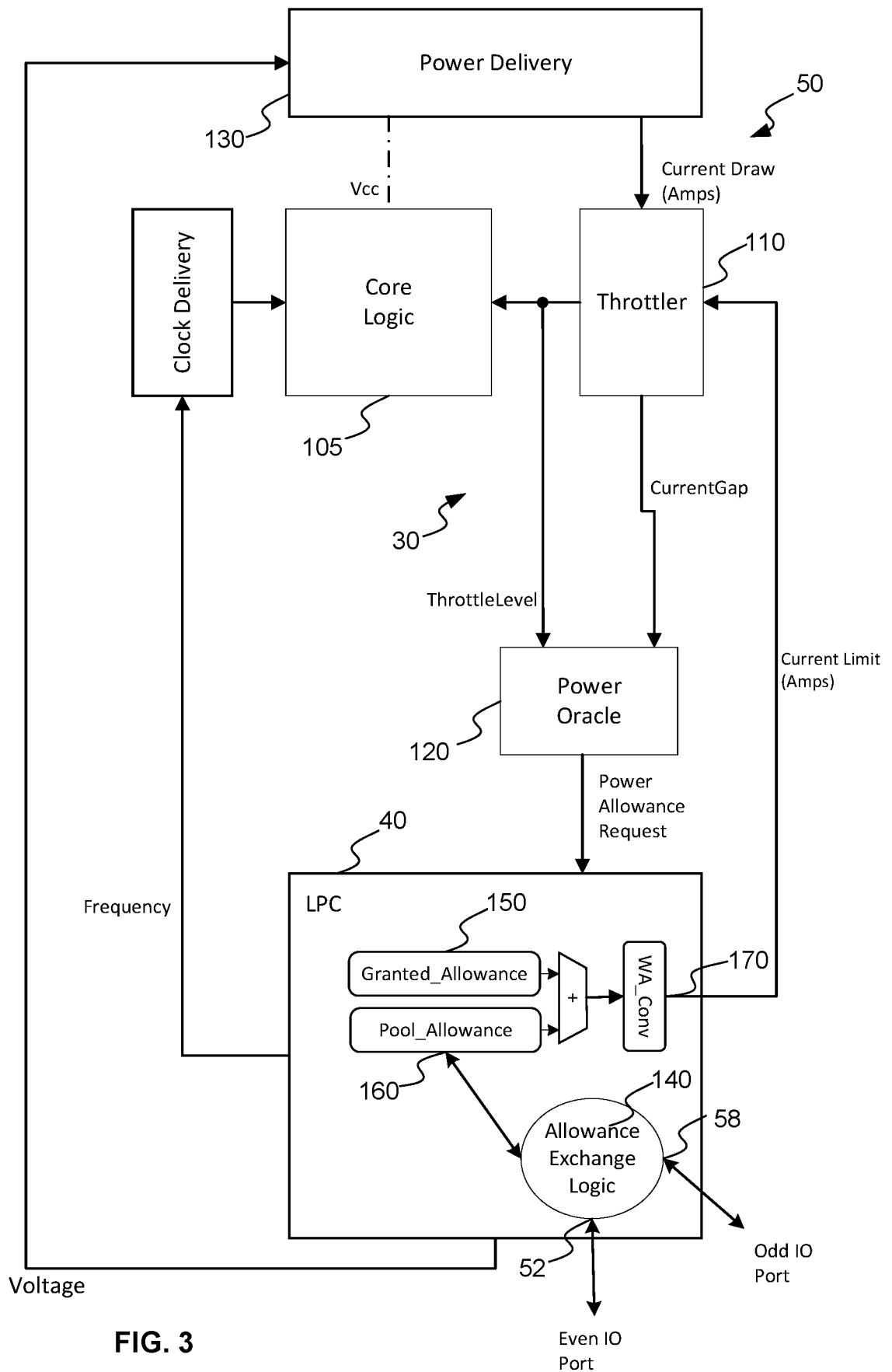
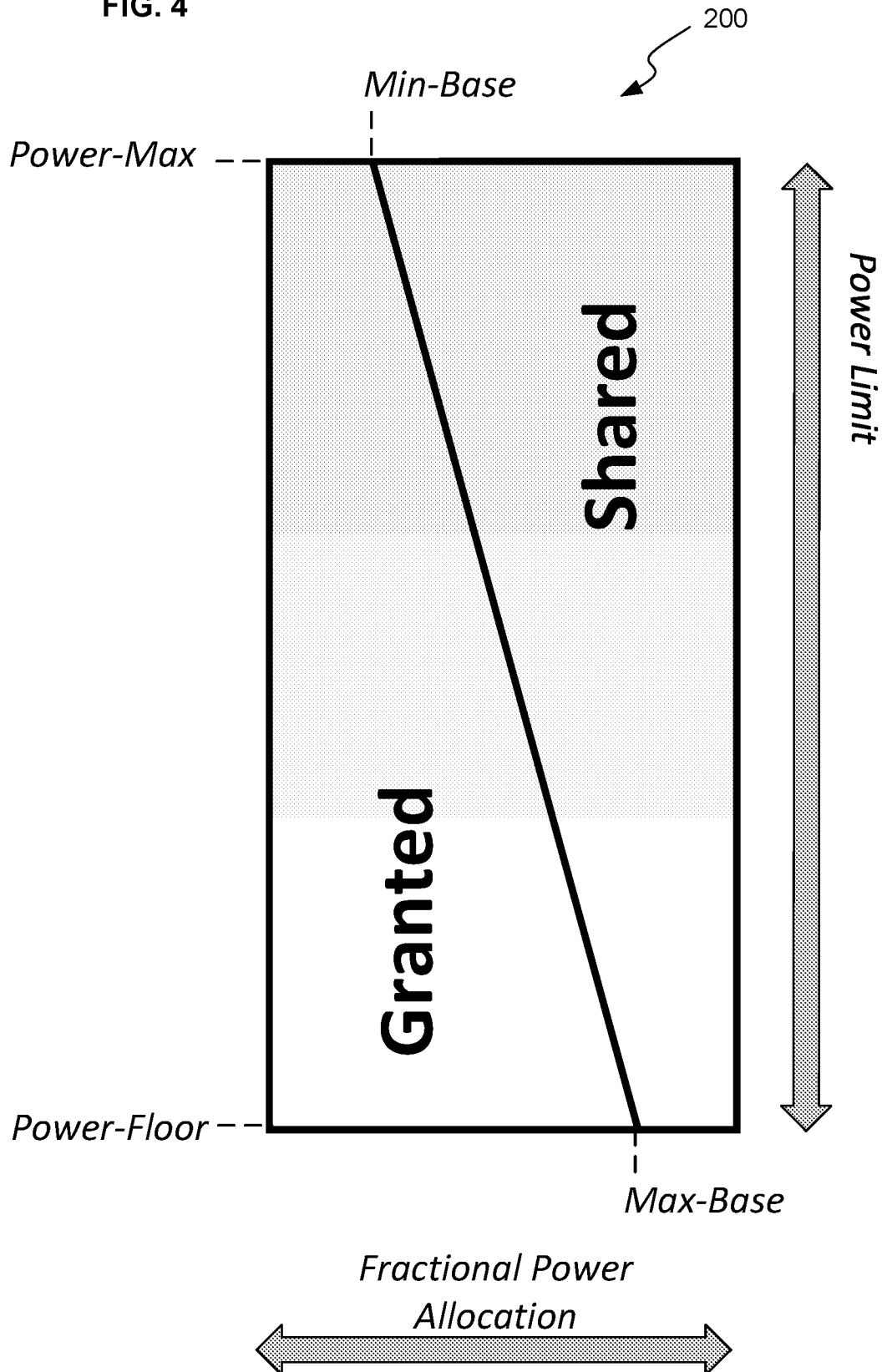


FIG. 3

FIG. 4



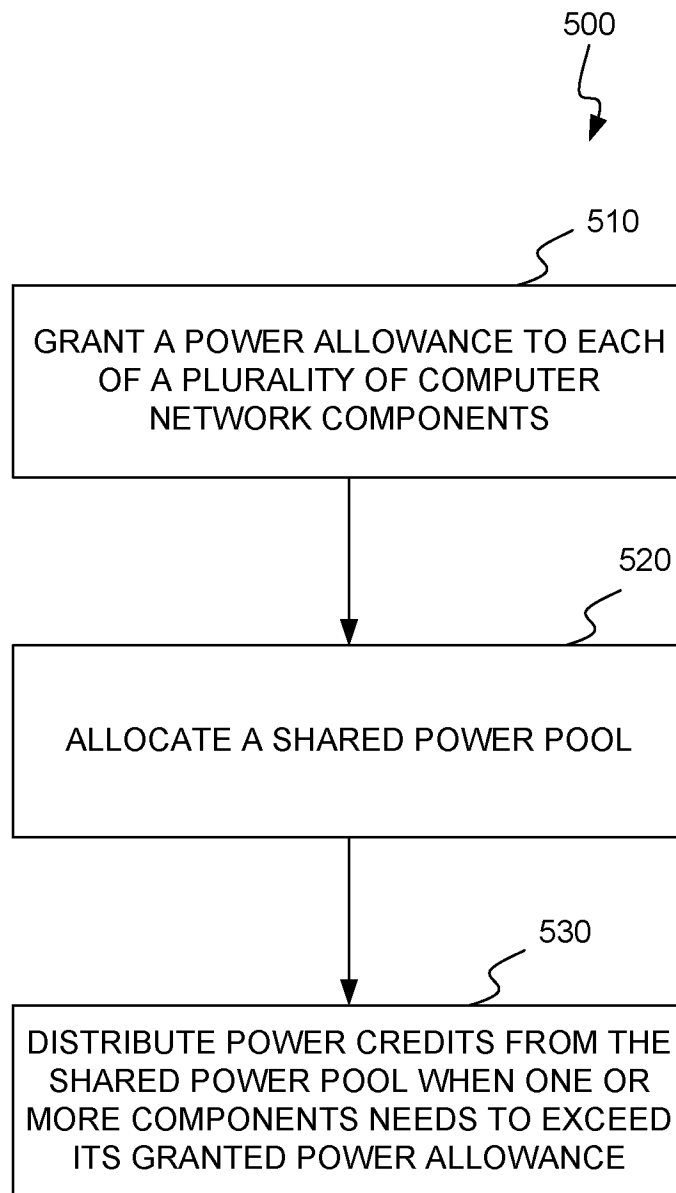


FIG. 5

A. CLASSIFICATION OF SUBJECT MATTER**G06F 1/32(2006.01)i, G06F 1/26(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/32; G06F 11/30; G06F 1/26; G06F 1/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: power unit, processor, interface, additional power, power distribution

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011-0029787 A1 (BRIAN A. DAY et al.) 03 February 2011	6
Y	See paragraphs [0002]-[0016]; claims 1, 7; and figure 1.	1-5, 7-25
Y	US 2012-0023345 A1 (SAMUEL D. NAFFZIGER et al.) 26 January 2012	1-5, 7-25
	See paragraphs [0021]-[0024]; claims 1, 4; and figure 1.	
A	US 2011-0010566 A1 (JUSTIN P. BANDHOLZ et al.) 13 January 2011	1-25
	See paragraphs [0015]-[0024]; claim 1; and figure 1.	
A	US 2010-0211807 A1 (SHUNSUKE AKIMOTO) 19 August 2010	1-25
	See paragraphs [0033]-[0039]; and figure 1.	
A	KR 10-2010-0111254 A (INTEL CORP.) 14 October 2010	1-25
	See paragraphs [0005]-[0007]; claim 1; and figure 1.	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 May 2017 (22.05.2017)

Date of mailing of the international search report

23 May 2017 (23.05.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

LEE, Dong Yun

Telephone No. +82-42-481-8734



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/016767

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011-0029787 A1	03/02/2011	CN 101986241 A	16/03/2011
		CN 101986241 B	03/02/2016
		EP 2284650 A2	16/02/2011
		EP 2284650 A3	13/08/2014
		JP 2011-028720 A	10/02/2011
		JP 2014-067440 A	17/04/2014
		JP 5506459 B2	28/05/2014
		JP 5727582 B2	03/06/2015
		KR 10-1443418 B1	24/09/2014
		KR 10-2011-0011501 A	08/02/2011
		TW 201104400 A	01/02/2011
		TW I497270 B	21/08/2015
		US 8239701 B2	07/08/2012
US 2012-0023345 A1	26/01/2012	CN 103069359 A	24/04/2013
		CN 103069359 B	19/10/2016
		EP 2596413 A1	29/05/2013
		EP 2596413 B1	14/12/2016
		JP 2013-539571A	24/10/2013
		JP 5689965 B2	25/03/2015
		KR 10-1468368 B1	02/12/2014
		KR 10-2013-0092566 A	20/08/2013
		US 8510582 B2	13/08/2013
		WO 2012-012256 A1	26/01/2012
US 2011-0010566 A1	13/01/2011	KR 10-2011-0004328 A	13/01/2011
US 2010-0211807 A1	19/08/2010	JP 2010-191595 A	02/09/2010
		JP 4743293 B2	10/08/2011
		US 8219839 B2	10/07/2012
KR 10-2010-0111254 A	14/10/2010	CN 101872996 A	27/10/2010
		GB 2469380 A	13/10/2010
		JP 2010-259320 A	11/11/2010
		JP 5285015 B2	11/09/2013
		US 2010-0257529 A1	07/10/2010