(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 August 2004 (26.08.2004)

PCT

(10) International Publication Number
WO 2004/073044 A2

(51) International Patent Classification[7]: H01L

(21) International Application Number:
PCT/US2004/004254

(22) International Filing Date: 13 February 2004 (13.02.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/447,191 13 February 2003 (13.02.2003) US

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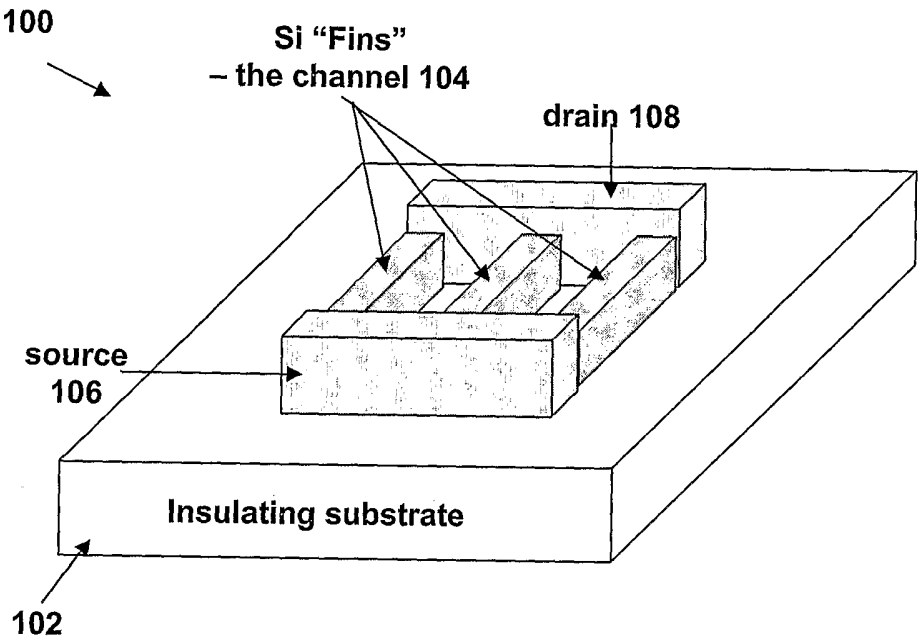
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: INTEGRATED SEMICONDUCTOR DEVICE AND METHOD TO MAKE SAME



(57) Abstract: A multiple-gate FET structure includes a semiconductor substrate. A gate region is formed on the semiconductor substrate. The gate region comprises a gate portion and a channel portion. The gate portion has at least two opposite vertical surfaces adjacent to the channel portion. A source region abuts the gate region at one end, and a drain diffusion region abuts the gate region at the other end.

WO 2004/073044 A2

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTEGRATED SEMICONDUCTOR DEVICE AND METHOD TO MAKE SAME

PRIORITY INFORMATION

This application claims priority from provisional application Ser. No. 60/447,191 filed February 13, 2003, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

The invention relates to the field of multiple-gate field effect transistor (FET) and method to fabricate the same, and in particular to fabricating strained-Si multiple-gate FET structures.

One of the primary challenges of very large scale integration (VLSI) has been the integration of an ever-increasing number of MOSFET devices within a single chip. This was achieved mainly in the prior art by scaling down the MOSFET device feature size without excessive short-channel effects. When the device becomes smaller and smaller, short-channel effects, which are caused by the two-dimensional electrostatic charge sharing between the gate and the source/drain diffusion regions, become a serious issue.

To scale down a MOSFET feature size without excessive short-channel effects, multiple-gate MOSFET structures have been developed. Yan, et al., "Scaling the Si MOSFET: From bulk to SOI to bulk", IEEE Trans. Elect. Dev., Vol. 39, p. 1704, July 1992, have shown that to reduce short-channel effects for 0.05 μm MOSFETs, it is important to have a backside-conducting layer present in the structure that screens the drain field away from the channel. The Yan, et al. results show that double-gated MOSFETs, or MOSFETs with a top gate and a backside ground plane, or in general multiple-gate device, are more immune to short-channel effects and hence can be scaled to shorter dimensions than conventional single-gated MOSFETs.

In all the multiple-gate MOSFETs, there are at least two gates which are opposite to each other, one on each side of the channel. The two gates are electrically connected so that they serve to modulate the channel. Short-channel effects are greatly suppressed in such a structure because the two gates very effectively terminate the drain field line preventing the drain potential from being felt at the source end of the channel. Consequently, the two-dimensional electrostatic charge sharing between

the gate and the source/drain diffusion regions in a multiple-gate MOSFET is much smaller than that of a conventional single-gated structure of the same channel length.

Moreover, multiple-gate MOSFET can provide significant performance advantages over the single gate devices. Various multiple-gate processes have been proposed. One promising approach is the FinFET technology, where silicon "fins" are defined on an insulator substrate, and two gates are made on the both sidewall of the fin. High performance FinFET CMOS has been designed using the state of art industry settings (See Y-K Choi, et al " Nanoscale CMOS spacer FinFET for the Terabit era," *IEEE, Electron Device Letters*, Vol. 23, No. 1, pp 23-27, 2002).

Another multiple-gate technology is formed using the Tri-Gate CMOS technology, which utilizes the additional top surface besides the two sidewalls (See B. Doyle, et al. "Tri-Gate fully-depleted CMOS transistors: fabrication, design, and layout," *IEEE VLSI Symposium, 2003).* Other multiple-gate technology includes Ω-gate technology, gate-all-around technology, etc.

To implement the multiple-gate technology, conventional thin film SOI wafers are used. Since the multiple-gate devices have very small channel dimension, typically less than 100nm, thus the non-uniformity of the Si film thickness across a SOI wafer will affect the device performance significantly. Thus, the multiple-gate technology requires very good film thickness uniformity. However, the conventional methods for SOI substrate production typically involve costly processes such as high dose ion implantation or wafer bonding. In addition, the SOI substrate produced by conventional methods has limitations in film thickness range and thickness uniformity. There is also no well-established method to produce strained-Si multiple-gate device in the prior art. A strained-Si multiple-gate device is able to combine the benefits of multiple-gate technology and high electron and hole mobility. Strained-Si is shown to enhance electron and hole mobility significantly.

SUMMARY OF THE INVENTION

According to one aspect of the invention, there is provided a multiple-gate FET structure. The multiple-gate FET structure includes a semiconductor substrate. A gate region is formed on the semiconductor substrate. The gate region comprises a gate portion and a channel portion. The gate portion has at least two opposite vertical surfaces adjacent to the channel portion. A source region abuts the gate region at one end, and a drain diffusion region abuts the gate region at the other end.

According to another aspect of the invention, there is provided a multiple-gate FET structure. The multiple-gate FET structure includes a semiconductor substrate. A gate region is formed on the semiconductor substrate. The gate region comprises a gate portion and a channel portion. The gate portion has at two opposite vertical surfaces and one horizontal top surface adjacent to the channel portion. A source region abuts the gate region at one end, and a drain diffusion region abuts the gate region at the other end.

According to another aspect of the invention, there is provided a method of forming a multiple-gate FET structure. The method includes providing a semiconductor substrate, and forming a gate region on the semiconductor substrate. The gate region comprises a gate portion and a channel portion. The gate portion has at least two opposite vertical surfaces adjacent to the channel portion. Furthermore, the method includes forming a source region that abuts the gate region at one end and forming a drain diffusion region abuts the gate region at the other end.

According to another aspect of the invention, there is provided a method of forming a multiple-gate FET structure. The method includes providing a semiconductor substrate, and forming a gate region on the semiconductor substrate. The gate region comprises a gate portion and a channel portion. The gate portion has at two opposite vertical surfaces and one horizontal top surface adjacent to the channel portion. Furthermore, the method includes forming a source region that abuts the gate region at one end and forming a drain diffusion region abuts the gate region at the other end.

According to another aspect of the invention, there is provided a digitalized semiconductor structure that includes a semiconductor substrate. A plurality of fin-shaped strips are formed on the semiconductor substrate. The fin-shaped strips have identical widths and identical heights and are distributed evenly throughout the entire structure, with a feature pitch between one another.

According to another aspect of the invention, there is provided a method of forming a digitalized semiconductor structure that includes a semiconductor substrate. The method includes forming a plurality of fin-shaped strips on the semiconductor substrate. The fin-shaped strips have identical widths and identical heights and are distributed evenly throughout the entire structure, with a feature pitch between one another.

According to another aspect of the invention, there is provided a method of

forming a digitalized semiconductor structure that includes a semiconductor substrate. The method includes forming a first semiconductor layer on the substrate. A second semiconductor layer is formed on the first layer, and the second semiconductor layer is different from the first semiconductor layer. Also, the method includes patterning the second semiconductor layer into a plurality of fin-shaped strips. The fin-shaped strips have identical heights, identical widths, and being distributed evenly throughout the entire substrate, with a feature pitch d between one another. Furthermore, the method includes converting the first semiconductor layer into a buried oxide layer.

According to another aspect of the invention, there is provided a method of forming a digitalized semiconductor structure that includes a semiconductor substrate. The method includes forming a first semiconductor layer on the substrate. The first semiconductor layer is converted into a first porous semiconductor layer. The method includes forming a second semiconductor layer on the first porous semiconductor layer. The second semiconductor layer is patterned into a plurality of fin-shaped strips. The fin-shaped strips having identical heights, identical widths, and being distributed evenly throughout the entire substrate, with a feature pitch d between one another. Furthermore, the method includes converting the first porous semiconductor layer into a buried oxide layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1A-1B are schematic diagrams illustrating the concept of the digitalized semiconductor-on-insulator substrate;

FIGs. 2A-2C are schematic diagrams illustrating a conventional SOI substrate and the IC fabrication process on the conventional SOI substrate;

FIGs. 3A-3C are schematic diagrams demonstrating the IC fabrication process on a digitalized semiconductor-on-insulator substrate;

FIGs. 4A-4B are schematic diagrams illustrating a technique used to make a source or drain of a FinFET structure using a digitalized semiconductor-on-insulator substrate;

FIGs. 5A-5C are schematic diagrams illustrating a technique to produce digitalized semiconductor-on-insulator substrates in accordance with the invention;

FIGs. 6A-6B are schematic diagrams illustrating another technique to produce digitalized semiconductor-on-insulator substrates in accordance with the invention;

FIGs. 7A-7E are schematic diagrams illustrating the formation of various

digitalized strained-Si fin structures;

FIGs. 8A-8F are schematic diagrams illustrating a conventional Si multiple-gate FET transistor;

FIGs. 9A-9C are schematic diagrams illustrating a multiple-gate FET device fabricated directly on a bulk semiconductor substrate having; and

FIGs. 10A-10C are schematic diagrams illustrating three different fin-shaped channel region structures used to form strained-material multiple-gate devices.

DETAILED DESCRIPTION OF THE INVENTION

The invention provides a digitalized semiconductor-on-insulator substrate. The advantage of such a digitalized semiconductor-on-insulator substrate is two-fold: (1) low wafer cost due to the starting substrate for the digitalized semiconductor-on-insulator substrate fabrication is bulk substrate instead of insulating substrate, and (2) uniform fin-shaped strips across the entire wafer, as it is defined by, for example, an epitaxial step and an etch process on a bulk Si wafer which forms the "fins", instead of by the SOI film. The digitalized semiconductor-on-insulator substrate can be used as a general substrate for any multiple-gate CMOS IC design. It is analogous to conventional silicon substrates, which can be used for any CMOS IC application.

FIGs. 1A-1B show the concept of a digitalized semiconductor-on-insulator substrate 2. In particular, FIG. 1A illustrates a top view of the substrate 2, and FIG. 1B is a cross-sectional view of the substrate 2. In the digitalized semiconductor-on-insulator substrate 2, isolated semiconductor structures 4 (or lines) are provided on the insulating substrate 6. The lines 4 are distributed evenly throughout the wafer, as shown in FIG. 1A and FIG. 1B. A typical value of pitch d ranges from 10 nm to 500nm. In other embodiments, the semiconductor lines 4 are not limited to Si, they may comprise relaxed-SiGe, relaxed-Ge, strained-Si, strained-SiGe, strained-Ge, SiC, GaN, GaAs or other III-V materials.

In alternative embodiments, the insulating substrate 6 can include any one of the following: a SOI material, a SSOI (strained-Si on insulator) material, a SGOI (SiGe on insulator) material, a strained-SGOI (strained-SiGe on insulator) material, a GOI (Ge on insulator) material, a strained-GOI (strained-Ge on insulator) material.

In comparison, FIGs. 2A-2C show a conventional SOI substrate 8 and the IC fabrication process on the conventional SOI substrate 8 in the prior art. FIG. 2A shows the conventional SOI substrate 8 having a continuous semiconductor layer 10

on an insulating substrate 12. In the conventional SOI IC fabrication process, customized IC layout design 14 is performed, as shown in FIG. 2B. The SOI substrate 8 is then patterned into desired semiconductor islands 16 according to the IC layout design 14, as shown in FIG. 2C. Those islands 16 may not necessarily have even dimensions and are typically not evenly distributed across the wafer. On those islands 16, conventional SOI devices are fabricated.

In contrast, FIGs. 3A-3C show the multiple-gate IC fabrication process on a digitalized semiconductor-on-insulator substrate 18, in accordance with the invention. In the digitalized semiconductor-on-insulator substrate 18, the semiconductor lines 20 are defined before the start of the IC layout design and semiconductor device fabrication. The substrate 18 has a feature line pitch value d, as shown in FIG. 3A. Then the customized multiple-gate (FinFET or Tri-gate) IC layout design 22 is performed, as shown in FIG. 3B. During the layout design, every semiconductor island 23 (corresponding to the Fins) in the design is required to have a digitalized value and digitalized location so that it can fit into the digitalized semiconductor-on-insulator substrate 18 where the lines 20 have a pitch of d. This can be easily done since the pitch d is so small (less than a few hundred nm), and any island 23 in the IC layout design can fit into the digitalized semiconductor-on-insulator substrate 18 by simply shifting the location by a distance less than the pitch size. The next step is to pattern the digitalized semiconductor-on-insulator substrate 18 into a desired structure according to the particular IC layout design 22, by simply removing part of the lines 20, as shown in FIG. 3C.

The benefit of the digitalized semiconductor-on-insulator substrate is that the digitalized semiconductor-on-insulator substrate can be produced in large volume without knowing the individual multiple-gate IC layout design. Therefore, the cost will be low due to the large volume. It also makes the IC device fabrication simple, since the Fin formation is one critical step. It is a general substrate for multiple-gate FET IC application. The requirement is that all the semiconductor islands on the IC layout have the same width and same height. This requirement is naturally met in FinFET or Tri-gate FET technology, where all the fins, i.e., lines, have the same dimension.

Although all the fins of a FinFET or a Tri-gate FET have the same dimensions and are separated from one another with an identical pitch, their source or drain regions typically have larger sizes than the channel fins, and all the fins join together

in the source and drain region. FIGs. 4A-4B show the technique used to make larger the size of the source or drain out of the digitalized semiconductor-on-insulator substrate. FIGs. 4A-4B illustrate the formation of the source/drain regions 26 of FinFET devices. The semiconductor lines (fins) 28 on a digitalized semiconductor-on-insulator substrate are patterned into desired structure 32 according to the IC layout design, as shown in FIG. 4A. Then a semiconductor regrowth step is performed on the source/drain region 26 to join various lines 28 together, as shown in FIG. 4B. This can be achieved during the conventional raised source/drain epi regrowth step. The raised source/drain epi regrowth step is a typically performed on thin SOI devices in order to increase the thickness of source/drain areas to facilitate source/drain contact. The lines 28 between the source/drain region 26 are fins for the FinFET device.

Note the semiconductor structures discussed herein can be comprised of various materials, such as Si, Ge, SiGe, SiC, GaAs, or other III-V materials, strained or unstrained etc. The typical SOI and FinFET device are made of Si material.

FIGs. 5A-5C and FIGs. 6A-6B illustrate techniques to produce digitalized semiconductor-on-insulator substrates in accordance with the invention. This inventive technique provides an approach to produce digitalized semiconductor-on-insulator substrates with uniform layers and structures with desired thicknesses. Moreover, the inventive technique produces digitalized semiconductor-on-insulator substrates without costly processes, such as high dose ion implantation or wafer bonding as in the conventional SOI fabrication.

FIG. 5A shows a SiGe or Si layer 51 formed on a single crystal semiconductor substrate 50, which can be a Si substrate or a SiGe virtual substrate, for example. A top layer 52 is formed on the layer 51, and can be either a SiGe or Si layer. The top layer 52 can also be converted into a porous layer. A single crystal device layer 54 of either SiGe or Si is then formed on the top layer 50, for example, by using standard epi techniques. The device layer 54 is then patterned into digitalized semiconductor lines 56. Selective etching is then performed as shown in FIG. 5B. Since the SiGe layer or porous layer 52 etches faster, the layer 52 is etched away while the digitalized semiconductor lines 56 remain. An insulator material is refilled in the space area to form a buried insulator layer 58, resulting in a digitalized SOI structure, as shown in FIG 5C. The presence of the insulating layer in the structure gives various benefits for the device fabricated on this structure, such as reduced parasitic capacitor, which

results in faster circuit speed or lower power consumption, etc.

FIGs. 6A-6B show another approach to the technique discussed with reference to FIGs. 5A-5C. In particular, FIG. 6A shows a SiGe or Si layer 61 formed on a single crystal semiconductor substrate 60. A top layer 62 is formed on the layer 61, and can be either a SiGe or Si layer. The top layer 62 can also be converted into porous material in one alternative embodiment. Then a single crystal device layer 64 of either SiGe or Si is formed on the top layer 62, for example, by using standard epi techniques, as shown in FIG. 6A. The device layer 64 is then patterned into digitalized semiconductor lines 66. Selective oxidation or nitridation is then performed to convert the layer 62 into insulator 68. Since the SiGe layer or porous layer 62 oxidizes faster and since the dimension is very small, the layer 62 converts to insulator quickly while the digitalized semiconductor lines 66 are still there, as shown in FIG. 6B.

In yet another aspect of the invention, a technique is provided to produce a digitalized strained-Si-on-insulator substrate to be used with strained-Si FinFET applications, and a process to produce strained-Si FinFET devices.

FIGs. 7A-7E illustrate the formation of a digitalized strained-Si Fin structures. In particular, FIG. 7A shows a digitalized relaxed-SiGe-on-insulator substrate 70 having SiGe relaxed digitized structures or lines 72 and insulating substrate 71. Epi strained-Si layers 74 are grown on the sidewalls of the SiGe lines 72 on the substrate 70, as shown in FIG. 7B. Strained-Si FinFET devices can be then made on this substrate 70. Note the epi strained-Si layers 74 can also be grown before the step of forming the insulator layer, as discussed in FIGs. 5A-5C and FIGs. 6A-6C, but after patterning the SiGe layer into digitalized lines.

FIGs. 7C illustrate another embodiment of a digitalized strained-Si fin structure, where epi strained-Si layers 75 are not only grown on the two sidewalls of the SiGe lines 72 on the substrate 70, but also on the top surface of SiGe lines 72.

FIGs. 7D-7E illustrate yet another embodiment of a digitalized strained-Si fin structure 76. It starts with a uniform strained-Si layer 79 on the substrate 70, as shown in FIG. 7D. The layer 79 is then patterned into digitalized lines 78, as shown in FIG. 7E. The embodiments shown in FIGs. 7A-7E of strained-Si substrates have different directions of strain. In the above structure 76, the lines 78 can be other materials, such Ge, SiGe, SiC, strained or unstrained.

FIGs. 8A show a conventional Si multiple-gate FET transistor 100, fabricated

on a SOI substrate 102. FIG. 8B shows the top view of a conventional Si FinFET or a conventional Si Tri-gate FET 100. FIG. 8C and FIG. 8D show the cross-section views of the same device 100 in two different directions. The conventional Si FinFET or Tri-gate device 100 has several separate Si channel regions 104 (fin-shaped) in between a source region 106 and drain region 108. The fin-shaped channel 104 typically has small heights. In order to have a good contact on source/drain regions, 106, 108 a typical raised source/drain epi regrowth step is used to increase the heights of the source/drain regions 106, 108. The FinFET and Tri-Gate FET devices in the prior art differ in the number of gates.

FIGs. 8E-8F illustrate the detailed structures of the FinFET and Tri-gate device, in particular the MOSFET device. FIG. 8E illustrates a gate region 80 on the substrate 77. The gate region 80 includes two portions: a gate portion 82 and a channel portion 84, which includes one of the line structures 104 from FIG. 8A-8D. The gate portion 82 includes two opposite gate conductors 86 adjacent to a channel portion 84 and insulating film 90. The gate conductors 86 can be semiconductor or metal materials. The insulating film 90 can be a silicon oxide, nitride or high-k dielectric material, such as HfO_2, ZrO_2, Hfn. The source/drain diffusion regions abut the gate region 80, and have junctions connecting to the two ends of the channel portion 84. FIG. 8F shows the gate structure 92 of a Tri-gate FET. It is similar to the structure 75 shown in FIG. 8E, except the gate conductor 94 of the structure 92 shown in FIG. 8F includes a horizontal top portion 96.

In order to make the multiple-gate devices on a SOI wafer having controllable performance, the uniformity of the height of all channel strips across the entire wafer, which originates from the uniformity of the starting SOI wafer, is very crucial. Multiple-gate device also require to start with ultra-thin SOI wafers. However, the conventional methods for SOI substrate production have limitations in film thickness and thickness uniformity. The conventional methods also typically involve costly processes such as high dose ion implantation or wafer bonding.

The invention provides a multiple-gate FET device structure which does not require SOI substrates, and provides much improved fin film thickness uniformity. FIG. 9A shows the top view of the multiple-gate FET device. FIGs. 9B and 9C show the cross-section view in Y-Y and X-X directions respectively. This inventive multiple-gate FET device 110 is fabricated directly on a bulk Si substrate 112 having a source 116 and drain 118. Note the substrate 112 can also be a SiGe substrate or the

like in other embodiments. Thanks to the multiple-gate structure, the fin-shaped channel regions 114 maintain the same device performance as those made on an insulating substrate 102. In one embodiment, the substrate 112 beneath the fin-shaped channel region 114 is doped such that it never turns on, therefore minimizes the influence of the bulk semiconductor substrate on the device performance.

The difference between this structure and the conventional multiple-gate FET in FIG 8 is the substrate, i.e. bulk Si substrate in FIG. 9 versus insulating substrate in FIG. 8. The advantage of such a multiple-gate FET 110 on bulk substrate 112 is three-fold: (1) low wafer cost due to the use of bulk substrate 112 instead of an insulating substrate, (2) uniform fin-shaped strip height across the entire wafer, as it is defined by etch process which forms the fins, and (3) no floating-body effect since it is not a SOI structure.

The invention also provides a high mobility multiple-gate FET device structure. By using strained-semiconductor materials or high Ge content materials such as strained-Si, strained-SiGe, or strained-Ge, the device's electron and hole mobility are improved dramatically. However, the use of strained-material is not straightforward. FIGs. 10A-10C show three different fin-shaped channel region structures used to form strained-material multiple-gate devices, using tensile strained-Si as an example. In FIG 10A, the fin strip 120 is formed directly from a strained-Si on insulator (SSOI) substrate 122. The fin strip 120 has 3 surfaces 124, 126, 128. As indicated in the FIG. 10A, the top horizontal surface 124 exhibit a biaxial tensile strain in both X and Y directions. The other two vertical surfaces, 126, 128, however, exhibit uniaxial tensile strain, i.e. tensile strain in Y direction only. In the Z direction, it is compressive strain. As understood in the prior art, biaxial tensile strained-Si shows better mobility enhancement than uniaxial strained-Si.

FIG. 10B shows another structure 130. In this structure 130, a relaxed SiGe strip 132 is formed first on a substrate 134. Then a strained-Si regrowth can be performed to form strained-Si films on the two vertical surfaces 136, 138 of the relaxed-SiGe strips 132. As a result, both strained-Si films on the two vertical surfaces 136, 138 are in biaxial tensile strain, in both Y and Z directions. This is a multiple-gate device with the gate portion structure same as the one shown in FIG. 8E (FinFET). If strained-Si is also deposited on the top horizontal surface 140 in FIG. 10B, it is also biaxial strained, in both X and Y direction, as shown in FIG. 10C. This is a multiple-gate device with the gate portion structure same as the one shown in

FIG. 8F (Tri-gate FET). In other embodiments, other strained-materials, such as strained-SiGe or strained-Ge, can be used. In these structures, the substrate 122 and 134 can be either an insulating substrate, like the one in FIG. 8, or a bulk semiconductor substrate, like the one in FIG. 9.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A multiple-gate field effect transistor (FET) structure comprising:

a semiconductor substrate,

a gate region formed on said semiconductor substrate, said gate region comprising a gate portion and a channel portion, said gate portion having at least two opposite vertical surfaces adjacent to the channel portion;

a source region abutting said gate region at one end; and

a drain diffusion region abutting said gate region at the other end.

2. The multiple-gate FET structure of claim 1, wherein said channel portion comprises either a Si channel, a strained-Si channel, a relaxed-SiGe channel, a strained-SiGe channel, a relaxed-Ge channel, a strained-Ge channel, a SiC channel, a GaN channel a GaAs channel, or other III-V material channel.

3. The multiple-gate FET structure of claim 1, wherein said channel portion comprises a center relaxed-semiconductor material region and an outer strained-semiconductor material region that covers at least the two opposite vertical surfaces of the center relaxed-semiconductor material region, and said semiconductor substrate comprises Si, SiGe, SiC, Ge, GaN, GaAs or other III-V materials.

4. The multiple-gate FET structure of claim 3, wherein said center relaxed-semiconductor material is either a relaxed-Si, a relaxed-SiGe, or a relaxed-SiC, and said outer strained-semiconductor material comprises either strained-Si, strained-SiGe, strained-SiC or strained-Ge material.

5. The multiple-gate FET structure of claim 1, wherein said semiconductor substrate comprises a bulk semiconductor substrate, such as a bulk Si substrate, a bulk Ge substrate, a bulk SiGe virtual substrate, a bulk GaAs substrate.

6. The multiple-gate FET structure of claim 1, wherein said semiconductor substrate comprises an insulating substrate.

7. The multiple-gate FET structure of claim 6, wherein said insulating substrate comprises an insulating layer of one of the following material: an SOI material, an SSOI (strained-Si on insulator) material, an SGOI (SiGe on insulator) material, a strained-SGOI (strained-SiGe on insulator) material, a GOI (Ge on insulator) material,

or a strained-GOI (strained-Ge on insulator) material.

8. The multiple-gate FET structure of claim 1, wherein said gate portion further comprises a conducting material film and an insulating film, said insulating film having at least two opposite vertical surfaces adjacent to the channel regions and separating said gate conductor from said channel portion.

9. The multiple-gate FET structure of claim 1, wherein said gate portion comprises a poly Si material, or a metal-gate material such as TiN, Mo, Ti.

10. The multiple-gate FET structure of claim 8, wherein said insulating film comprises a high-k dielectric material.

11. The multiple-gate FET structure of claim 1, wherein said high-k dielectric material comprises HfO_2, ZrO_2, HfN.

12. A multiple-gate field effect transistor (FET) structure comprising:

a semiconductor substrate,

a gate region formed on said semiconductor substrate, said gate region comprising a gate portion and a channel portion, said gate portion having at two opposite verticals surface and one horizontal top surface adjacent to the channel portion; and

a source region abutting said gate region at one end; and

a drain diffusion region abutting said gate region at the other end.

13. The multiple-gate FET structure of claim 12, wherein said channel portion comprises either a Si channel, a strained-Si channel, a relaxed-SiGe channel, a strained-SiGe channel, a relaxed-Ge channel, a strained-Ge channel, a SiC channel, a GaN channel or other III-V materials.

14. The multiple-gate FET structure of claim 12, wherein said channel portion comprises a center relaxed-semiconductor material region and an outer strained-semiconductor material region that covers at least the two opposite vertical surfaces of the center relaxed-semiconductor material region.

15. The multiple-gate FET structure of claim 14, wherein said center relaxed-semiconductor material is either a relaxed-Si, a relaxed-SiGe, or a relaxed-SiC, and

said outer strained-semiconductor material comprises either strained-Si, strained-SiGe, strained-SiC or strained-Ge material, and said semiconductor substrate comprises Si, SiGe, SiC, Ge, GaN, GaAs or other III-V materials.

16. The multiple-gate FET structure of claim 12, wherein said semiconductor substrate comprises a bulk semiconductor substrate, such as a bulk Si substrate, a bulk Ge substrate, a bulk SiGe virtual substrate, a bulk GaAs substrate.

17. The multiple-gate FET structure of claim 12, wherein said semiconductor substrate comprises an insulating substrate.

18. The multiple-gate FET structure of claim 17, wherein said insulating substrate comprises an insulating layer of one of the following material: an SOI material, an SSOI (strained-Si on insulator) material, an SGOI (SiGe on insulator) material, a strained-SGOI (strained-SiGe on insulator) material, a GOI (Ge on insulator) material, or a strained-GOI (strained-Ge on insulator) material.

19. The multiple-gate FET structure of claim 12, wherein said gate portion further comprises a conducting material film and an insulating film, said insulating film having at least two opposite vertical surfaces adjacent to the channel regions and separating said gate conductor from said channel portion.

20. The multiple-gate FET structure of claim 12, wherein said gate portion comprises or a poly Si material a metal-gate material such as TiN, Mo, Ti.

21. The multiple-gate FET structure of claim 19, wherein said insulating film comprises a high-k dielectric material.

22. The multiple-gate FET structure of claim 21, wherein said high-k dielectric material comprises HfO_2, ZrO_2, Hfn.

23. A digitalized semiconductor structure comprising:

a semiconductor substrate; and

a plurality of fin-shaped strips formed on said semiconductor substrate, said fin-shaped strips having identical widths and identical heights and being distributed evenly throughout the entire substrate, with a feature pitch d between one another.

24. The digitalized semiconductor structure of claim 23, wherein each of said fin-

shaped strips comprises a width and a height ranging between 1 nm and 200 nm.

25. The digitalized semiconductor structure of claim 23, wherein said pitch d comprises a range between 5 nm and 500 nm.

26. The digitalized semiconductor structure of claim 23, wherein said semiconductor substrate comprises a bulk semiconductor substrate, such as a bulk Si substrate, a bulk Ge substrate, a bulk SiGe virtual substrate, a bulk GaAs substrate.

27. The digitalized semiconductor structure of claim 23, wherein said semiconductor substrate comprises an insulating substrate.

28. The digitalized semiconductor structure of claim 27, wherein said insulating substrate comprises an insulating layer of one of the following material: an SOI material, an SSOI (strained-Si on insulator) material, an SGOI (SiGe on insulator) material, a strained-SGOI (strained-SiGe on insulator) material, a GOI (Ge on insulator) material, or a strained-GOI (strained-Ge on insulator) material.

29. The digitalized semiconductor structure of claim 23, wherein said fin-shaped strips comprise either Si, strained-Si, relaxed-SiGe, strained-SiGe, relaxed-Ge, strained-Ge, SiC, GaN, GaAs, other III-V materials, or a semiconductor comprising of more than one material.

30. The digitalized semiconductor structure of claim 31, wherein said semiconductor comprises a center relaxed-semiconductor material region and an outer strained-semiconductor material region that covers at least the two opposite vertical surfaces of the center relaxed-semiconductor material region.

31. The digitalized semiconductor structure of claim 30, wherein said center relaxed-semiconductor material is either a relaxed-Si, a relaxed-SiGe, or a relaxed-SiC, GaN, GaAs, other III-V materials and said outer strained-material comprises either strained-Si, strained-SiGe, strained-SiC, or strained-Ge material.

32. The digitalized semiconductor structure of claim 30, wherein said outer strained-semiconductor material region further covers the horizontal top surfaces of the center relaxed-semiconductor material region.

33. A method of forming a multiple-gate field effect transistor (FET) structure

comprising comprising:

providing a semiconductor substrate,

forming a gate region formed on said semiconductor substrate, said gate region comprising a gate portion and a channel portion, said gate portion having at least two opposite vertical surfaces adjacent to the channel portion;

forming a source region abutting said gate region at one end; and

forming a drain diffusion region abutting said gate region at the other end.

34. The method of claim 33, wherein said channel portion comprises either a Si channel, a strained-Si channel, a relaxed-SiGe channel, a strained-SiGe channel, a relaxed-Ge channel, a strained-Ge channel, or a SiC channel.

35. The method of claim 33, wherein said channel portion comprises a center relaxed-semiconductor material region and an outer strained-semiconductor material region that covers at least the two opposite vertical surfaces of the center relaxed-semiconductor material region.

36. The method of claim 35, wherein said center relaxed-semiconductor material is either a relaxed-Si, a relaxed-SiGe, or a relaxed-SiC, and said outer strained-semiconductor material comprises either strained-Si, strained-SiGe, strained-SiC or strained-Ge material, and said semiconductor substrate comprises Si, SiGe, SiC, Ge, GaN, GaAs or other III-V materials.

37. The method of claim 33, wherein said semiconductor substrate comprises a bulk Si substrate.

38. The method of claim 34, wherein said semiconductor substrate comprises an insulating substrate.

39. The method of claim 38, wherein said insulating substrate comprises an insulating layer of one of the following material: an SOI material, an SSOI (strained-Si on insulator) material, an SGOI (SiGe on insulator) material, a strained-SGOI (strained-SiGe on insulator) material, a GOI (Ge on insulator) material, or a strained-GOI (strained-Ge on insulator) material.

40. The method of claim 33, wherein said gate portion further comprises a conducting material film and an insulating film, said insulating film having at least two opposite

vertical surfaces adjacent to the channel regions and separating said gate conductor from said channel portion.

41. The method of claim 33, wherein said gate portion comprises a metal-gate material.

42. The multiple-gate FET structure of claim 41, wherein said insulating film comprises a high-k dielectric material.

43. The method of claim 33, wherein said high-k dielectric material comprises HfO.

44. A method of forming a multiple-gate field effect transistor (FET) structure comprising:

providing a semiconductor substrate,

forming a gate region formed on said semiconductor substrate, said gate region comprising a gate portion and a channel portion, said gate portion having at two opposite vertical surface and one horizontal top surface adjacent to the channel portion; and

forming a source region abutting said gate region at one end; and

forming a drain diffusion region abutting said gate region at the other end.

45. The method of claim 44, wherein said channel portion comprises either a Si channel, a strained-Si channel, a relaxed-SiGe channel, a strained-SiGe channel, a relaxed-Ge channel, a strained-Ge channel, or a SiC channel.

46. The method of claim 44, wherein said channel portion comprises a center relaxed-semiconductor material region and an outer strained-semiconductor material region that covers at least the two opposite vertical surfaces of the center relaxed-semiconductor material region.

47. The method of claim 46, wherein said center relaxed-semiconductor material is either a relaxed-Si, a relaxed-SiGe, or a relaxed-SiC, and said outer strained-semiconductor material comprises either strained-Si, strained-SiGe, strained-SiC or strained-Ge material, and said semiconductor substrate comprises Si, SiGe, SiC, Ge, GaN, GaAs or other III-V materials.

48. The method of claim 44, wherein said semiconductor substrate comprises a bulk

Si substrate.

49. The method of claim 44, wherein said semiconductor substrate comprises an insulating substrate.

50. The method of claim 49, wherein said insulating substrate comprises an insulating layer of one of the following material: an SOI material, an SSOI (strained-Si on insulator) material, an SGOI (SiGe on insulator) material, a strained-SGOI (strained-SiGe on insulator) material, a GOI (Ge on insulator) material, or a strained-GOI (strained-Ge on insulator) material.

51. The method of claim 44, wherein said gate portion further comprises a conducting material film and an insulating film, said insulating film having at least two opposite vertical surfaces adjacent to the channel regions and separating said gate conductor from said channel portion.

52. The method of claim 44, wherein said gate portion comprises a metal-gate material.

53. The method of claim 51, wherein said insulating film comprises a high-k dielectric material.

54. A method of forming a digitalized semiconductor structure comprising:

providing a semiconductor substrate; and

forming a plurality of fin-shaped strips formed on said semiconductor substrate, said fin-shaped strips having identical widths and identical heights and being distributed evenly throughout the entire substrate, with a feature pitch d between one another.

55. The method of claim 54, wherein each of said fin-shaped strips comprises a width and a height ranging between 1 nm and 200 nm.

56. The method of claim 54, wherein said pitch d comprises a range between 5 nm and 500 nm.

57. The method of claim 54, wherein said semiconductor substrate comprises a bulk Si substrate.

58. The method of claim 54, wherein said semiconductor substrate comprises an insulating substrate.

59. The method of claim 58, wherein said insulating substrate comprises an insulating layer of one of the following material: an SOI material, an SSOI (strained-Si on insulator) material, an SGOI (SiGe on insulator) material, a strained-SGOI (strained-SiGe on insulator) material, a GOI (Ge on insulator) material, or a strained-GOI (strained-Ge on insulator) material.

60. The method of claim 54, wherein said fin-shaped strips comprise either Si, strained-Si, relaxed-SiGe, strained-SiGe, relaxed-Ge, strained-Ge, SiC, or a semiconductor comprising of more than one material.

61. The method of claim 60, wherein said semiconductor comprises a center relaxed-semiconductor material region and an outer strained-semiconductor material region that covers at least the two opposite vertical surfaces of the center relaxed-semiconductor material region.

62. The method of claim 61, wherein said center relaxed-semiconductor material comprises either a relaxed-Si, a relaxed-SiGe, or a relaxed-SiC, and said outer strained-material comprises either strained-Si, strained-SiGe, strained-SiC or strained-Ge material.

63. The method of claim 61, wherein said outer strained-semiconductor material region further covers the horizontal top surfaces of the center relaxed-semiconductor material region.

64. A method of forming a digitalized semiconductor structure comprising:

providing a semiconductor substrate;

forming a first semiconductor layer on said substrate;

forming a second semiconductor layer on said first semiconductor layer, and said second semiconductor layer is different from said first semiconductor layer;

patterning said second semiconductor layer into a plurality of fin-shaped strips, said fin-shaped strips having identical heights, identical widths, and being distributed evenly throughout the entire substrate, with a feature pitch d between one another; and

converting said first semiconductor layer into a buried oxide layer.

65. The method of claim 64, wherein said semiconductor substrate comprises a Si substrate, or a SiGe virtual substrate with a relaxed SiGe film on a top layer.

66. The method of claim 64, wherein said first layer comprises either a Si layer, a strained-Si layer, a relaxed-SiGe layer, a strained-SiGe layer, a relaxed-Ge layer, a strained-Ge layer, or a SiC layer.

67. The method of claim 64, wherein said second layer comprises either a Si layer, a strained-Si layer, a relaxed-SiGe layer, a strained-SiGe layer, a relaxed-Ge layer, a strained-Ge layer, or a SiC layer, and said first layer is different from said second layer by different material or by different doping type.

68. The method of claim 64, wherein said first layer comprises a faster oxidation or nitridation rate than the second layer, and said first layer is converted into a buried oxide layer by selectively oxidation or nitridation.

69. The method in claim 64, wherein said first layer comprises faster etch rate than the second layer, and said first layer is converted into a buried oxide layer by selectively etching away the first layer and then the empty spaces are fill with insulator.

70. The method of claim 64 further comprising forming multiple-gate FET devices on the structure.

71. A method of forming a digitalized semiconductor structure comprising:

providing a semiconductor substrate;

forming a first semiconductor layer on said substrate;

converting said first semiconductor layer into a first porous semiconductor layer;

forming a second semiconductor layer on said first porous semiconductor layer;

patterning said second semiconductor layer into a plurality of fin-shaped strips, said fin-shaped strips having identical heights, identical widths, and being distributed evenly throughout the entire substrate, with a feature pitch d between one another; and

converting said first porous semiconductor layer into a buried oxide layer.

72. The method of claim 71, wherein said semiconductor substrate comprises a Si substrate or a SiGe virtual substrate with a relaxed SiGe film on a top layer.

73. The method of claim 71, wherein said first layer comprises either a Si layer, a strained-Si layer, a relaxed-SiGe layer, a strained-SiGe layer, a relaxed-Ge layer, a strained-Ge layer, or a SiC layer.

74. The method of claim 71, wherein said second layer comprises either a Si layer, a strained-Si layer, a relaxed-SiGe layer, a strained-SiGe layer, a relaxed-Ge layer, a strained-Ge layer, or a SiC layer.

75. The method in claim 71, wherein said first porous semiconductor layer is converted into a buried oxide layer by selectively oxidizing said first porous layer.

76. The method in claim 71 wherein said first porous semiconductor layer is converted into a buried oxide layer by selectively etching away said first porous layer and then the empty spaces are filled with oxide.

77 The method in claim 71 further comprising forming multiple-gate FET devices on the structure.

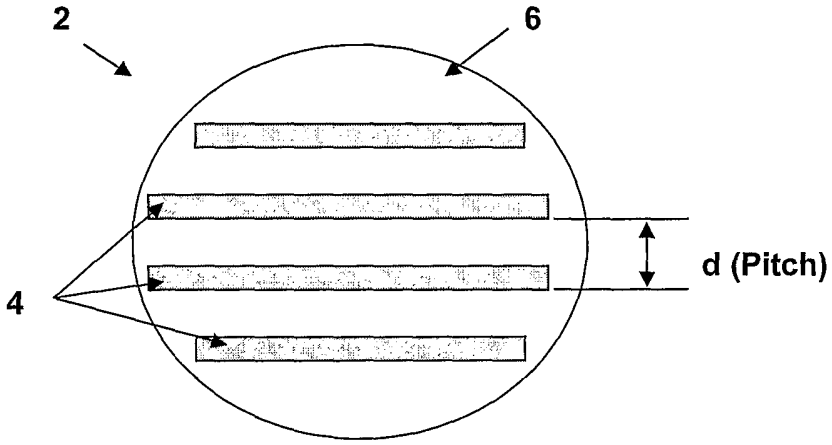


FIG. 1A

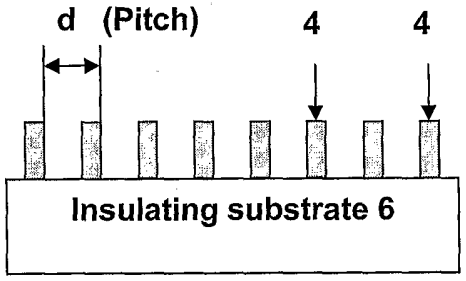


FIG. 1B

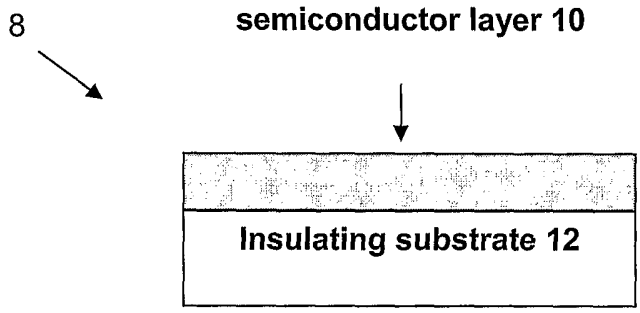


FIG. 2A

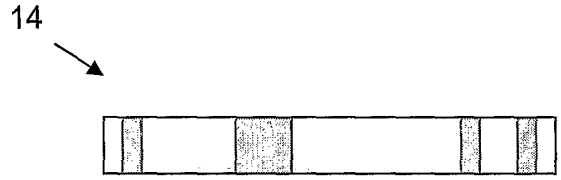


FIG. 2B

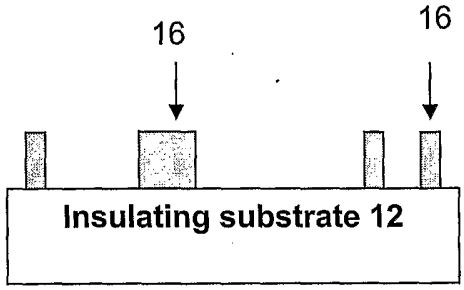


FIG. 2C

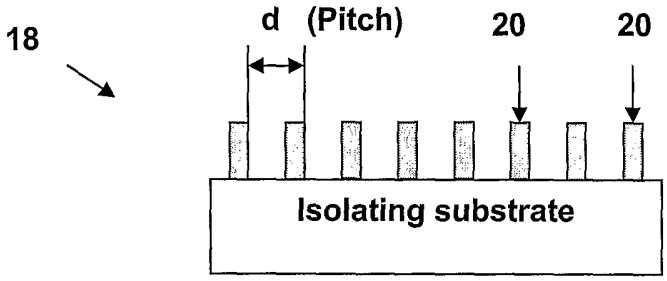


FIG. 3A

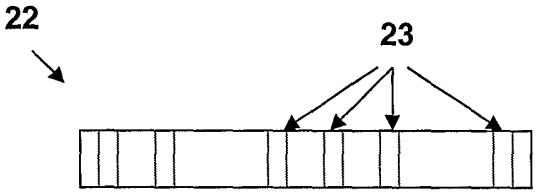


FIG. 3B

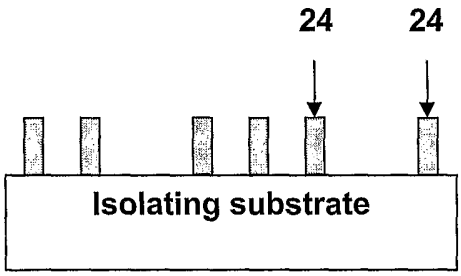


FIG. 3C

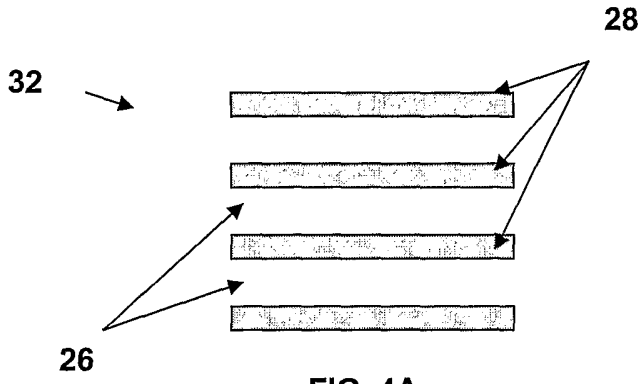


FIG. 4A

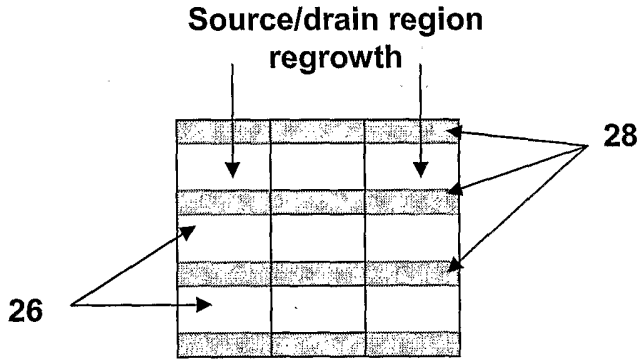


FIG. 4B

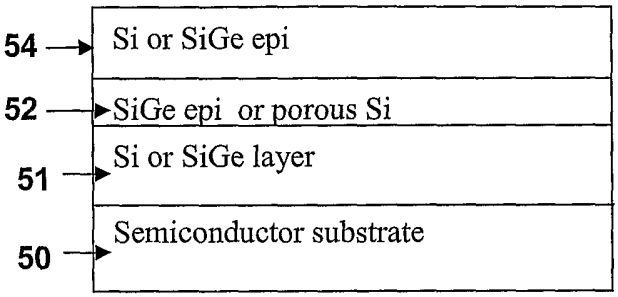


FIG. 5A

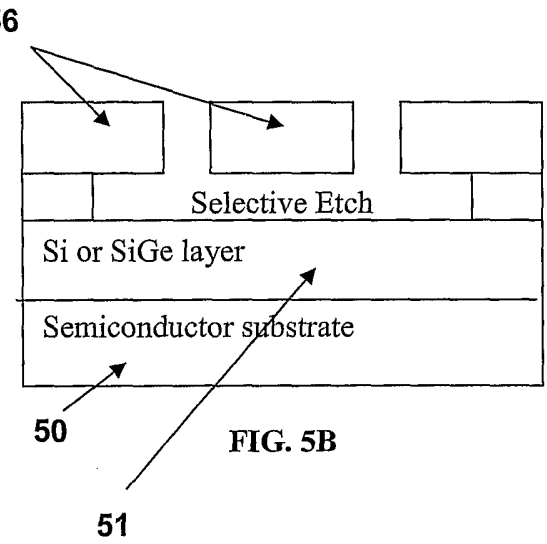


FIG. 5B

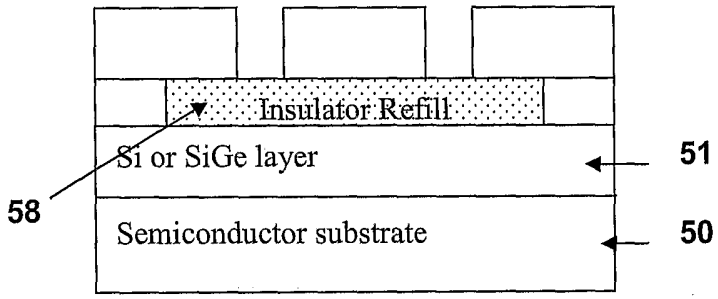


FIG. 5C

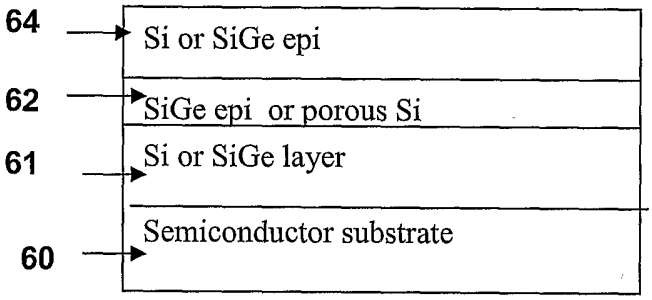

64
Si or SiGe epi
62
SiGe epi or porous Si
61
Si or SiGe layer
Semiconductor substrate
60

FIG. 6A

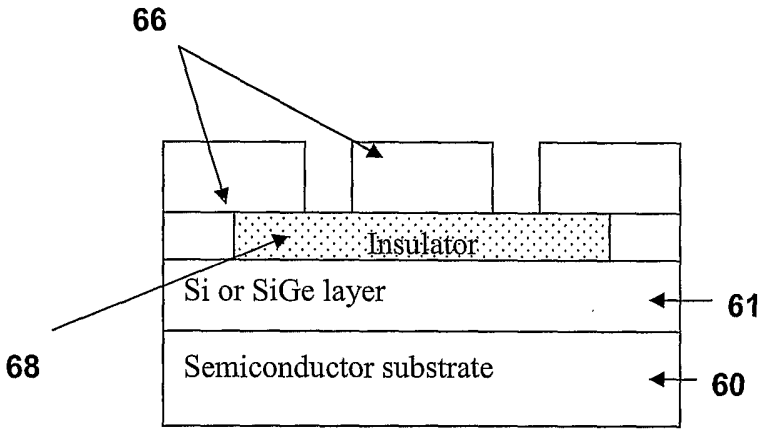

66
Insulator
Si or SiGe layer
61
68
Semiconductor substrate
60

FIG. 6B

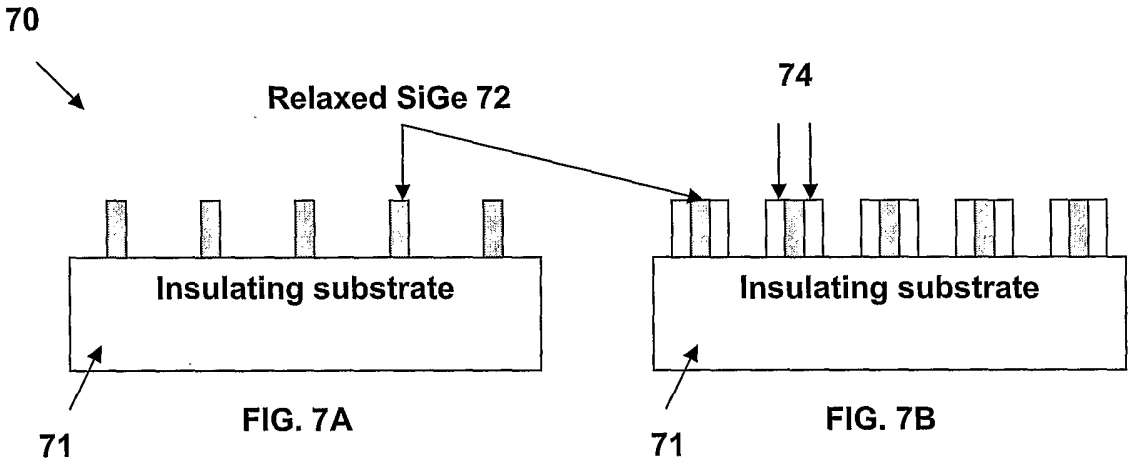


FIG. 7A FIG. 7B

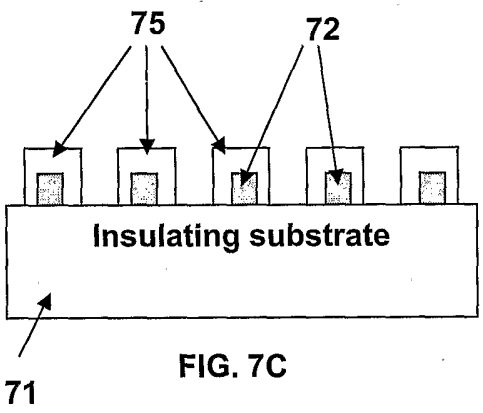


FIG. 7C

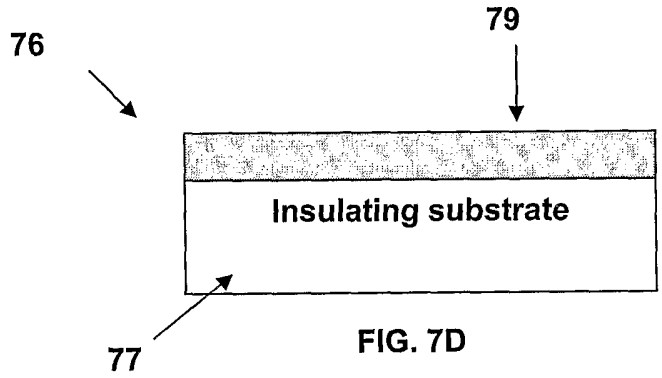

76
79
Insulating substrate
77

FIG. 7D

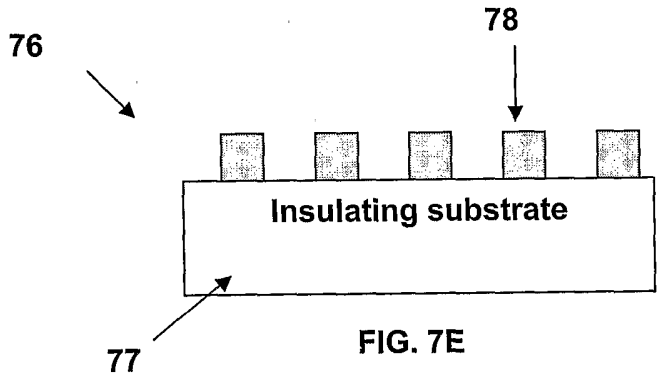

76
78
Insulating substrate
77

FIG. 7E

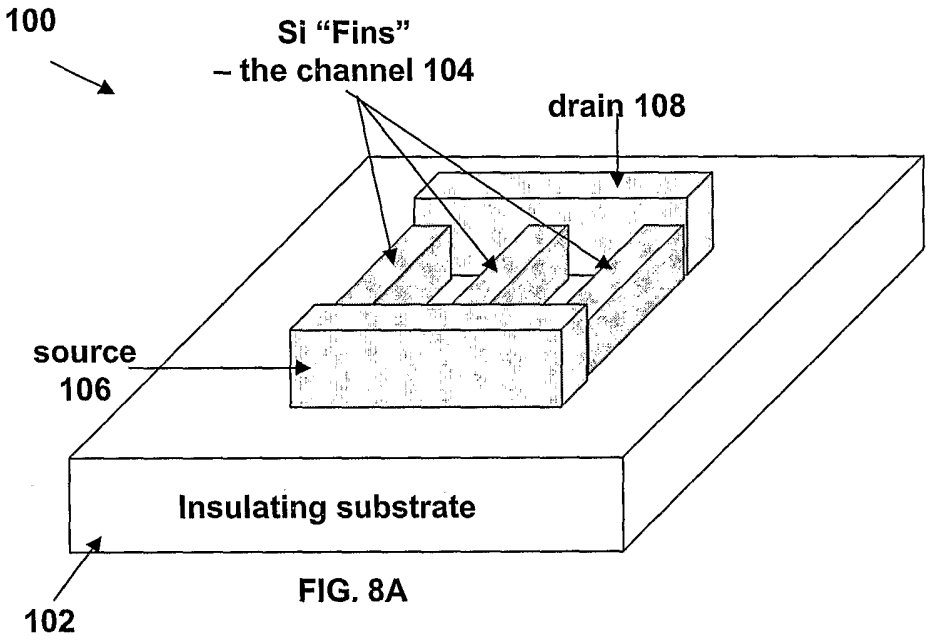

100
Si "Fins"
– the channel 104
drain 108
source
106
Insulating substrate
102

FIG. 8A

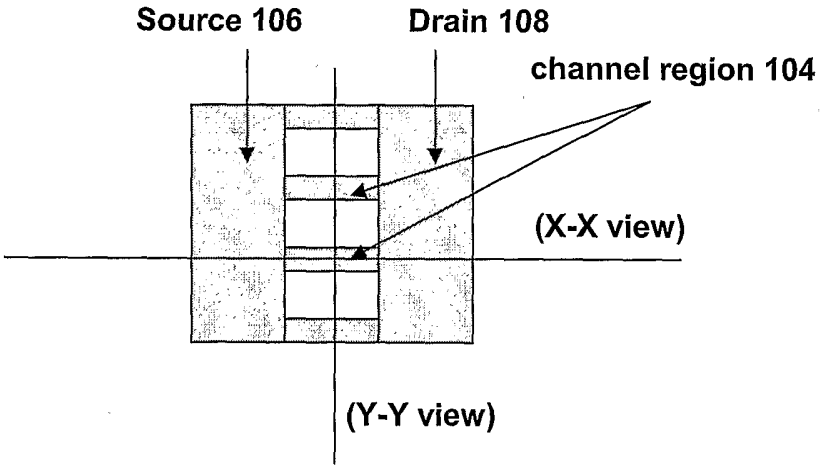


FIG. 8B (top view)

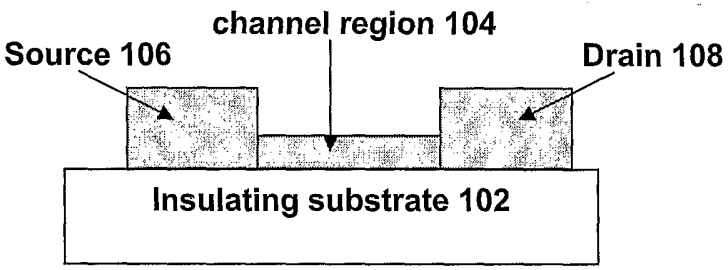


FIG. 8C (X-X view)

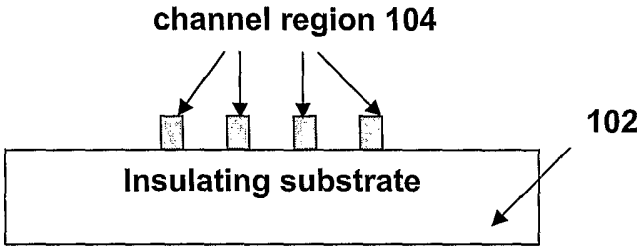


FIG. 8D (Y-Y view)

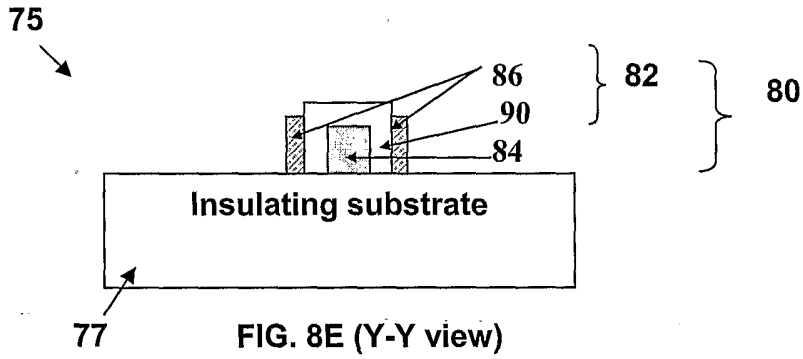


FIG. 8E (Y-Y view)

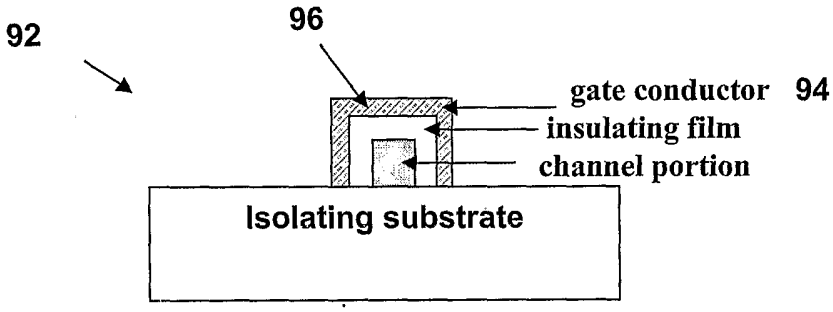


FIG. 8F (Y-Y view)

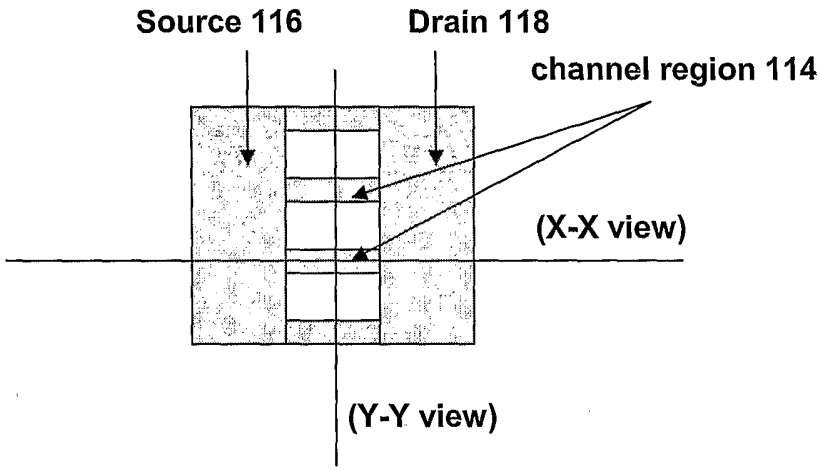


FIG. 9A (top view)

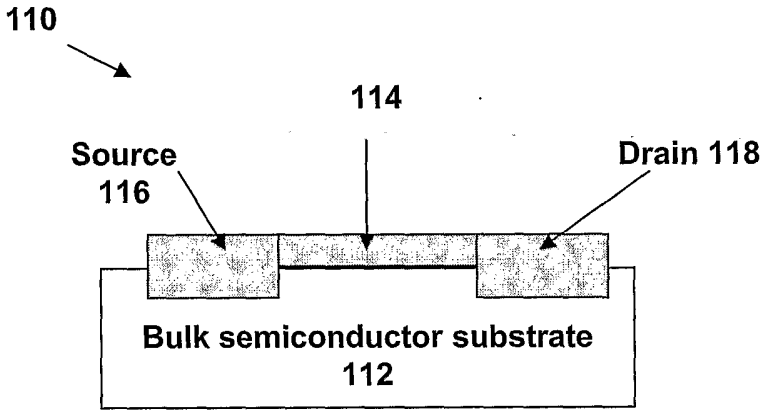


FIG. 9B (X-X view)

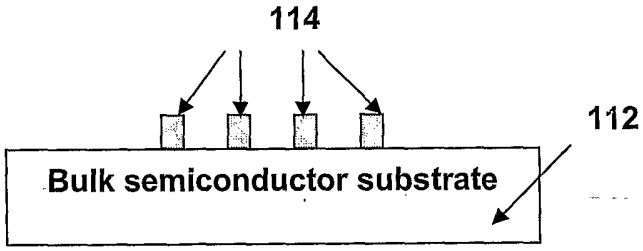


FIG. 9C (Y-Y view)

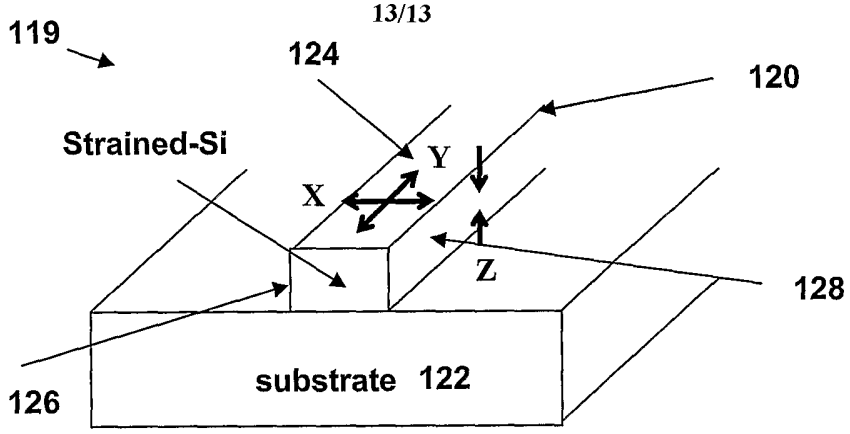


FIG. 10A

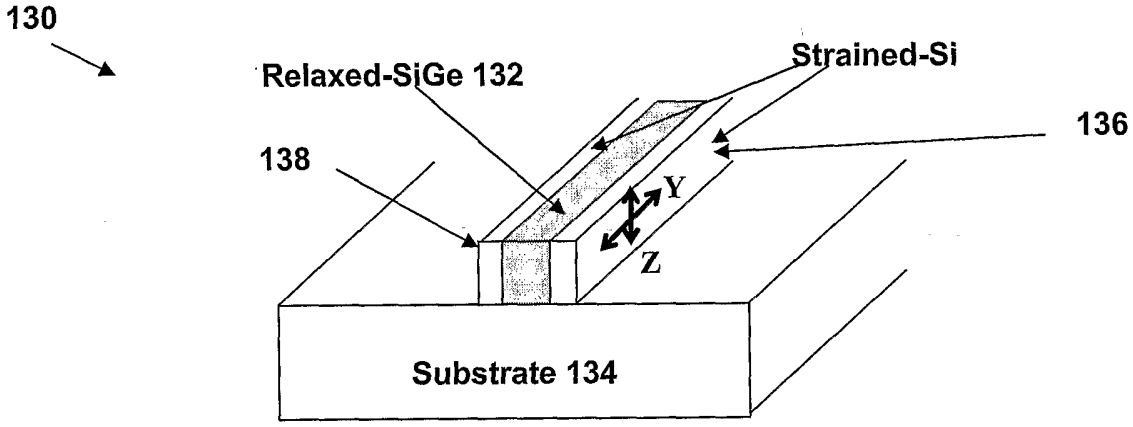


FIG. 10B

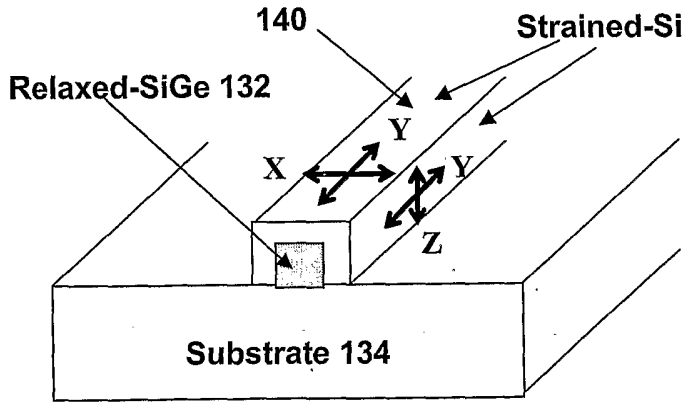


FIG. 10C