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Title: METHOD OF FABRICATING MODE-SIZE CONVERTER WITH THREE-DIMENSIONAL TAPER

Abstract: A three-dimensional taper geometry is employed in passive and active waveguide components. The structure has two portions with tapering in both the lateral and vertical direction.
Method Of Fabricating Mode-Size Converter With Three-Dimensional Taper

Field of the Invention
[0001] This invention relates to the field of photonics, and in particular to a method of fabricating a mode-size converter with a three-dimensional taper.

Background of the Invention
[0002] The effective coupling of light to an optical fiber is a critical aspect of many optical communication systems and industries. Optical modes in waveguides with small dimensions, particularly waveguides with high refractive index contrast, are mismatched to the optical modes in fibers commonly used in fiber optic communications. Modal mismatches may result in a 7 to 10 dB insertion loss. Proper means need to be employed to improve the waveguide to fiber coupling. The above-described problem exists for both passive and active waveguide components. Much work has been done in the past to address the mismatch between optical modes in lasers and fibers, and semiconductor waveguide devices have been developed to try to solve this mode-matching problem. One method for accomplishing such is with the use of tapered waveguides (or often referred to as mode-size converter, mode-size transformer). Tapered waveguides offer a monolithically-integrated means by which efficient coupling can be achieved. Briefly, a tapered region in a semiconductor waveguide device acts to adiabatically (with minimum optical loss) control the expansion of a propagating wave and therefore, the resultant mode-size of the guided optical wave. A properly designed tapered waveguide supports a mode of comparable size as in fibers at one end, and transforms the mode adiabatically to an appropriate size at the other end as required by other waveguide optical components. These tapers may be formed through various techniques. Most of these approaches, however, require complex growth or processing steps such as multiple etch-regrowth or sequences or lithographic patterning of extremely small radius waveguide tips in order to achieve the desired coupler performance.
Several geometries of tapers have been proposed previously, with different degrees of success. Lateral tapers have a tapered waveguide width, usually done through layout design. Typically, waveguide devices with lateral tapers are lithographically produced using sub-minor masking and etching procedures as exemplified in U.S. Patent 5,574,742. However, it is difficult to precisely control these lithographic processes and the resultant tapers are not easily reproducible. Vertical tapers have similar changes but in the direction perpendicular to the waveguide surface. Vertical tapers can be more desirably fabricated using one of several different other techniques. These techniques include selective area growth/etch, shadow mask growth/etch, dip etch, and multiple etch-stop layers. However, these techniques require an extremely high degree of reproducibility as desired. Also, many of the devices fabricated by the conventional techniques in the past suffer from a high degree of optical loss during adiabatic mode conversion. Thus, the light emitted from these conventional tapered waveguide devices have improved output beam mode quality in terms of divergence, but at the cost of lower optical output power. A two-portion taper with the same material has also been proposed, wherein the upper portion tapers to a point, and the lower portion tapers to a smaller width suitable for a single mode waveguide. The mode is substantially transferred from the upper portion at the large end to the lower portion at the small end.

Lateral and vertical tapers only addresses the mode mismatch in one direction. The previously proposed two-portion taper only tapers in the lateral direction. Mode matching is facilitated in both directions. In order to force the mode down to the lower waveguide, the upper waveguide needs to be tapered gradually to a very narrow width. Any light remaining in the upper portion represents optical loss. Minimizing the width only is not sufficiently effective.

In known fabrication methods, two-portion tapers of the same material require uniform etching with smooth etched surfaces and precisely controlled etch
depth, in order not to degrade the performance of the lower portion waveguides and other associated waveguide components. To achieve a point termination in the upper portion (approximately 0.1 mm wide), high-resolution pattern definition methods, such as electro-beam lithography, are required. These kinds of methods are expensive and not suitable for volume production.

[0006] Therefore, there remains a need for improved waveguide coupler that can be made easily, and couple the light between a semiconductor optical device and an optical fiber with high efficiency.

Summary of the Invention

[0007] The invention relates to semiconductor optical devices, and more particularly to a ridge waveguide with taper that provides efficient coupling thereof into and out of an optical fiber.

[0008] An object of the invention is to provide a method of fabricating a vertical and horizontal waveguide taper in semiconductor devices that performs adiabatic mode conversion and provides high reproducibility of the desired mode profile in the output beam from the device. In accordance with the principles of the invention, a three-dimensional taper geometry is employed. The inventive structure has two portions with tapering in both the lateral and vertical directions.

[0009] Three-dimensional geometry provides more efficient coupling from the upper to the lower waveguide than previous designs. Two-layer tapers with a sandwich thin, optically 'invisible' etch-stop layer has relaxed constraints on processing controls. Oxidation for point termination eliminates the needs for high-resolution lithography, and makes the taper fabrication compatible with VLSI manufacturing.

[0010] Tapering in the vertical direction only needs to be introduced near the
termination point. Reduced size in both directions will efficiently force the optical mode into the lower waveguide. This geometry is generally effective, in a variety of material systems such as III-V compounds and silicon-on-insulator (SOI).

[0011] Accordingly, in one aspect, there is provided a method of fabricating a three-dimensional taper on an optical component, the method comprising the steps of: forming a lower waveguide in a substrate, covering the lower waveguide with a thin etch-stop layer, covering the etch-stop layer with an upper waveguide, etching the etch-stop layer to make a layered wedge, and etching the etch-stop layer and the upper waveguide vertically and laterally into the wedge.

[0012] According to another aspect, there is provided a precursor for a three-dimensional tapered waveguide, comprising a wedge-shaped body of waveguide material, a layer of sacrificial material on said wedge-shaped body, and a thin layer under tensile stress forming a hard mask on said sacrificial material.

In a still further aspect there is provided a method of fabricating a tapered waveguide structure, comprising the steps of providing a wedge-shaped body of waveguide material; forming a sacrificial layer on said wedge-shaped body; providing a non-etchable hard mask on said sacrificial layer, said non-etchable mask being under tensile stress; and providing an etching environment for said wedge-shaped body and said sacrificial layer so that as etching proceeds, said non-etchable mask becomes undercut and peels back under said tensile stress to leave a vertical taper on said wedge-shaped body.

The hard mask is preferably a metal such as aluminum, or other suitable metal that can be deposited on the silicon diode layer in tensile stress.

[0013] Other aspects and advantages of embodiments of the invention will be readily apparent to those ordinarily skilled in the art upon review of the following description.
Brief Description of the Drawings

[0014] The invention will now be described in more detail, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 illustrates a two-portion three-dimensional taper structure in accordance with one embodiment of the invention;

Figure 2 is a schematic view of a first etching step for obtaining a vertical taper near the termination end of the upper waveguide according to an embodiment of the present invention;

Figure 3 is a schematic view of a second etching step for obtaining a vertical taper near the termination end of the upper waveguide according to an embodiment of the present invention;

Figure 4 is a schematic view of a third etching step for obtaining a vertical taper near the termination end of the upper waveguide according to an embodiment of the present invention;

Figure 5 is a schematic view of a fourth etching step for obtaining a vertical taper near the termination end of the upper waveguide according to an embodiment of the present invention;

Figure 6 is a schematic view of a fifth etching step for obtaining a vertical taper near the termination end of the upper waveguide according to an embodiment of the present invention;

Figure 7 illustrates a cross-sectional view of a two-layer taper structure; and Figure 8 illustrates a top schematic view illustrating how a blunt termination can be sharpened through the oxidation of silicon.

[0015] This invention will now be described in detail with respect to certain specific representative embodiments thereof, the materials, apparatus and process steps being understood as examples that are intended to be illustrative only. In particular, the invention is not intended to be limited to the methods, materials, conditions, process parameters, apparatus and the like specifically recited herein.
Detailed Description of the Preferred Embodiments

[0016] The present invention is directed toward a waveguide with a designed mode profile that is capable of being efficiently coupled into an optical fiber. The device achieves two dimensional expansion or contraction of the output optical mode of single-transverse-mode semiconductor waveguide modulators and lasers.

[0017] Figure 1 illustrates a fully processed semiconductor. The device 10 may be a semiconductor structure or other active medium device where light propagates through a tapered section 14.

[0018] Figures 2 to 6 illustrate the steps according to one method for achieving an upper vertical taper. The method is described as follows in an example of SOI-based structure. The structure is first patterned with a thin layer of a suitable metal, such as aluminum, copper, or gold, a layer of sacrificial material, and a thick layer of silicon (Si). The metal is under tensile stress and the sacrificial layer etches substantially faster than the silicon. Silicon dioxide is a candidate for such a sacrificial layer. The layered wedge is then placed in a chemical etching environment. For example, common etching gas chemistries include use of an O₂-free, Ar, CHF₃, and optional CF₄ gas mixture, an O₂-free, fluorine-containing and nitrogen gas mixture, a CF₄ and CO gas mixture, an O₂, CF₄ and CH₄ gas mixture, and freon and neon gas mixtures. A further discussion of such processes can be found, for example, in B. Kim et al., J. Vac. Sci. Technol. A17, 2593, 1999; A. K. Dutta, Proceedings of International Symposium on Surfaces and Thin Films of Electronic Materials, 30, 169, 1995; M. V. Bazylenko and M. Gross, J. Vac. Sci Technol. A14, 2994, 1996; and Ph Nussbaum et a., Proceedings of the SPIE Conference on Micromachine Technology for Diffractive and Holographic Optics, Santa Clara, California, vol. 3879, 63 (1999).

[0019] The sacrificial layer and Si are etched both vertically and laterally into the wedge. The etchant attacks both the silicon and silicon dioxide isotropically.
Since the sacrificial layer etches faster than the silicon, the metal mask quickly becomes undercut; therefore, the metal mask is gradually freed and peels back under its own tensile stress, exposing more of the sacrificial layer and the underlying silicon to the etch reactants. This process continues down the length of the taper, with the silicon beneath the metal etching on a vertical slant as it is progressively exposed, forming a vertical taper near the termination end.

Referring to Figure 7, although the concept of a two-layer taper structure is generally applicable, it is described in the following through an example of SOI based structure. A lower waveguide is first formed in the single crystalline Si layer on a SOI substrate (called lower waveguide layer). The surface is covered with a thin etch-stop layer, and in this case it may be chosen as a dielectric layer (Si dioxide or nitride). Epitaxially grown SiGe layer is another possibility. In the selected etch chemistry, the upper layer would etch much faster than the etch-stop layer. The etch stop layer is designed to be sufficiently thin, so it is effectively 'invisible' to the optical modes. Finally the surface is covered by a thick optically transparent layer (called upper waveguide layer), and in this case it may be amorphous silicon (a-Si) or poly-crystalline silicon (poly-Si). The upper taper is formed in the upper layer by etching down to the dielectric etch-stop layer. SF₆ based chemistry may be used, which has high etch selectivity between silicon and oxide/nitride. Small variations in the etch rate of the upper layer or surface roughness will not be transferred into the lower layer. Process tolerance is therefore greatly improved. Since the required taper length is relatively short (on the order of 200 μm), slightly increased absorption in the a-Si or poly-Si materials is acceptable.

Referring to Figure 8, in order to achieve well-defined 'point' termination in the upper waveguide of a two-portion taper structure, high-resolution (such as electron-beam) lithography has traditionally been used. However, this is not suitable for volume production. Embodiments of the present invention form a two-portion taper with optical lithography, which is readily
available in semiconductor manufacturing and easily has a resolution near or below 1 μm. Then the structure undergoes thermal oxidation, which consumes Si from all exposed surfaces. Oxidation process for moderate to large oxide thickness is diffusion controlled. The oxidation rate decreases with the thickness of the oxide present on the surface. The width of the upper waveguide near termination point is designed to reduce gently, to ensure that after a certain thickness of oxide is formed, the oxidation primarily takes place from the two sides, as indicated in Fig. 4. The oxide thickness can be so chosen that the termination forms a 'point'. This method is fully compatible with VLSI manufacturing. The different oxidation rates between various crystal planes (e.g. the oxidation rate for (111) planes can be up to 50% higher than that for (100) planes) may also facilitate the formation of a 3-dimensional taper near the termination end.

[0022] Tapering in the vertical direction only needs to be introduced near the termination point. Reduced size in both directions will efficiently force the optical mode into the lower waveguide. This geometry is generally effective, in a variety of material systems such as III-V compounds and silicon-on-insulator (SOI).

[0023] Three-dimensional geometry provides more efficient coupling from the upper to the lower waveguide than previous designs. Two-layer taper with a sandwiched thin, optically 'invisible' etch-stop layer has relaxed constraints on processing controls. Oxidation for point termination eliminates the needs for high-resolution lithography, and makes the taper fabrication compatible with VLSI manufacturing.

[0024] Numerous modifications may be made without departing from the spirit and scope of the invention as defined in the appended claims.
What is claimed is:

1. An optical component employing a three-dimensional taper geometry.

2. An optical component as claimed in claim 1, wherein said taper geometry includes two portions with tapering in both the lateral and vertical direction.

3. An optical component as claimed in claim 2, wherein said component is a passive waveguide.

4. An optical component as claimed in claim 2, wherein said component is an active waveguide.

5. A precursor for a three-dimensional tapered waveguide, comprising a wedge-shaped body of waveguide material, a layer of sacrificial material on said wedge-shaped body, and a thin layer under tensile stress forming a hard mask on said sacrificial material.

6. A precursor as claimed in claim 5, wherein said hard mask is a metal.

7. A precursor as claimed in claim 6, wherein said hard mask is aluminum.

8. A precursor as claimed in any of claims 5 to 7, wherein said waveguide material is silicon and said sacrificial material is silicon dioxide.

9. A method of fabricating a three-dimensional taper on an optical component, the method comprising the steps of:
forming a lower waveguide in a substrate;
covering the lower waveguide with a thin etch-stop layer;
covering the etch-stop layer with an upper waveguide;
etching the etch-stop layer to make a layered wedge; and
etching the etch-stop layer and the upper waveguide vertically and laterally into the wedge.

10. A method of fabricating a tapered waveguide structure, comprising the steps of:
    providing a wedge-shaped body of waveguide material;
    forming a sacrificial layer on said wedge-shaped body;
    providing a non-etchable hard mask on said sacrificial layer, said non-etchable mask being under tensile stress; and
    providing an etching environment for said wedge-shaped body and said sacrificial layer so that as etching proceeds, said non-etchable mask becomes undercut and peels back under said tensile stress to leave a vertical taper on said wedge-shaped body.

11. A method as claimed in claim 10, wherein said non-etchable hard mask is metal.

12. A method as claimed in claim 11, wherein said waveguide material is silicon and said sacrificial layer is silicon dioxide.

13. A method as claimed in any one of claims 9 to 12, wherein said etching environment is a chemical etching environment.
14. A method as claimed in claim 13, wherein said etchant is \( \text{C}_4\text{H}_8 \).

15. A method of fabricating a tapered waveguide structure, comprising the steps of:
   - forming a lower waveguide on a substrate;
   - covering said lower waveguide with an etch stop layer;
   - forming an upper waveguide layer on said etch stop layer;
   - masking said upper layer to define a wedge-shaped form; and
   - etching said upper layer down to said etch stop layer to form a wedge-shaped waveguide.

16. A method as claimed in claim 15, further comprising oxidizing the walls of said wedge-shaped waveguide.

17. A method as claimed in claim 16, wherein said upper waveguide is selected from the group consisting of amorphous silicon and polycrystalline silicon.