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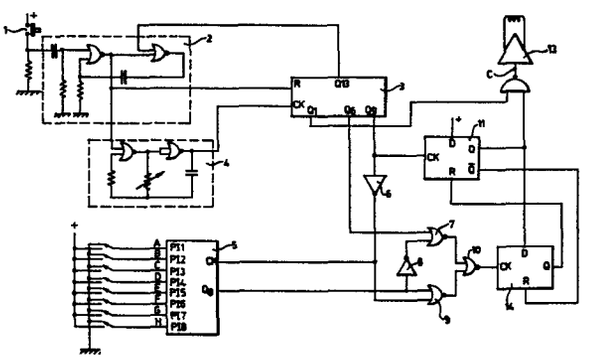
(54) Programmer for implanted pacer.

(57) A plurality of programming bits are placed into a parallel in-serially out register (5). When the programmer is activated, a monostable (2) resets a counter (3), and energizes an oscillator (4) which clocks the counter. Three subintervals from the counter are utilized for pulse width modulation of the programming signals. Once for each bit, the output is energized and begins transmitting pulses at the lowest subinterval rate. Depending upon the logic state of each bit, the transmission pulse is terminated either at the second or the third subinterval time.



EP 0 000 986 A1

"Programmer for Implanted Pacer"

Field of the Invention

This invention relates to an apparatus for transmitting a preselected signal comprising a sequence of signal bits of different values. Such an apparatus can be termed a programmable transmitter where the signal it is desired to transmit to a receiver may be selected, or set, prior to transmission. The invention is especially concerned with programmable transmitters for enabling programming signals to be transmitted to, and received by, implanted, programmable body function control apparatus such as cardiac pacemakers.

Background Art

Pacemakers for generating artificial stimulating pulses for the heart, and which may be implanted in the body, are well known. Originally the electrical circuitry for such pacemakers was of analog design, but in recent years digital circuitry has been also employed. A digital approach to pacemakers has led to the evolution of programmable pacemakers - pacemakers having parameters such as pulse rates which are adjustable (programmable) once the pacemaker has been implanted. Programmable pacemakers are described in, for instance, British Specifications 1,385,954 and 1,398,875. Such pacemakers have circuitry to detect and decode signals transmitted outside the body and alter the program accordingly. In British Specification 1,385,954 (claiming priority based on U.S.S.N. 141694, in turn a parent of U.S.P.N. 3,805,796 to Tenz) the programming is accomplished by means

of a magnetic field which is sensed by a magnetic reed switch; the opening and closing of the switch provides programming pulses to a program store. In British Specification 1,398,875 (based on U.S.P.N. 3,833,005 to Wingrove) the programming is by means of radio frequency transmission and reception.

Although much attention has been paid to the development of the implantable programmable pacemaker, there is also a need for an external programmable transmitter which can be programmed with the pacemaker program and this program then accurately transmitted to the implanted pacemaker.

We have now developed a programmable transmitter for such use.

Disclosure of Invention

According to the invention we provide an external programmer for supplying a fixed number of pulse-width modulated signal bits as a program to an implanted, programmable body function control apparatus which comprises means for preselecting and storing a fixed number of signal bits in a code representative of the program to be supplied to said implanted apparatus and for supplying said code as an output of said means when actuated, counter means for actuating the said code output, means for actuating the counter, and means responsive to said code output for transmitting said program to said implanted apparatus as a sequence of a said fixed number of pulse-width modulated signal bits.

Brief Description of the Drawing

Preferred features of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows schematically the electrical circuit diagram of an external programmer for encoding an 8-bit program, and for transmitting the program to an implanted, programmable cardiac pacemaker,

Figure 2 is a timing diagram for use with Figure 1, and

Figure 3 shows schematically the electrical circuit diagram of an alternative embodiment.

Best Mode of Carrying Out the Invention

The illustrated programmer is designed to transmit an 8-bit tone burst modulated program, that is, an 8-bit pulse width modulated signal where a sine wave carrier frequency is pulse width modulated by each of the 8 data bits.

Referring to Figure 1, the programmer comprises a "press-to-program" switch 1 tied between the positive supply rail and earth. The switch output drives a monostable 2. The monostable 2 is employed to reset a 13 stage counter 3, and to control an oscillator 4. The oscillator 4 includes an "oscillator disable" NOR gate 16 on its input side which, when supplied with a high input from monostable 2, provides a low output which disables the oscillator output to a clock input of counter 3.

Only the Q1, Q6, Q9, and Q13 stages of counter 3 are employed. Stage Q9 is employed to clock a parallel in/serial out eight bit shift register 5 via an inverter 6. The eight parallel inputs for shift register 5 (PI 1 to 8) are labelled A to H and the values of such inputs are set by eight switches which individually can be connected to the positive supply rail or to earth.

The outputs from the Q6 stage of counter 3, inverter 6, and the serial output Q8 of shift register 5 drive a pulse sterring network composed of NOR gates 7. 9, and 10 and inverter 8.

The Q9 stage of counter 3 also clocks a D-type flip-flop 11 whose D-input is tied to the positive supply rail. The Q output of flip-flop 11 is supplied to one input of a NAND gate 12, whose second input is supplied by the Q1 stage of counter 3. NAND gate 12 drives an amplifier/transmitter 13, outputs from which are transmitted into the body for receipt by an implanted cardiac pacemaker where the received pulses are decoded and employed for changing the program stored in the pacemaker.

The output of NOR gate 10 clocks a further D-type flip-flop 14, whose D-input and reset are driven by the Q

and $\bar{Q}$ outputs, respectively, of flip-flop 11. The Q output of flip-flop 14 is employed to reset flip-flop 11.

The operation of the programmer will now be described generally and then in detail with reference also to the timing diagram of Figure 2, which illustrates the pulses at positions indicated on Figure 1.

The pacemaker program transmitted by amplifier/transmitter 13 consists of an eight bit pulse-width modulated signal wherein each pulse is itself several cycles of a sine wave carrier frequency. The pulses of short bit length (which might represent "0" in the pacemaker program) and long bit length ("1") are determined by the signal supplied to NAND gate 12 from flip-flop 11 and are initially generated by the values selected by the settings of the eight switches on the inputs A to H of shift register 5. The carrier frequency present in each pulse is derived from the rapid transitions made by the Q1 stage of counter 3, as supplied to the second input of NAND gate 12. The output of NAND gate 12 is thus the square wave carrier frequency from Q1 modulated by the long or short bit lengths determined by the switching times of flip-flop 11. After passage through amplifier/transmitter 13, this output becomes the tone burst modulated signal described above.

Referring to the operation in more detail, with the press-to-program switch normally open, the monostable 2 output remains high maintaining a reset on counter 3 and disabling oscillator 4.

When it is desired to change the 8-bit program stored in the implanted pacemaker, the values of the 8-bits are selected by providing an appropriate combination of values through opening or closing each of the eight switches on the inputs to shift register 5. In the example given, referring to Figure 2, the inputs H, G, D, and B are tied to the positive supply rail whereas inputs F, E, C, and A are earthed. This will provide, as to be described, for transmission by amplifier/transmitter 13, the program

00110101 where "0" represents a pulse of short length (and "1" of long length), it being appreciated that the values are transmitted in the sequence HGFEDCBA. This arises since the first value appearing at the Q8 output of shift register 5 is the value of the PI 8 input (H).

To transmit the selected program, the press-to-program switch 1 is depressed. This causes monostable 2 to fire (i.e. causing its output to go low), thus removing the reset from counter 3 and allowing oscillator 4 to commence running at a period T_0 determined by its timing components. Counter 3 will increment by 1 count on every negative clock edge provided by oscillator 4.

At a count of Q9, flip-flop 11 clocks the level of its D-input to its Q output, putting Q "high" and $\bar{Q}$ "low". This removes the reset on flip-flop 14 and places its D-input "high". The "high" output of Q is also applied to NAND gate 12 to commence transmission of the first bit in the 8-bit sequence of data. The next positive edge on the clock input of flip-flop 14 will clock its Q output to "high", thus resetting flip-flop 11. The reset of the latter will, in turn, reset flip-flop 14, causing its Q output to go "low" and terminate transmission of the first bit in the 8-bit sequence.

The time at which flip-flop 14 clocks a "high" to its Q output determines the width of the flip-flop 11 Q output and hence the pulse width of the modulation at point C in Figure 1. It is dependent upon the state of the steering network comprising components 7, 8, 9, and 10. The level on the Q8 output of shift register 5 determines whether the clock pulse for flip-flop 14 arises via NOR gate 7 or 9 and is derived from either the Q6 or Q9 stage of counter 3. With gate 7 enabled, the first positive edge on the flip-flop 14 clock input occurs at $32T_0$ from the time the flip-flop 11 Q output went "high". With gate 9 enabled, this first positive edge occurs at $256T_0$ from the time the flip-flop 11 Q output went "high".

Initially, the Q8 output of shift register 5 represents

the value at its H input ("high") and this causes the pulse supplied by flip-flop 11 to NAND gate 12 to be cut off after $32T_0$ (i.e. causing a short pulse representing "0" to be transmitted).

Subsequent bits are then transmitted as the values of the seven remaining shift register stages are sequentially clocked to the Q8 output of shift register 5. The bits are transmitted at each positive transition of the Q9 stage of counter 3 until Q13 is reached. Shift register 5 is clocked on each negative edge of the Q9 stage of counter 3. When the Q13 stage of counter 3 goes high this resets monostable 2 to its initial condition, resets counter 3 and disables the oscillator 4. By this time the values of all eight stages of shift register 5 will have appeared at the Q8 output and the corresponding 8-bits will have been transmitted by amplifier/transmitter 13.

In a typical programmer constructed as described, T_0 was set to 0.05 ms: this provided short pulses of 1.6 ms in width and long pulses of 12.8 ms in width. These pulses were each modulated via the Q1 stage of counter 3 at 10 KHz.

The alternative embodiment shown in Figure 3 will now be described.

Referring to Figure 3, the programmer again comprises a "press-to-program" switch 1 tied between the electrical supply rails. The switch output drives a monostable 2. The monostable 2 is employed to reset a 13 stage counter 3 to control an oscillator 4, and to reset a decade counter 15. The oscillator 4 includes an "oscillator disable" NOR gate 16 which, when supplied with a high input from monostable 2, provides a low output which disables the oscillator output to a clock input of counter 3.

The Q7, 8 and 9 output stages of counter 3 are combined through a NAND gate 17 and a NOR gate 18 to provide a "short" output pulse to a transmission gate 19. The Q9 output stage of counter 3 provides a "long" output pulse to a transmission gate 20 and, through inverter 21, to the clock input of the decade counter 15.

A NAND gate 22 receives the Q1 output of counter 3 and also the outputs of transmission gates 19 and 20. The output of NAND gate 22 drives an amplifier/transmitter 23, output pulses from which are transmitted into the body for receipt by an implanted programmable cardiac pacemaker where the received pulses are decoded and employed for changing the program stored in the pacemaker.

The Q13 output of counter 3 is supplied to a disable input of monostable 2.

The decade counter 15 has eight output stages (0 to 7) which are successively employed to control (turn on and off) eight transmission gates which, in this embodiment, take the form of two quad/bilateral switches 24. The eight gates formed by the switches 24 each receive an input from a selector switch 25. The switches 25 ("A" to "H") can be individually connected to the positive supply rail or to earth. The eight outputs of the switches 24 are coupled together to provide a common bus 26 which is employed to control transmission gate 20 and (via inverter 27) transmission gate 19.

The operation of the programmer will now be described first generally and then in more detail.

The counts which are supplied by counter 3 to transmission gates 19 and 20 supply pulses representative of short bit lengths (e.g. "0") and long bit lengths (e.g. "1"). The eight bit program desired is selected by setting the switches 25 appropriately and these values are sequentially clocked onto the common bus 26 to open either transmission gate 19 or 20 depending upon the logic value supplied on bus 26. The short or long pulse supplied to the amplifier/transmitter 23 from the opened transmission gate 9 or 10 is employed to modulate the higher frequency count supplied to NAND gate 22 from the Q1 stage of counter 3 so that the output of the amplifier/transmitter is an eight-bit tone burst signal.

Referring to the operation in more detail, with the press to program switch 1 normally open, the monostable 2

output remains high, maintaining a reset on counters 3 and 5 and disabling oscillator 4. No output is provided to amplifier/transmitter 23. When it is desired to change the 8-bit program stored in the implanted pacemaker, the values of the 8-bits are selected by providing an appropriate combination of values through opening or closing each of the switches 25. The press to program switch 1 is then pressed. Pressing, i.e. closing, switch 1 causes monostable 2 to fire (i.e. causing its output to go low), thus removing the reset from the counters 3 and 5 and allowing oscillator 4 to commence running. The removal of the reset to decade counter 15 leaves a count at its "zero" stage, which opens the transmission gate in switches 24 corresponding to switch 25 "A". The output of switch 25 "A" is supplied on common bus 26 and depending on its logic value, opens either transmission gate 19 or 20 thus to supply either a short pulse or a long pulse to NAND gate 22. This short or long pulse modulates the high frequency output of the Q1 stage of counter 3, and is amplified and transmitted by amplifier/transmitter 13.

As soon as the Q9 stage of counter 3 falls, decade counter 15 is incremented by one so that the count, now at its "one" stage, causes the output value supplied by switch 25 "B" rather than 25 "A" to control which of the transmission gates 19 and 20 is opened. The short or long pulse (modulating the Q1 high frequency output as before) is again transmitted by amplifier/transmitter 23.

This cycle repeats for each of the eight switches 25 so that a total of eight tone burst modulated pulses, of either short or long width, is transmitted. Once the eighth pulse has been transmitted, the Q13 stage of counter 3 is then reached to disable monostable 2. This causes the latter to revert to its stable state, which reintroduces a reset to counters 3 and 15 and disables oscillator 4. No further information is hence transmitted until the press to program switch 1 is once again depressed, when the whole cycle would then repeat.

Typically, the oscillator has a 20 KHz frequency. This provides a 10 KHz output at the Q1 stage of counter 3, a pulse length of 3.2 ms to transmission gate 19 (a"short" pulse), a pulse length of 12.8 ms to transmission gate 20 (a "long" pulse), and a data rate for clocking decade counter 15 of 25.6 ms. The NAND gate 22 thus transmits to amplifier/transmitter 23 eight bits, either of 3.2 ms or 12.8 ms in width and each including a 10 KHz square wave carrier.

What is claimed is:

1. An external programmer for supplying a fixed number of signal bits as a program for varying given operational functions of an implanted, programmable body function apparatus comprising:

register means for preselecting and storing a fixed number of signal bits, said bits being in coded representation of the program to be supplied serially to said implanted apparatus;

means for generating a pulse signal at a predetermined frequency;

counter means, responsive to said means for generating, for providing digital control states at three subintervals of a datum count;

output means for transmitting signals from said programmer to said implanted apparatus;

means, responsive to said counter, for periodically enabling said output means to transmit signals at the rate of the smallest of said subintervals, the periodicity of said means for enabling corresponding to said fixed number of fractional parts of said datum count period;

logic means, responsive to said counter means and to said register means, for disabling said output means, once for each said periodic enabling, at a time after each enabling, said times successively corresponding to the logical state of each associated successive one of said signal bits.

2. A programmer as described in claim 1 wherein said logic means comprises means, responsive to each occurrence of a given logic bit in said register means, for disabling said output means upon the occurrence of the intermediate one of said subintervals; and means, responsive to each occurrence of an opposite logic bit in said register means, for disabling said output means upon the occurrence of the third of said subintervals.

3. A programmer according to claim 2 wherein said logic means comprises at least two transmission gates, said counter means supplying inputs to said gates and the outputs supplied to said transmitter by said gates being controlled by said code output.

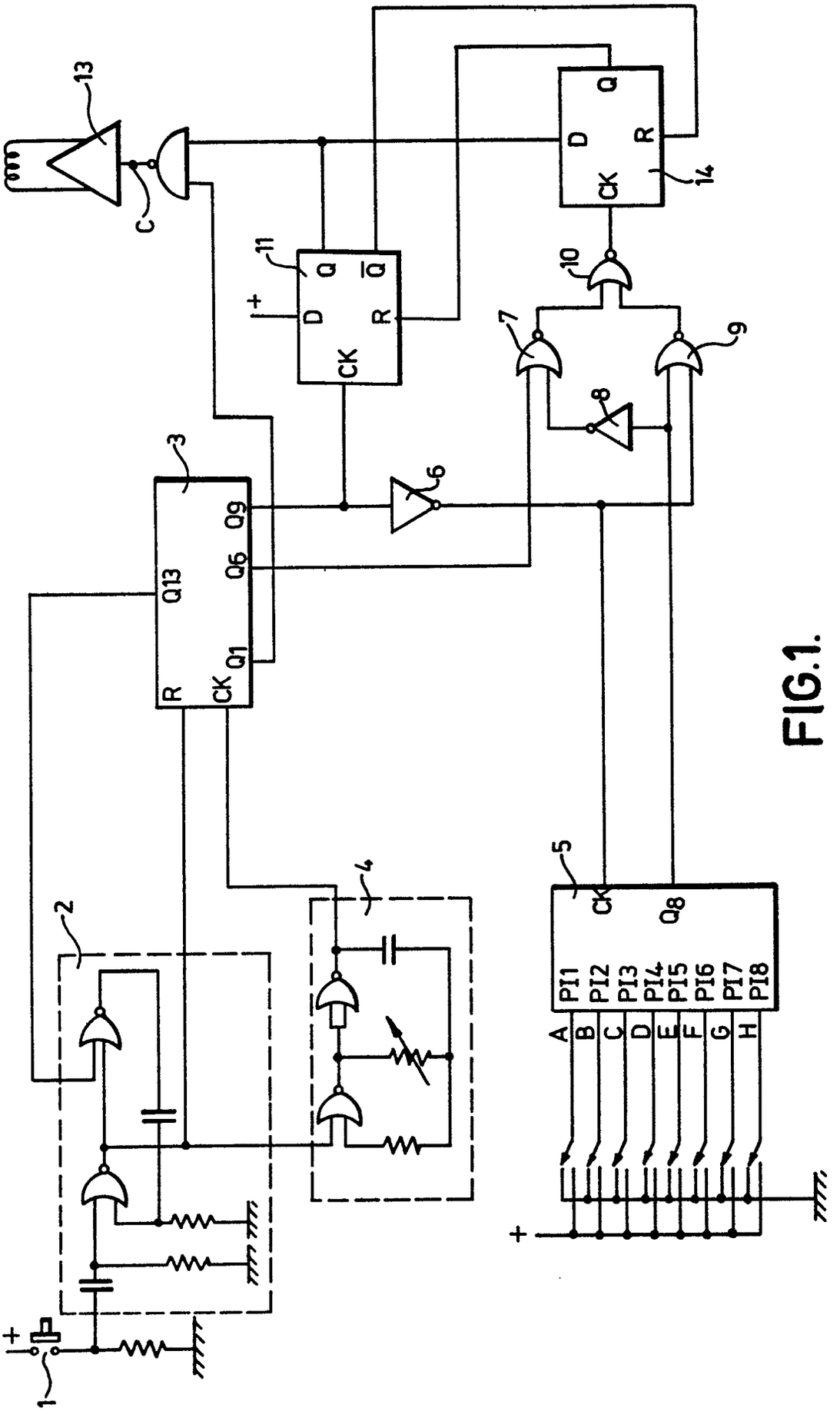
4. A programmer according to claim 3 wherein said means for enabling comprises a first flip-flop for controlling the time of commencement of transmission of any signal bit, and said logic means further comprises a second flip-flop for controlling the time of termination of transmission of any signal bit.

5. A programmer as described in claim 1 wherein said means for generating comprises:

programmer activating switch means;

monostable means, energized by said switch means, for resetting said counter and for defining a time limit for said datum count; and

oscillator means, enabled by said monostable means, for clocking said counter, thereby further establishing the periodicity of said smallest subintervals.


13
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D
Q
$\overline{Q}$
R
CK
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7
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8
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Q13
Q9
Q6
Q1
R
CK
6
2
4
5
CK
Q8
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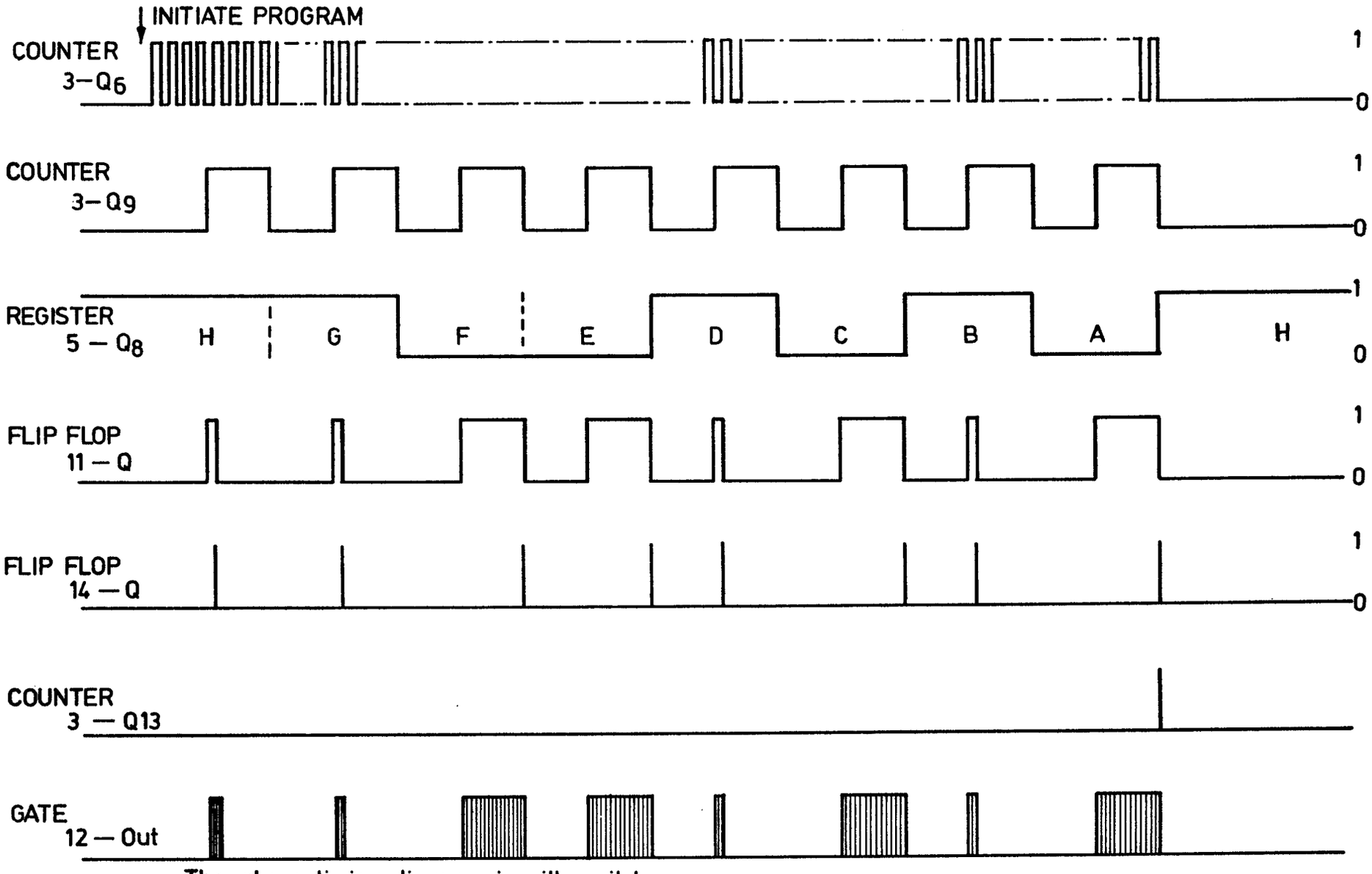
FIG.1.



The above timing diagram is with switches
A= –, B= +, C= –, D= +, E= –, F= –, G= +, H= +

FIG.2.

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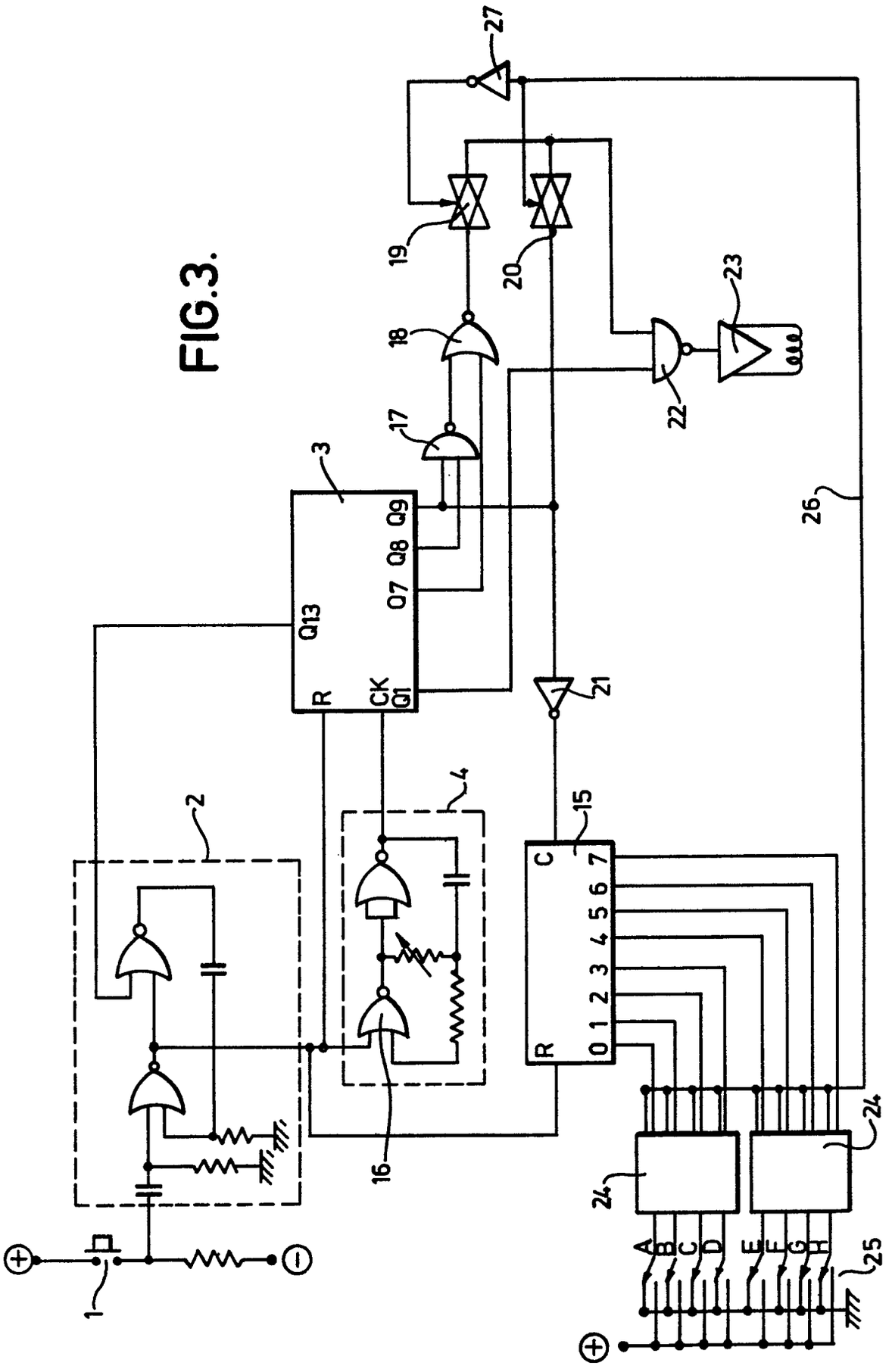
FIG.3.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EUROPEAN SEARCH REPORT

0000986
Application number

EP 78 30 0240

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int. Cl.²)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
	US - A - 3 906 348 (WILLMOTT) * Column 1, lines 60-67; column 2, line 6 - column 3, line 46 * --	1-3,5	A 61 N 1/36 G 08 C 19/22
	LU - A - 76 880 (ARCO) & US - A - 4 049 004 * Page 37, paragraphs 2 and 3; page 40, paragraphs 2 and 4; page 41, paragraph 1; page 43, paragraph 2; page 44; page 45; page 46, paragraphs 1 and 3 * --	1	TECHNICAL FIELDS SEARCHED (Int.Cl.²)
	US - A - 4 024 875 (MEDTRONIC) * Column 3, lines 34-64; column 4, lines 44-57; column 7, line 63 - column 8, line 3 * ----	1,5	A 61 N 1/36 G 08 C 19/22 A 61 N 1/08

CATEGORY OF CITED DOCUMENTS

X: particularly relevant
A: technological background
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E: conflicting application
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L: citation for other reasons

&: member of the same patent family, corresponding document

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	27-11-1978	SIMON

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