



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(21) International Application Number: PCT/GB90/01841 (22) International Filing Date: 27 November 1990 (27.11.90) (30) Priority data: 8927281.9 1 December 1989 (01.12.89) GB (71) Applicant (for all designated States except US): UNIVERSITY OF STRATHCLYDE [GB/GB]; McCance Building, 16 Richmond Street, Glasgow G1 1XQ (GB). (72) Inventors; and (75) Inventors/Applicants (for US only): MILNE, George, Johnstone [GB/GB]; 8 Carlaverock Road, Newlands, Glasgow G43 2SA (GB). COCKSHOT, William, Paul [GB/GB]; 115 Albert Road, Glasgow G42 8UB (GB).		(74) Agents: MacDOUGALL, Donald, Carmichael et al.; Cruikshank & Fairweather, 19 Royal Exchange Square, Glasgow G1 3AE (GB). (81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB (European patent), GR (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent), US. Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>
(54) Title: METHOD AND APPARATUS FOR SIMULATION OF A PHYSICAL PROCESS		
(57) Abstract In the simulation of a spatially-extended physical process the complete spatial extent of which is defined by a multiplicity of parameters (A), each parameter (A) is represented with a multi-state distinguished sequential digital logic circuit (B) the possible states of which represent the possible states of the pertaining parameter (A). The interaction of each pair of parameters (A) is represented with an interconnection (C) between the pertaining circuits (B). Each logic circuit (B) is initially established in a known state and thereafter at least one circuit (B) is pulsed to cause evolution of the circuits (B) through some or all of their possible states. The states of certain circuits (B) are determined intermittently as a measure of the corresponding states of the parameters (A).		

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METHOD AND APPARATUS FOR SIMULATION
OF A PHYSICAL PROCESS

This invention relates to a method and apparatus for simulation of a spatially-extended physical process.

Simulation of spatially-extended physical processes is already well known and conventionally is implemented on a digital computer which has the ability of modelling the physical process, the complete spatial extent of which is defined by a multiplicity of parameters, utilising signal input/output devices, a logic unit and a memory unit. The memory unit has a first set of memory cells which contain values for the multiplicity of parameters and a second set of memory cells which store a logic unit instruction program. The logic unit is arranged to fetch first instructions from the second set of memory cells and to implement these first instructions on first selected parameter values retrieved from the first set of memory cells in order to compute new values for these parameters which are then returned to the first selected cells of the first set. This procedure is then repeated through second and subsequent instructions implemented on second and subsequent selected parameter values. Intermittently the logic unit recycles through the first, second and subsequent instructions to update the first, second and subsequent parameter values. The development of the physical process is thus simulated on a cyclic basis with each cycle containing a plurality of sequential steps each operating on a selection of parameter values. Each selection is limited by the number of binary bits of information that can be transmitted simultaneously between the logic unit and the memory unit on the conductors interconnecting these units and as a practical matter these conductors are limited in

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number being substantially fewer than the number of parameters in the multiplicity defining the physical process. Accordingly, the speed of operation of the known simulation method and apparatus is limited and the multiplicity of parameter values cannot be updated simultaneously.

It is an object of the present invention to provide a new and improved method and apparatus for simulating a physical process.

According to the present invention there is provided a method of simulating a spatially-extended physical process, the complete spatial extent of which is defined by a multiplicity of parameters, the method comprising representing each parameter with a multi-state distinguished sequential digital logic circuit the possible states of which represent the possible states of the pertaining parameter, representing the interaction of each pair of parameters with an interconnection between the pertaining multi-state distinguished sequential digital logic circuits, initially establishing each logic circuit in a known state, pulsing at least one of the multi-state distinguished sequential digital logic circuits in the array to cause circuits of the array to evolve through at least some of their possible states, and intermittently determining the states of at least some of the circuits of the array as a measure of the corresponding states of the parameters of the physical process.

The pulsing step may be implemented by an external pulse signal applied to all of the circuits of the array or by an internal pulse signal generated by one or more of the circuits of the array and applied to less than all of the circuits of the array.

In another aspect the present invention provides apparatus for simulating a spatially-extended physical process the complete spatial extent of which is defined by a

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multiplicity of parameters, the apparatus comprising a multiplicity of multi-state sequential digital logic circuits each distinguished to represent a respective one of the multiplicity of parameters of the process so that the possible states of each said circuit represent the possible states of the pertaining parameter, means interconnecting at least those said circuits representing parameters having mutual interaction, means for initially establishing each logic circuit in a known state, means for pulsing at least one of said circuits to cause circuits of the array to evolve through at least some of their possible states, and means for intermittently determining the states of at least some of said circuits to provide a measure of the corresponding states of the parameters of the physical process.

By virtue of the present invention the value of each parameter can be updated simultaneously when the array is pulsed and can be repeatedly updated by applying repeated pulses which only require to be time separated sufficiently to accommodate signal propagation delays in the array. Accordingly, simulation of the development of the spatially-extended physical process is much faster than hitherto arising out of the absence of a memory unit and fetch-and-carry steps associated therewith.

Preferably the apparatus comprises a multiplicity of universal sequential digital logic circuits each associated with means adapted to configure the pertaining circuit distinguished to represent a pertaining parameter as aforesaid. Conveniently the adaption means comprises a fixed logic circuit. Each universal sequential digital logic circuit and associated adaption means may be configured to represent a plurality of distinguished circuits.

Preferably the apparatus comprises a plurality of rectilinear circuit boards each containing a universal

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sequential digital logic circuit and associated adaption means as aforesaid, each board being interconnected to its neighbours via orthogonally disposed signal conductors emergent from each board edge. The emergent signal conductors may take the form of edge connectors or any other suitable form of connector. Conveniently said signal conductors comprise a first conductor set interconnecting the universal sequential digital logic circuits of adjacent boards, and a second conductor set interconnecting the adaption means (fixed logic circuits) of adjacent boards.

Preferably also, said initially establishing means is formed by said fixed logic circuits, the interconnection thereof with the pertaining universal sequential digital logic circuit, signals conducted by the second conductor set, and synchronisation or reset signals delivered to the fixed logic circuits from a central synchronisation unit.

Preferably also, on each board neighbouring sequential digital logic circuits are interconnected via orthogonally disposed signal pathways forming on-board extensions of said orthogonally disposed signal conductors, said pathways comprising selectively-operable switches the settings of which define the presence or absence of an interconnection between adjacent distinguished sequential digital logic circuits.

An embodiment of the present invention will now be described by way of example with reference to the accompanying drawings, in which:-

Fig. 1 schematically illustrates apparatus for simulating a spatially-extended physical process;

Fig. 2 illustrates one circuit of the Fig. 1 apparatus;

Fig. 3 illustrates interconnection of a pair of Fig. 2 circuits;

Fig. 4 illustrates an array of interconnected Fig. 2 circuits;

Fig. 5 illustrates one practical implementation of the

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Fig. 2 circuit;

Fig. 6 illustrates an array of interconnected Fig. 5 boards;

Fig. 7 illustrates a specific form of sequential circuits adapted to model a specific process; and

Fig. 8 illustrates the edge interconnection of boards incorporating the Fig. 7 circuits.

The embodiment which will now be described is particularly suitable for simulating a two-dimensional spatially extended physical process such as the flow of a thin slice of fluid, or the evolution of a two-dimensional slice of a solid or the behaviour of an electronic circuit chip, but is not limited in application to two-dimensional processes. Such a spatially-extended process is diagrammatically shown by numeral 10 in Fig. 1 and comprises a plurality of areas A of which only two are shown, each area A being defined by parameters of the process 10. Fig. 1 also illustrates apparatus 12 for simulating the process 10 as comprising input/output devices 13 and a simulation surface 14, the latter being formed by sequential logic circuits B which are organised respectively to represent areas A as denoted by lines 11 such that the possible states of a circuit B conceptually represent the states of the parameters of the pertaining area A.

By way of example one circuit B is shown in Fig. 2 as comprising four logic cells L interconnected by signal pathways incorporating eight switches S each capable of being set either in open or closed condition for the purpose of rendering the particular circuit B distinguished so as to represent a particular area A of the process 10. The Fig. 2 circuit B has four conductors C which emerge from circuit B to enable interconnection with one or more adjoining circuits B via selectively-operable switches 16 as schematically illustrated in Fig. 3 for the purpose of representing interaction of the parameters of the

corresponding areas A of the process 10. A plurality of the circuits B with interconnecting switches 16 are preferably implemented by a single circuit block B1, described with reference to Fig. 5 and the complete simulation surface 14 is formed of a set of interconnected circuit blocks B1 as shown in Fig. 4 each circuit block B1 having had its circuits B set to a predetermined state by a distinguished set of reset signals 17 from the input/output device 13. Clock pulses 18 externally provided (in this case) to the surface 14 then cause the circuits B to evolve through a series of states corresponding to development of the process 10. The developing values of the parameters of the process 10 are represented by signals appearing on conductors 19 emergent from each circuit block B1 and which form part of input/output device 13.

Each circuit block B1 is preferably implemented, as shown in Fig. 5, by a variable logic block 20 in association with a fixed logic block 22, these blocks 20, 22 being interconnected by a conductor set 24 mounted on a rectilinear circuit board 26. Variable logic block 20 is of universal configuration and is configured to the required sequential logic state or states so as to represent one or more circuits B by the fixed logic block 22. Board 26 is interconnected to its neighbours via orthogonally disposed signal conductors comprising a first conductor set 28 connected only to the variable logic block 20 and a second conductor set 30 connected only to the fixed logic block 22. Each set has a north, south, east and west conductor so that the number of such conductors on opposite sides of the board 26 is the same. External synchronisation or clock pulse signals 18, when provided, are delivered to the fixed logic block 22.

The surface 14 is thereafter formed as shown in Fig. 6 by a two-dimensional array of the boards 26 of Fig. 5 with each board 26 connected to its neighbours via conductor sets

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28, 30. All boards 26 other than those at the edges of the array have the same connector pattern and some or all edge boards are connected via conductor sets 28, 30 to the input/output device 13 (of Fig. 1). Each board 26 has a sync signal supplied to it from a central synchronisation unit 32.

By way of a specific example it is well known that two-dimensional gases can be modelled as a lattice of discrete points which are governed by deterministic transition rules as set forth in the article entitled "Lattice-Gas Automata for the Navier-Stokes Equation" by Frisch, Hasslacher & Pomeau published in Physical Review Letters Vol. 56, No. 14. The apparatus 12 can be applied to this spatially-extended modelling process by representing each point in the gas lattice with a sequential logic circuit 40 having six input 42 and six output wires 44 and by connecting adjacent logic circuits 40 via switches so that the inputs of one circuit go to the outputs of another circuit in a hexagonal lattice topology as shown in Fig.

7. Within each circuit 40 switches are set to establish an AND array accounting for the 64 different combinations of incoming particles (molecules) and an OR array to compute when an outgoing particle (molecule) is to be sent in each of 6 directions. The truth table (not shown) of the logic circuit encodes the rules for the lattice gas and D-type latches on the 6 output wires are clocked by a synchronisation signal so that the output pulses at each instant represent a delayed function of the input pulses of the previous clock period. At the edges of the boards the wires from the marginal sequential circuits 40 are sent to adjacent boards along the conductor set 28 (of Fig. 5) so that they connect to the appropriate inputs and outputs of circuits 40 on adjacent boards. This is shown in Fig. 8.

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CLAIMS

1. A method of simulating a spatially-extended physical process the complete spatial extent of which is defined by a multiplicity of parameters, comprising representing each parameter with a multi-state distinguished sequential digital logic circuit the possible states of which represent the possible states of the pertaining parameter, representing the interaction of each pair of parameters with an interconnection between the pertaining multi-state distinguished sequential digital logic circuits, initially establishing each logic circuit in a known state, pulsing at least one of the multi-state distinguished sequential digital logic circuits in the array to cause circuits of the array to evolve through at least some of their possible states, and intermittently determining the states of at least some of the circuits of the array as a measure of the corresponding states of the parameters of the physical process.

2. A method as claimed in claim 1, wherein the pulsing step is implemented by an external pulse signal applied to all of the circuits of the array.

3. A method as claimed in claim 1, wherein the pulsing step is implemented by an internal pulse signal generated by one or more of the circuits of the array and applied to less than all of the circuits of the array.

4. Apparatus for simulating a spatially-extended physical process (10) the complete spatial extent of which is defined by a multiplicity of parameters, the apparatus (12) comprising a multiplicity of multi-state sequential digital logic circuits B each distinguished S to represent a respective one of the multiplicity of parameters of the

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process (10) so that the possible states of each said circuit B represent the possible states of the pertaining parameter, means C, (16) interconnecting at least those said circuits B representing parameters having mutual interaction, means (13,17) for initially establishing each logic circuit B in a known state, means (18) for pulsing at least one of said circuits B to cause circuits B of the array to evolve through at least some of their possible states, and means (19,13) for intermittently determining the states of at least some of said circuits B to provide a measure of the corresponding states of the parameters of the physical process (10).

5. Apparatus as claimed in claim 4, comprising a multiplicity of universal sequential digital logic circuits (20) each associated with means (22) adapted to configure the pertaining circuit (20) distinguished to represent a pertaining parameter.

6. Apparatus as claimed in Claim 4, wherein each universal sequential digital logic circuit (20) and associated adaption means (22) is configured to represent a plurality of distinguished circuits B,S.

7. Apparatus as claimed in claim 5 or claim 6, wherein the adaption means (22) comprises a fixed logic circuit.

8. Apparatus as claimed in any one of claims 5 to 7, comprising a plurality of rectilinear circuit boards (26) each containing a universal sequential digital logic circuit (20) and associated adaption means (22), each board (26) being interconnected to its neighbours via orthogonally disposed signal conductors (28,30) emergent from each board edge.

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9. Apparatus as claimed in claim 8, wherein said signal conductors (28,30) comprise a first conductor set (28) interconnecting the universal sequential digital logic circuits (20) of adjacent boards (26), and a second conductor set (30) interconnecting the adaption means (28) of adjacent boards (26).

10. Apparatus as claimed in claim 9, wherein said initially establishing means is formed by said fixed logic circuits (22), the interconnection thereof with the pertaining universal sequential digital logic circuit (20), signals conducted by the second conductor set (30), and synchronisation or reset signals delivered to the fixed logic circuits (22) from a central synchronisation unit (32).

11. Apparatus as claimed in any one of claims 8-10, wherein on each board (26) neighbouring sequential digital logic circuits B are interconnected via orthogonally disposed signal pathways forming on-board extensions of said orthogonally disposed signal conductors (28,30), said pathways comprising selectively-operable switches S the settings of which define the presence or absence of an interconnection between adjacent distinguished sequential digital logic circuits B,S.

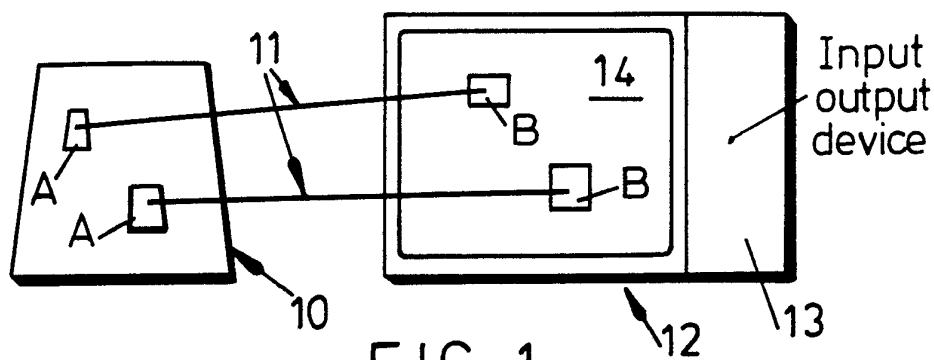


FIG. 1

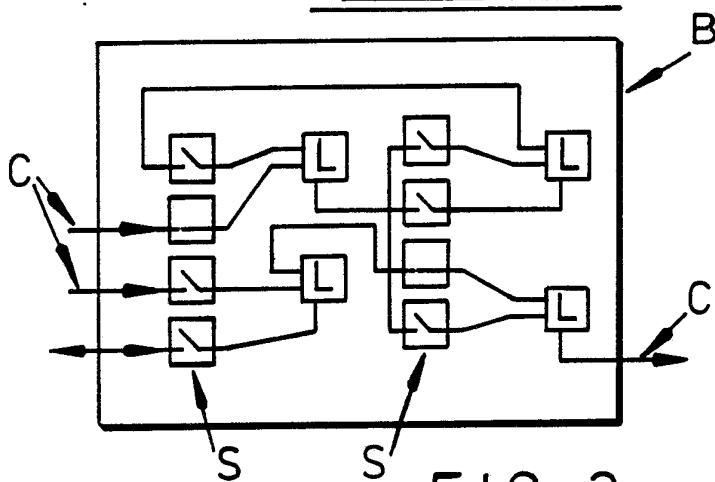


FIG. 2

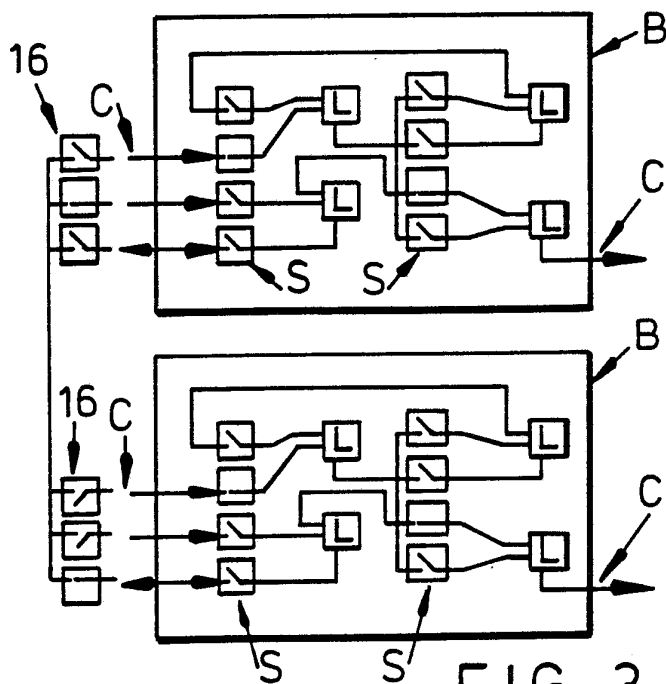
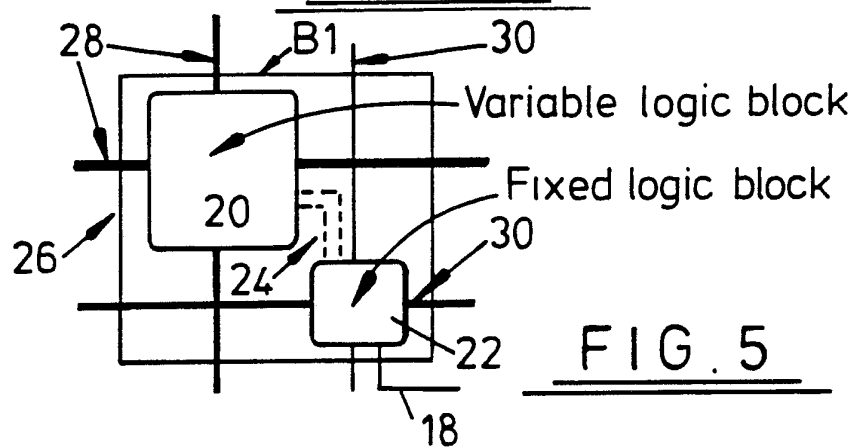
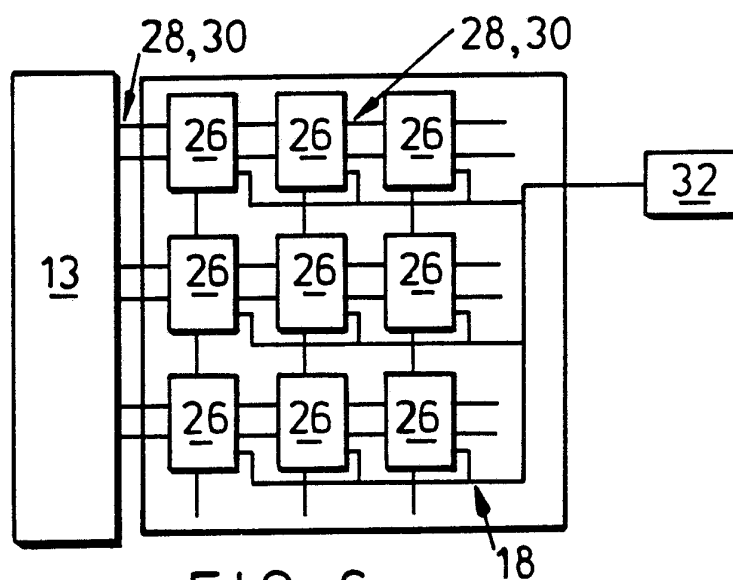
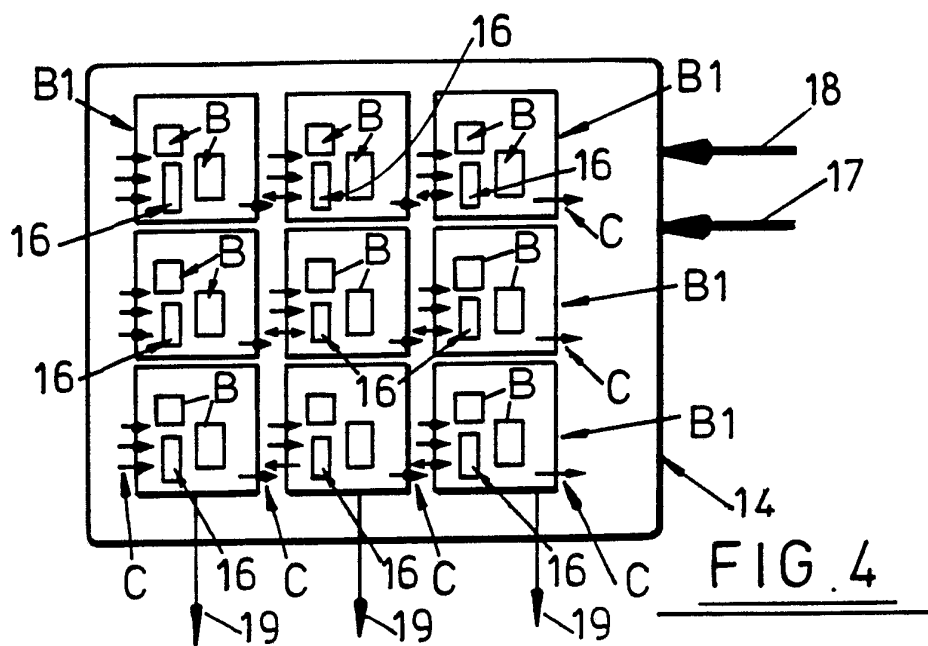
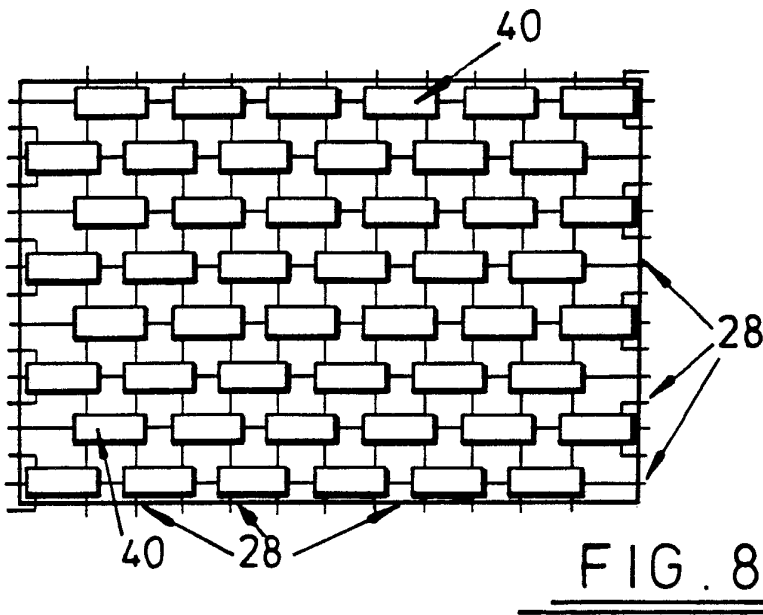
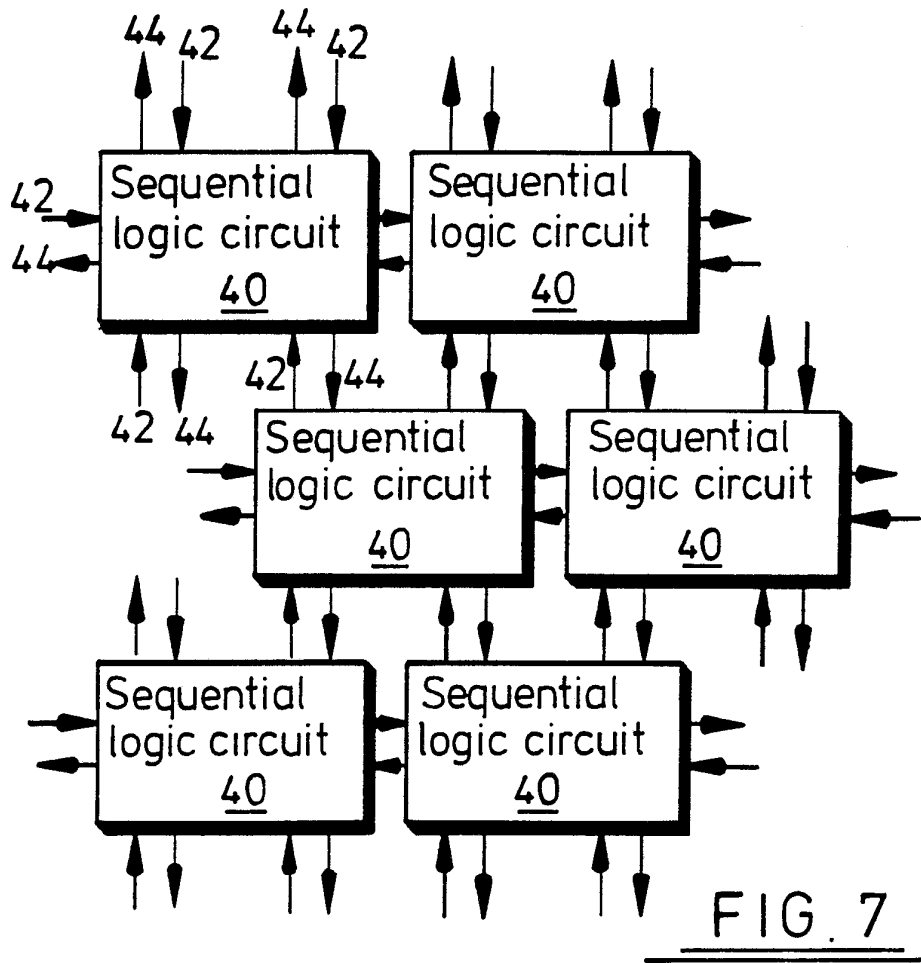


FIG. 3





INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 90/01841

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶ According to International Patent Classification (IPC) or to both National Classification and IPC IPC ⁵ : G 09 B 23/12, G 09 B 23/06, G 06 F 15/60, G 09 B 23/18																							
II. FIELDS SEARCHED Minimum Documentation Searched ⁷ <table style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 30%; border-bottom: 1px solid black;">Classification System</th> <th style="border-bottom: 1px solid black;">Classification Symbols</th> </tr> <tr> <td style="padding: 5px; vertical-align: top;">IPC⁵</td> <td style="padding: 5px; vertical-align: top;">G 09 B, G 06 F</td> </tr> </table> Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁸			Classification System	Classification Symbols	IPC ⁵	G 09 B, G 06 F																	
Classification System	Classification Symbols																						
IPC ⁵	G 09 B, G 06 F																						
III. DOCUMENTS CONSIDERED TO BE RELEVANT⁹ <table style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 10%; border-bottom: 1px solid black;">Category ⁹</th> <th style="width: 70%; border-bottom: 1px solid black;">Citation of Document, ¹¹ with Indication, where appropriate, of the relevant passages ¹²</th> <th style="width: 20%; border-bottom: 1px solid black;">Relevant to Claim No. ¹³</th> </tr> <tr> <td style="text-align: center; vertical-align: top; padding: 5px;">Y</td> <td style="padding: 5px;">EP, A, 0228915 (S. WOLFRAM) 15 July 1987 see page 7, line 17 - page 30, line 20; claims; figures</td> <td style="text-align: center; vertical-align: top; padding: 5px;">1,2,4</td> </tr> <tr> <td style="text-align: center; vertical-align: top; padding: 5px;">A</td> <td style="text-align: center; vertical-align: top; padding: 5px;">--</td> <td style="text-align: center; vertical-align: top; padding: 5px;">5,8,11</td> </tr> <tr> <td style="text-align: center; vertical-align: top; padding: 5px;">P,Y</td> <td style="padding: 5px;">EP, A, 0372833 (S.P. SAMPLE) 13 June 1990 see column 2, line 26 - column 18, line 2; claims 1-3,5,7; figures</td> <td style="text-align: center; vertical-align: top; padding: 5px;">1,2,4</td> </tr> <tr> <td style="text-align: center; vertical-align: top; padding: 5px;">A</td> <td style="text-align: center; vertical-align: top; padding: 5px;">--</td> <td style="text-align: center; vertical-align: top; padding: 5px;">5-7</td> </tr> <tr> <td style="text-align: center; vertical-align: top; padding: 5px;">A</td> <td style="padding: 5px;">US, A, 3728534 (U. BERTRAM et al.) 17 April 1973 see column 3, line 27 - column 6, line 15; claims; figures</td> <td style="text-align: center; vertical-align: top; padding: 5px;">1,4-6,8,9</td> </tr> <tr> <td colspan="3" style="text-align: center; padding: 10px;">./.</td> </tr> </table>			Category ⁹	Citation of Document, ¹¹ with Indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³	Y	EP, A, 0228915 (S. WOLFRAM) 15 July 1987 see page 7, line 17 - page 30, line 20; claims; figures	1,2,4	A	--	5,8,11	P,Y	EP, A, 0372833 (S.P. SAMPLE) 13 June 1990 see column 2, line 26 - column 18, line 2; claims 1-3,5,7; figures	1,2,4	A	--	5-7	A	US, A, 3728534 (U. BERTRAM et al.) 17 April 1973 see column 3, line 27 - column 6, line 15; claims; figures	1,4-6,8,9	./.		
Category ⁹	Citation of Document, ¹¹ with Indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³																					
Y	EP, A, 0228915 (S. WOLFRAM) 15 July 1987 see page 7, line 17 - page 30, line 20; claims; figures	1,2,4																					
A	--	5,8,11																					
P,Y	EP, A, 0372833 (S.P. SAMPLE) 13 June 1990 see column 2, line 26 - column 18, line 2; claims 1-3,5,7; figures	1,2,4																					
A	--	5-7																					
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¹⁰ Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "G" document member of the same patent family																							
IV. CERTIFICATION <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; padding: 5px;"> Date of the Actual Completion of the International Search 10th April 1991 </td> <td style="width: 50%; padding: 5px;"> Date of Mailing of this International Search Report 21. 05. 91 </td> </tr> <tr> <td style="padding: 5px;"> International Searching Authority EUROPEAN PATENT OFFICE </td> <td style="padding: 5px;"> Signature of Authorized Officer M. PEIS M. Peis </td> </tr> </table>			Date of the Actual Completion of the International Search 10th April 1991	Date of Mailing of this International Search Report 21. 05. 91	International Searching Authority EUROPEAN PATENT OFFICE	Signature of Authorized Officer M. PEIS M. Peis																	
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International Searching Authority EUROPEAN PATENT OFFICE	Signature of Authorized Officer M. PEIS M. Peis																						

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)		
Category *	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	US, A, 4376538 (M.P. KEENAN) 15 March 1983 see column 7, line 40 - column 9, line 27; claim 1; figures 4,5 --	1,4,5,8,11
A	Electro 1988 Conference Record, vol. 13, 10-12 May 1988, (Los Angeles, CA, US), K. McElvain: "A functional modeling strategy for silicon compilation", pages 1-7 see the whole article -----	1

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

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SA 42279

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
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