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(54) Titre : CIRCUIT POUR LA RECUPERATION D'UN SIGNAL DE DONNEES ET LA REGENERATION D'UN SIGNAL D'HORLOGE

(54) Title: CIRCUIT FOR DATA SIGNAL RECOVERY AND CLOCK SIGNAL REGENERATION

(57) Abrégé/Abstract:
According to the invention, the circuit for recovering a data signal and regenerating a clock signal can be fully integrated into a chip and has two independent series-mounted PLL regulating steps (2, 6) that can be optimally adjusted in a separate manner. The first regulating step (2) has a wide bandwidth and is optimized for the highest possible jitter tolerance. The second regulating step (2, 6) has a narrow bandwidth and is optimized for the lowest possible jitter transfer. The circuit can be used, for example, in transceivers for ATM, SONET and SDH applications with Gbit signal transmission links.

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Abstract

According to the invention, the circuit for recovering a data signal and regenerating a clock signal can be fully integrated into a chip and has two independent series-mounted PLL regulating steps (2, 6) that can be optimally adjusted in a separate manner. The first regulating step (2) has a wide bandwidth and is optimized for the highest possible jitter tolerance. The second regulating step (2, 6) has a narrow bandwidth and is optimized for the lowest possible jitter transfer. The circuit can be used, for example, in transceivers for ATM, SONET and SDH applications with Gbit signal transmission links.

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Circuit for data signal recovery and clock signal regeneration

The invention relates to a circuit, which can be completely integrated in an electronic module (chip), for data signal recovery and clock signal regeneration from an incoming serial data signal stream, using a PLL (Phase Locked Loop) regulating stage which is provided with a voltage-controlled oscillator (VCO) and to which the serial data signal stream is fed, having a retiming circuit.

The invention is directed, in particular, at the recovery and the retiming of data signals and clock signals, respectively, from serial data streams, e.g. in transceiver circuits for ATM (asynchronous transfer mode), SONET (synchronous optical network) and SDH (synchronous digital hierarchy) applications.

It is known to realize the reconditioning of data signals and clock signals with the aid of a PLL regulating stage and retiming flip-flop. There are diverse types of phase and frequency detectors for this purpose. In this connection, reference is made to the paper by Herzog, Hans-Jürgen: "Auswahl von Bausteinen für die Daten- und Taktregenerierung in Telekom- und Datennetzen" ["Selection of modules for data and clock regeneration in telecommunications and data networks"], published in the journal "HF-Praxis", issue 5, 1998, volume 4, pp. 12-14.

The incoming data signal is generally a serial bit sequence incumbent with noise and jitter. Various requirements are imposed on a transceiver which receives and evaluates this data signal stream, in order that a signal of required quality is produced again on the output side. Two important

requirements, which, however, are partly at odds with one another, are the values for the jitter tolerance and for the jitter transfer. The jitter tolerance defines the maximum permissible input jitter which the circuit can still process in a manner free from errors. This value should be as large as possible. The jitter transfer defines the maximum permissible jitter which is allowed to be transferred from the input to the output. It should be as small as possible.

In order to fulfill these jitter requirements, the bandwidth of the PLL regulating loop used in the reconditioning of data signals and clock signals must be adapted to the requirements. A large PLL regulating loop bandwidth is necessary for a large jitter tolerance.

A large bandwidth enables the PLL regulating loop to effect rapid following in terms of the frequency and phase of the incoming signal and thus reliable sampling in the temporal center of a data bit. This fact then also results in the circuit having high input sensitivity.

A small PLL regulating loop bandwidth is necessary for a low jitter transfer. This ensures that the PLL regulating stage does not follow the high-frequency jitter, noise and other interference and thus impair the quality of the recovered data signal.

In order to simultaneously meet both conditions to some extent, one is thus forced to adopt a compromise. In this case, the bandwidth of such a PLL regulating loop is in a very narrow range. Since a PLL regulating stage can in part comprise highly nonlinear components, particularly in the case of completely integrated PLL regulating loops, it is difficult to calculate or realize the bandwidth.

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The invention is based on the object of providing a circuit, which can be completely integrated on an electronic chip and thus implemented without external circuitry, for the recovery and for the retiming of data signals and clock signals, respectively, from serial data streams, in particular for a simpler construction of ATM, SONET and SDH-conforming transceiver circuits for possible use in signal transmission links in the gigabit range, the jitter requirements being complied with and, consequently, a data signal of required quality, that is to say having a prescribed low bit error rate, being produced again on the output side.

This object is achieved, according to the invention, which relates to a circuit of the type mentioned in the introduction, by virtue of the fact that there is connected downstream of the PLL regulating stage in series a second PLL regulating stage, that the two PLL regulating stages are independent and are each optimally adjustable separately, that the first PLL regulating stage is set in such a way that it has a large bandwidth and is optimized for maximum jitter tolerance, and that the second PLL regulating stage is set in such a way that it has a small bandwidth and is optimized for minimum jitter transfer.

Accordingly, in one aspect of the invention, there is provided a circuit for data signal recovery and clock signal regeneration from an incoming serial data signal stream comprising data bits, comprising: a first PLL regulating stage having a voltage-controlled oscillator, an input receiving a serial data signal stream, and an output outputting a clock signal; a second PLL regulating stage connected to said output of said first PLL regulating stage and in series therewith, said second PLL regulating stage having an input receiving the clock signal and an output

outputting an output clock signal; said first and second PLL regulating stages adjusted separately, said first PLL regulating stage being set at a first bandwidth, and said second PLL regulating stage being fixed at a second bandwidth smaller than the first bandwidth.

In a second aspect, there is provided a circuit assembly for data signal recovery and clock signal regeneration, comprising: a transceiver circuit at an end of a transmission link of a telecommunications and data transmission network emitting a serial data signal stream having data bits; and a circuit receiving the serial data signal from the transceiver circuit and including a first PLL regulating stage having a voltage-controlled oscillator, an input receiving a serial data signal stream, and an output outputting a clock signal; a second PLL regulating stage connected to said output of said first PLL regulating stage and in series therewith, said second PLL regulating stage having an input receiving the clock signal and an output outputting an output clock signal; said first and second PLL regulating stages each being adjusted separately, said first PLL regulating stage being set at a first bandwidth, and said second PLL regulating stage being fixed a t a second bandwidth smaller than the first bandwidth.

In a third aspect, there is provided a circuit assembly for data signal recovery and clock signal regeneration, comprising: a signal transmission link operating in a gigabit range; and a circuit being connected to said signal transmission link and including a first PLL regulating stage having a voltage-controlled oscillator, an input receiving a serial data signal stream, and an output outputting a clock signal; a second PLL regulating stage connected to said output of said first PLL regulating stage

and in series therewith, said second PLL regulating stage having an input receiving the clock signal and an output outputting an output clock signal; said first and second PLL regulating stages each being adjusted separately, said first PLL regulating stage being set at a first bandwidth, and said second PLL regulating stage being fixed at a second bandwidth smaller than the first bandwidth.

In a fourth aspect, there is provided an electronic module assembly, comprising an electronic module containing a completely integrated circuit including a first PLL regulating stage having a voltage-controlled oscillator, an input receiving a serial data signal stream, and an output outputting a clock signal; a second PLL regulating stage connected to said output of said first PLL regulating stage and in series therewith, said second PLL regulating stage having an input receiving the clock signal and an output outputting an output clock signal; said first and second PLL regulating stages each being adjusted separately, said first PLL regulating stage being set at a first bandwidth, and said second PLL regulating stage being fixed at a second bandwidth smaller than the first bandwidth.

The invention thus solves the problem by connecting two independent PLL regulating stages in series, for each of which the optimum setting is performed separately. The first PLL regulating stage has a large bandwidth and regenerates the level of the incoming signal.

As a result, the signal/noise ratio becomes less critical and the second PLL regulating stage can guarantee error-free data regeneration, even without sampling in the absolute center of a data bit. The second PLL regulating stage has a small bandwidth and can thus be optimized for low jitter transfer.

Complete integration on a single chip is possible since the circuit according to the invention can tolerate relatively large parameter fluctuations of the circuit.

Advantageously, the transition from the first PLL regulating stage to the second PLL regulating stage is performed by means of synchronization of the two clock signals which is carried out in the second PLL regulating stage. The second PLL regulating stage can be realized in a simple manner and without a high technical outlay on circuitry.

The reference frequency of the first PLL regulating stage is expediently stabilized by a frequency-constant crystal oscillator.

A circuit for data signal recovery and clock signal regeneration according to the invention is explained below with reference to a block diagram illustrated in the accompanying drawing.

The sole FIGURE of the drawing shows a schematic block circuit diagram of a circuit according to an embodiment of the invention.

An incoming digital data stream DATA IN is fed to a first PLL regulating stage 2 via an isolation amplifier 1. The reference frequency f_{Ref} of the PLL regulating stage 2 is formed by a crystal oscillator 3, is therefore stable in frequency and holds a voltage-controlled oscillator in a valid operating range.

The first PLL regulating stage 2 is provided with a voltage-controlled oscillator (VCO) 4, which may be realized by a ring oscillator, for example, and an integrator 5, with which the bandwidth of the PLL regulating stage 2 is determined. There is connected downstream of the first PLL

regulating stage 2 a second PLL regulating stage 6, which is likewise provided with a voltage-controlled oscillator 7 and an integrator 8 which critically determines the bandwidth of the second PLL regulating stage 6.

The finally recovered data signals and clock signals DATA OUT and CLOCK OUT respectivcly, are passed out from the second PLL regulating stage 6 via a respective isolation amplifier 9 and 10. The optimum setting for the two independent PLL regulating stages 2 and 6 is performed separately in each case. The first PLL regulating stage 2 has a large bandwidth and regenerates the level of the incoming signal DATA IN.

The signal/noise ratio thus becomes less critical, and the second PLL regulating stage 6 ensures error-free data recovery, and it does not necessarily have to effect sampling in the absolute center of the data bits of the data signals DATA fed from the first PLL regulating stage 2.

In contrast to the first PLL regulating stage 2, the second PLL regulating stage 6 has a small bandwidth and can be optimized for minimum jitter transfer. The transition from the first PLL regulating stage 2, in which the data signals DATA and clock signals CLOCK are recovered, is effected by means of synchronization of the two clock signals CLOCK and CLOCK OUT in the PLL regulating stage 6, which can be realized in a relatively simple manner.

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CLAIMS:

1. A circuit for data signal recovery and clock signal regeneration from an incoming serial data signal stream comprising data bits, comprising:

a first PLL regulating stage having a voltage-controlled oscillator, an input receiving a serial data signal stream, and an output outputting a clock signal;

a second PLL regulating stage connected to said output of said first PLL regulating stage and in series therewith, said second PLL regulating stage having an input receiving the clock signal and an output outputting an output clock signal;

said first and second PLL regulating stages adjusted separately, said first PLL regulating stage being set at a first bandwidth, and said second PLL regulating stage being fixed at a second bandwidth smaller than the first bandwidth.

2. The circuit as claimed in claim 1, characterized in that

the transition from the first PLL regulating stage to the second PLL regulating stage is performed by means of synchronization of the clock signal and the output clock signal which is realized in the second PLL regulating stage.

3. The circuit as claimed in claim 1 or 2, characterized in that

a reference frequency of the first PLL regulating stage is stabilized by a frequency-constant crystal oscillator.

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4. The circuit as claimed in any one of claims 1 to 3, characterized by

application in transceiver circuits at the end of transmission links of a telecommunications and data transmission network.

5. The circuit as claimed in any one of claims 1 to 4, characterized by

use in signal transmission links in the gigabit range.

6. A circuit assembly for data signal recovery and clock signal regeneration, comprising:

a transceiver circuit at an end of a transmission link of a telecommunications and data transmission network emitting a serial data signal stream having data bits; and

a circuit receiving the serial data signal from the transceiver circuit and including a first PLL regulating stage having a voltage-controlled oscillator, an input receiving a serial data signal stream, and an output outputting a clock signal; a second PLL regulating stage connected to said output of said first PLL regulating stage and in series therewith, said second PLL regulating stage having an input receiving the clock signal and an output outputting an output clock signal; said first and second PLL regulating stages each being adjusted separately, said first PLL regulating stage being set at a first bandwidth, and said second PLL regulating stage being fixed at a second bandwidth smaller than the first bandwidth.

7. A circuit assembly for data signal recovery and clock signal regeneration, comprising:

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a signal transmission link operating in a gigabit range; and

a circuit being connected to said signal transmission link and including a first PLL regulating stage having a voltage-controlled oscillator, an input receiving a serial data signal stream, and an output outputting a clock signal; a second PLL regulating stage connected to said output of said first PLL regulating stage and in series therewith, said second PLL regulating stage having an input receiving the clock signal and an output outputting an output clock signal; said first and second PLL regulating stages each being adjusted separately, said first PLL regulating stage being set at a first bandwidth, and said second PLL regulating stage being fixed at a second bandwidth smaller than the first bandwidth.

8. An electronic module assembly, comprising an electronic module containing a completely integrated circuit including a first PLL regulating stage having a voltage-controlled oscillator, an input receiving a serial data signal stream, and an output outputting a clock signal; a second PLL regulating stage connected to said output of said first PLL regulating stage and in series therewith, said second PLL regulating stage having an input receiving the clock signal and an output outputting an output clock signal; said first and second PLL regulating stages each being adjusted separately, said first PLL regulating stage being set at a first bandwidth, and said second PLL regulating stage being fixed at a second bandwidth smaller than the first bandwidth.

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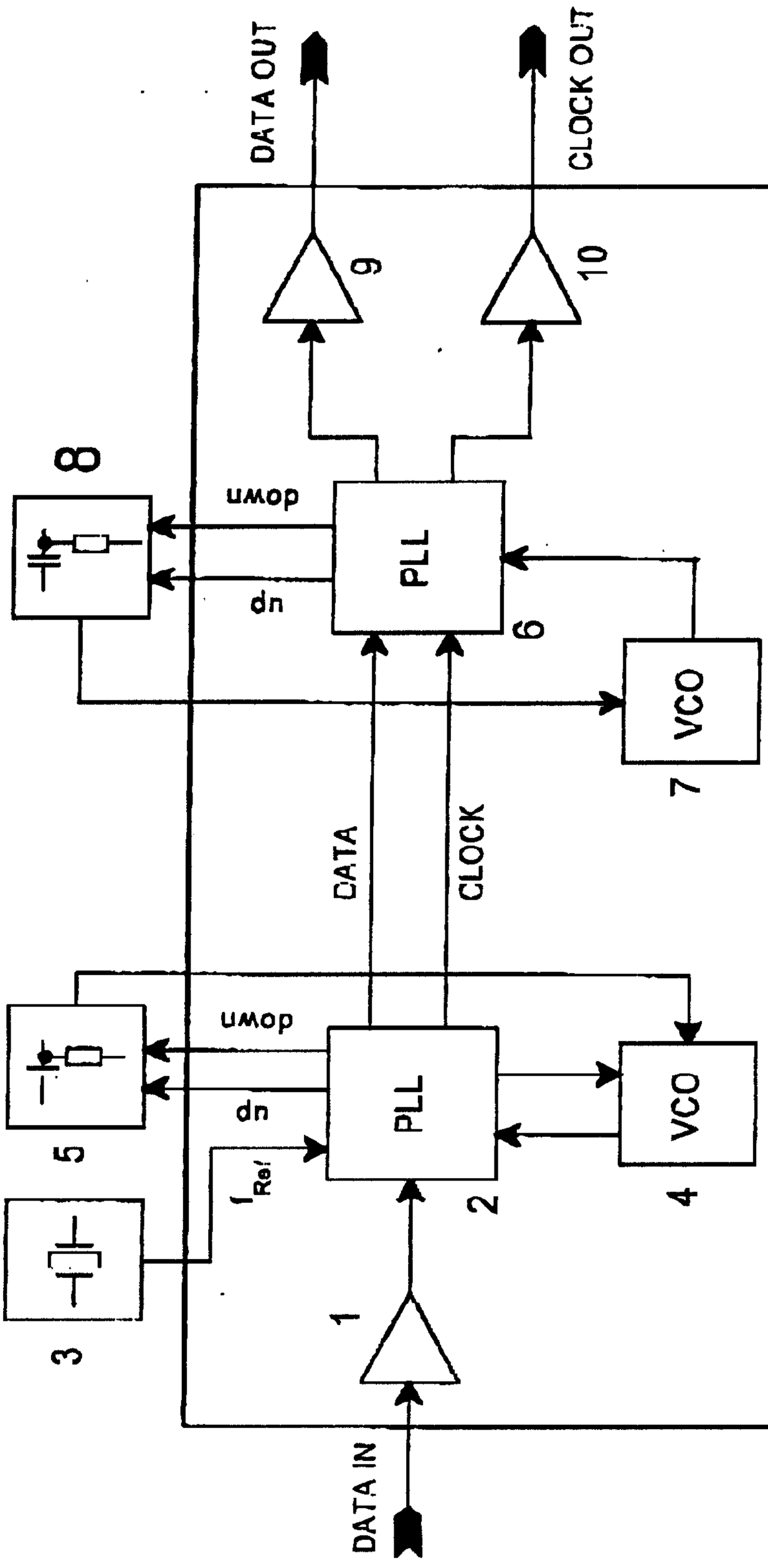
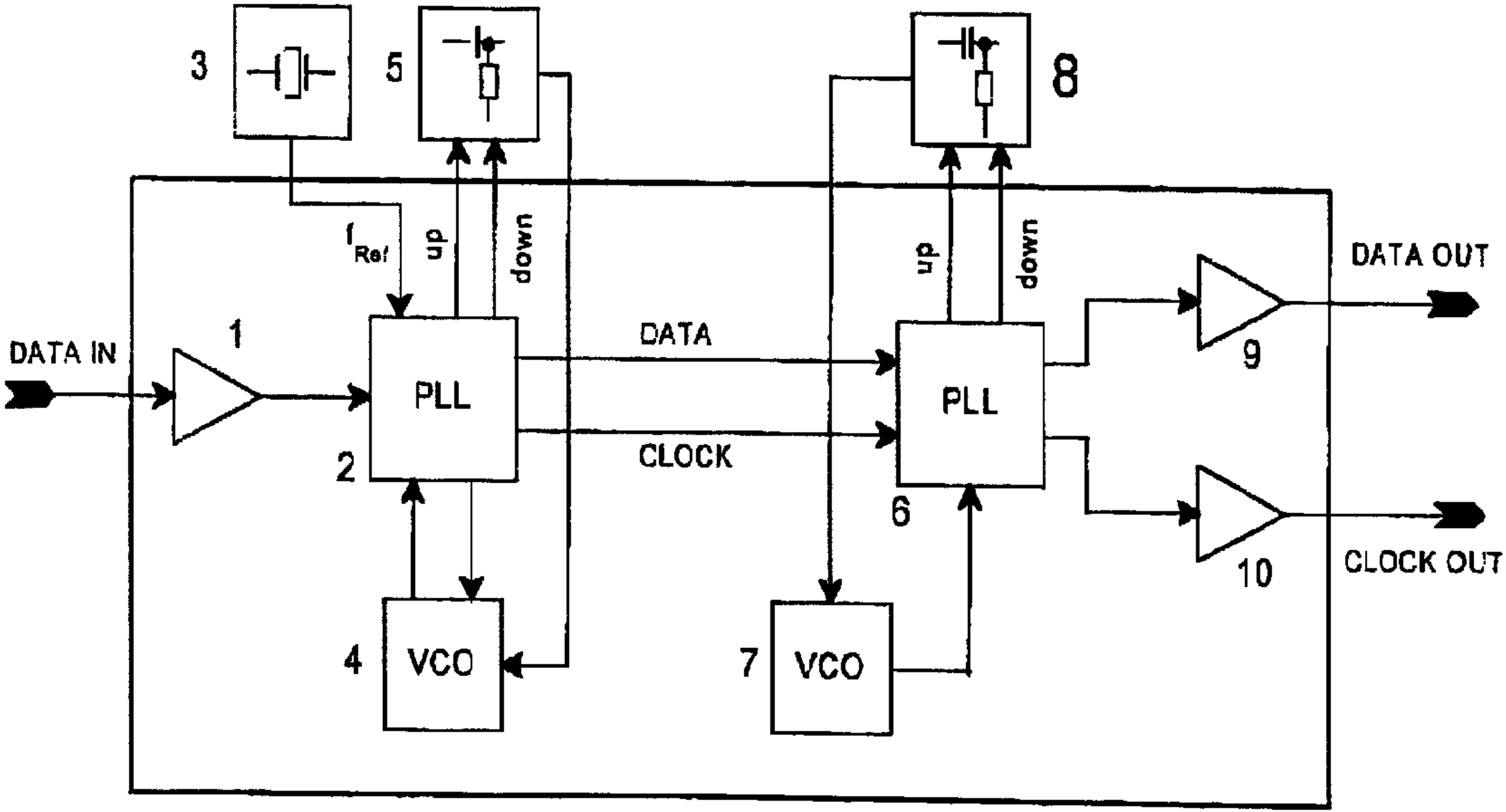
PATENT AGENTS


DATA OUT
CLOCK OUT
9
10
8
down
PLL
up
6
VCO
7
DATA
CLOCK
5
down
PLL
VCO
dn
f_{Ref}
4
2
3
1
N
DATA IN


3
5
8
f_{Ref}
up
down
up
down
DATA OUT
DATA IN
1
DATA
PLL
PLL
9
2
CLOCK
6
10
CLOCK OUT
4
VCO
7
VCO