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(54) Multiplexer circuit.

(57) A multiplexer circuit for effecting in successive phases of operation thereof actuation of selected devices of respective groups of devices of a series of capacitance actuated devices has a series of parallel electrical paths to which the respective devices are connected. A signal generator is connected across said paths and two capacitors of each device are connected between the path of the associated device and the respective paths on opposite sides of the path of the associated device. First and second switching means are disposed in each path and are closed by respective logic signals applied thereto so that when the first and second switching means of one path are respectively closed and open and the first and second switching means of each of the paths on respective opposite sides of that one path are respectively open and closed, charging of the capacitors connected to that one path takes place and when thereafter the first and second switching means of that one path are respectively open and closed discharge of the capacitors connected to that one path takes place.

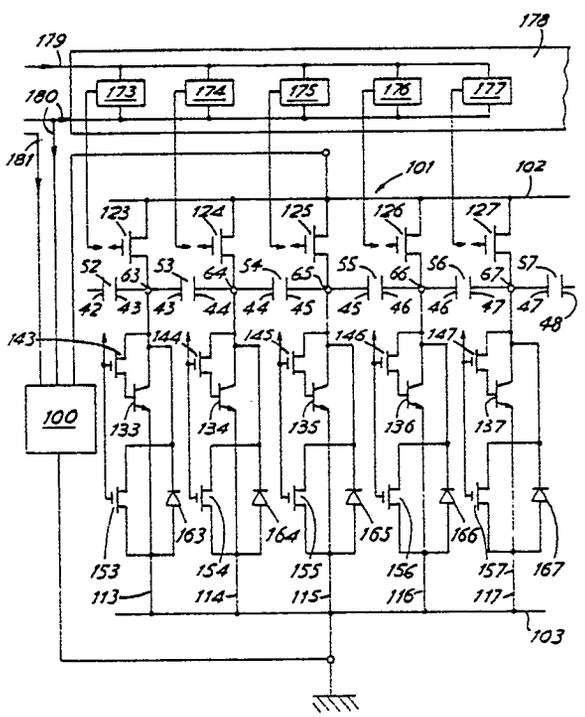

FIG.2

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Multiplexer Circuit.

This invention relates to multiplexer circuits for effecting in successive phases of operation thereof actuation of selected devices of respective groups of devices of a series of capacitance actuated devices.

One application of such a multiplexer circuit is a pulsed droplet deposition apparatus, such as a drop-on-demand ink jet printer having a multi-channel array from the channels of which the droplets are ejected and in which the channels are arranged in groups, channels from the respective groups being selected for printing droplets in successive phases of operation of the multiplexer circuit. In known forms of pulsed droplet ink jet printers, so-called drop-on-demand printers, circuits to handle substantial actuating currents have to be constructed and such currents give rise to risk of burn-out failure. One object of the present invention is to provide a multiplexer circuit for such an application which is called upon to handle only relatively low power. Further, in known forms of pulsed droplet ink jet printed die switching of the substantial actuating currents gives rise to radio frequencey interference. It is therefore a further object of the invention to minimise such interference.

The present invention consists in a multiplexer circuit for effecting in successive phases of operation thereof actuation of selected devices of respective groups of devices of a series of capacitance actuated devices, characterised in that said circuit comprises a series of parallel connected electrical paths to which the respective devices are adapted to be connected, said paths being adapted for connection in parallel with a signal generator, with two capacitors of each device connected between the path of the associated device and the respective paths on opposite sides of said path of said associated device and first and second switching means disposed in each path and adapted to be closed by respective logic signals applied thereto so that when the first and second switching means of one path are respectively closed and open and the first and second switching means of each of the paths on respective opposite sides of said one path are respectively open and closed, charging of the capacitors connected to said one path takes place and when thereafter the first and second switching means of said one path are respectively open and closed discharge of the capacitors connected to said one path takes place.

Suitably, a diode device is connected across the second switching means of each path and provides a conductive path for discharging capacitors connected between the path in which said diode is connected and the paths on respective opposite sides thereof.

Advantageously, the first and second switching means are provided on a silicon chip integrated circuit, said switching means comprising transistor switches. Suitably, the transistor means comprise field effect transistors.

In one form of multiplexer circuit according to the invention the second switching means of each path comprises first and second switching components of which the first switching component provides a by-pass path in parallel with the second switching component during charging of the capacitors connected between the path containing said second switching means and the paths on opposite sides thereof by way of the first switching means of said paths on opposite sides of the path containing said second switching means, whilst the second switching component provides a conductive path for discharging the capacitors connected to the path containing said second switching component after charging thereof by way of the first switching means contained in the same path as said second switching component. Suitably, the first and second switching means are provided on a silicon chip integrated circuit, the first switching means comprising a field effect transistor and the first and second switching components of the second switching means comprising respectively a field effect transistor and a field effect transistor controlling conduction of a bipolar transistor.

Suitably, in each phase of operation the capacitors of devices selected for actuation are charged in an initial part of a voltage waveform-supplied from the signal generator after which the signal generator is disconnected from the circuit for a further interval of said waveform prior to discharge of the charged capacitors. Suitably, the signal generator and the parallel electrical paths and the first and second switching means thereof are formed in a silicon chip integrated circuit.

According to a desirable feature of the invention where actuation of each selected device is required to cause a substantially identical effect and where actuation of any device is affected by the actuated or non-actuated status of devices on opposite sides of that actuated device, it is important to effect the actuation of each selected device according to the actuated or non-actuated status of devices adjacent each selected device. To that end, the logic signal applying means are adapted to apply signals to the first and second switching means to enable charging of the capacitors of each of the devices selected fob actuation for a period dependent upon the actuated or non-actuated status of devices adjacent each of said selected de-

vices.

The invention further consists in a multi-channel array, electrically pulsed droplet deposition apparatus for depositing liquid droplets upon a surface, comprising a droplet deposition head formed from electrically active material, a multiplicity of channels for liquid formed in said head and arranged in a plurality of groups, nozzles communicating with the respective channels, longitudinal side walls each serving to divide one channel from the next and electrically actuable means for effecting transverse displacement in opposite senses of said longitudinal side-walls of each channel, said electrically actuable means comprising electrodes in each channel on respective facing surfaces of the longitudinal channel side-walls, conductive means connecting the electrodes in each channel, said electrodes forming a series of capacitors each consisting of one of said longitudinal channel side walls and the electrodes on opposite sides thereof and a multiplexer circuit for effecting in successive phases of operation actuation of said longitudinal walls of selected channels in the respective channel groups, said circuit comprising a series of parallel electrical paths, said capacitors being connected respectively between successive paths of said electrical paths, a signal generator connected across said parallel electrical paths, first and second switching means disposed in each of said paths, and logic signal applying means for effecting conduction of said first and second switching means, so that when the first and second switching means of one path are respectively closed and open and the first and second switching means of each of the paths on opposite sides of said one path are respectively open and closed charging of the capacitors connected to said one path takes place and when thereafter the first and second switching means of said one path are respectively open and closed discharge of said capacitors takes place.

With a pulsed droplet deposition apparatus according to the invention, cross-talk due to channel wall compliance, i.e. the effect in an actuated channel of pressures existing in neighbouring channels, can, according to an important feature of the invention, be compensated for electrically. To achieve such compensation, the logic signal applying means are adapted to apply signals to the first and second switching means in each of said parallel paths to which the capacitors of selected channels are connected to enable charging of the capacitors of each selected channel for a period to provide a voltage level thereon dependent upon the selected or non-selected status of adjacent channels of the group containing the selected channels.

Suitably, the signal generator is adapted during charging of said capacitors to apply a signal to the capacitors of the selected channels which is of relatively slowly increasing voltage and the logic signal applying means are adapted to effect disconnection of the signal generator from the capacitors of said selected channels when a predetermined charge voltage is reached and after an interval to actuate the switching means to effect rapid discharge of the charged capacitors whereby during charging of the capacitors of the selected channels the longitudinal side walls of the said channel are displaced outwardly relatively slowly and during discharge of the capacitors the channel walls are rapidly returned.

The invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings of which:

FIGURE 1 illustrates a cross-section of an ink jet printhead having shear mode wall actuators as described in co-pending European Patent Application No. 88300146.3;

FIGURE 2 illustrates one form of multiplexer circuit as connected to the shear mode actuators of the printhead illustrated in Figure 1;

FIGURE 3 illustrates a further form of multiplexer circuit for use with the shear mode actuators of Figure 1; and

FIGURE 4 illustrates a suitable waveform for operation of the ink jet printhead of Figure 1 employing the circuit of either Figure 2 or Figure 3.

In the drawings like parts are accorded the same reference numerals.

Figure 1 illustrates a module part 10 of an ink jet printhead 12 in which a multiplicity of closely spaced drop-on-demand ink drop ejectors are disposed side by side in an array. The ejectors consist of extended parallel channels 20-28 filled with ink and separated by piezo-electric shear mode wall actuators 30-39, such as are disclosed in co-pending European Patent Application No. 88300146.3 the contents of which are herein incorporated by reference.

The ink channels 20-28 have electrodes 40-48 coating the walls of each channel, which provide actuating electrodes for the wall actuators and which, together with the wall actuators effectively form capacitors 50 to 58. The electrodes are connected via tracks 70-78 to terminals 60-68 of a silicon chip integrated circuit hereinafter referred to.

As explained in the co-pending European Patent Application referred to, the ink ejectors are divided separately into two groups of odd and even numbered channels and selected channels in the odd and even numbered groups are actuated in alternating cycles. In a typical cycle, operation is performed by holding the electrodes of one group (e.g. the even numbered channels) at earth potential and applying a voltage waveform to those chan-

nels due to print in the odd group of channels.

One typical multiplexer drive circuit is illustrated in Figure 2 which shows a signal generator 100 provided in a silicon chip integrated circuit 101 and connected across internal buses 102 and 103 thereof, bus 102 being connected to the positive output terminal of the signal generator and bus 103 to the negative output terminal thereof which is held at ground potential. Between the buses 102 and 103, there are provided parallel electrical paths respectively associated with the actuator channels and of which only paths 113 to 117 are illustrated and these respectively include terminals 63 to 67.

Between the bus 102 and the terminals 63 to 67 are connected in the paths 113 to 117 respective field effect transistor devices 123 to 127 at the gate electrode of each of which is applicable as hereinafter described an internally generated logic signal to render the device conductive.

Between the terminals 63 to 67 and the bus 103, the paths 113 to 117 respectively include the collector emitter paths of n-p-n bipolar transistor devices 133 to 137. The base emitter paths of these devices respectively include field effect devices 143 to 147 to the gate electrodes of which are applicable internally generated logic signals to render these devices conductive. The collector emitter paths of devices 133 to 137 are shunted by respective field effect devices 153 to 157 the gate electrodes of which are connected to the gate electrodes of devices 143 to 147 so that these devices are rendered conductive by the same logic signals as activate the devices 143 to 147. The devices 153 to 157 are themselves respectively shunted by diodes 163 to 167 which provide capacitor discharge paths as hereinafter referred to.

The logic signals for effecting and terminating conduction of the transistors 123-127, 143-147 and 153-157 are supplied from registers 173-177 of logic block 178 to which is supplied print pattern data on a line 179 and relatively high frequency clock pulses on a line 180 which connects also with the signal generator 100 to which is also connected a clock line 181 on which are supplied relatively low frequency clock pulses.

The data stream supplied on line 179 consists of an N bit print pattern applied to each chip of the printhead where N is the number of channels to which the chip is connected. The N bits determine in one cycle which of the channels of the even numbered channel group are to be actuated and in a following cycle which of the channels of the odd numbered channel group are to be actuated. The N bit data stream additionally contains subsets n of data relating to the print status of channels of the same group as those selected for actuation on opposite sides of each of the selected channels which are to be actuated. The data sets n may be four bit words in which case they give the print status of two channels of the same group as the selected channels on each side of each channel selected for actuation. If the data sets n are in the form of six bit words they give the print status of three channels on each side of each channel which is to be actuated.

At the end of printing of a printline and before the next pulse on the line 181 is supplied to the signal generator 100 the data N with its subsets n is loaded into the registers 173 to 177 at the rate set by the clock pulses on line 180, suitably about 10MHertz and the data sets n are sent to a look-up table in a ROM (not shown) which sends digital signals respectively determined by the data sets n to the registers 173-177 which signals are stored in the registers and employed to afford a count of pulses on line 180 which determines the level of charging of the capacitors of each actuated channel.

The voltage cycles applied by the signal generator 100 across the buses 102 and 103 are initiated by the pulses on the clock line 181 and upon initiation of one such cycle the data stored in the registers 171 to 177 selects for printing the channels of one of the channel groups which have their transistors 123-127 switched on and their transistors 143 to 147 switched off so that charging of the capacitors of the selected channels commences and is terminated by switching off of the transistors 123-127 of the selected channels when the voltage level thereon reaches a value determined by the digital signals stored in the registers 173-179 and supplied thereto from the look-up table referred to. The registers of each of the end channels of modules making up the printhead, it will be appreciated, receive from the ROM sets n of bits which provide the print status of adjoining channels spanning the butted region of the module in which the end channel concerned is located and the adjoining module. The integrated circuit of Figure 2 is a bi-C mos design.

Figure 4 illustrates the waveform provided by the signal generator 100 to energise the actuators 30 to 39 during successive phases of the two phase multiplexer circuit circuit of Figure 2. The waveform consists of a charge period τ_1 during which the charge on the capacitors 52 to 57 belonging to one of the channel groups gradually rises to predetermined values for each channel of that group selected for actuation at which the capacitors are disconnected from the signal generator and remain at or substantially at their charged voltage level for a further period, the "hold" period, τ_2, during which the signal voltage is kept at least at the level of the charge voltage. As shown, the signal voltage is allowed in this period first to rise above and at the end of the period return to the

charge voltage. After the period τ_2 the signal voltage proceeds to zero to enable reconnection of the signal generator to the capacitors for the next phase of operation. Before that commences a rapid discharge of the capacitors, as hereinafter described, is effected.

In the period τ_1, the wall actuator electrodes of selected channels of say the odd numbered channels 21 to 27 are energised to cause the wall actuators to deform outwards from the channels into a chevron or cantilever form as described in the co-pending European patent application referred to due to the charge voltage and the direction of polarisation of the wall actuators. The rate of rise of voltage is however gradual so that the magnitude of the acoustic waves formed in the ink channels only mildly disturbs the ink menisci in the ejection nozzles of the channels and is not sufficient to eject drops of ink from the nozzles of the even numbered channels adjacent the activated even numbered channels. The charge period τ_1 exceeds the time of travel of acoustic waves in the activated channels so that $\tau_1 \geq L/C$ where L is the channel length and C is the acoustic wave velocity in the channels.

In the hold period τ_2 further ink is drawn into the activated odd numbered channels by the action of the acoustic waves and this causes the channel wall actuators to relax outwardly as the ink quantity in the channels increases. After the hold period, typically also L/C, the pressure of ink in the selected channels is a maximum and the capacitors of those channels are then rapidly discharged to cause rapid inward movement of the channel actuator walls which generates pressure waves in the selected channels causing ejection of an ink drop from the nozzles of those channels. After replenishment of ink in the channels from which ink drop ejection has taken place, the next phase of operation is effected on selected even numbered channels by a further signal phase of the signal generator.

The detailed operation of the drive circuit components of Figure 2 will now be described. In the quiescent state of the circuit the devices 143 to 147 and the devices 153 to 157 are held in a conducting condition by an internally generated logic signal applied to the gate electrodes thereof, whilst devices 123 to 127 are in a non-conducting condition. Assuming now that channel 25 is one of the group of odd numbered channels to be selected for activation, at the commencement of the period τ_1 of the signal from the signal generator which is initiated by a pulse on line 181, the field effect device 125 is rendered conductive by a logic signal from register 175 applied to its gate and the signal at the gate electrodes of devices 145 and 155 is removed so rendering those devices non-conducting. The capacitors 54 and 55 therefore, relatively slowly, charge to a predetermined voltage during the period τ_1, by way of, in the case of capacitor 54, the field effect devices 125 and 154, and, in the case of capacitor 55, by way of field effect devices 125 and 156, the predetermined voltage being determined by the signal from the ROM stored in register 175. The actuator walls of channel 25 accordingly move outwards allowing flow of ink into that channel and, because of the slow rate of charge, no ink drops are expelled from the adjoining channels.

During the hold period τ_2, the logic signals to the field effect devices 125 are removed so disconnecting the actuators from the drive circuit signal.

Firing, that is to say discharge of the capacitor 54 and 55 is effected by applying a signal from the register 175 after a predetermined count of pulses on line 180 to the gate electrodes of the field effect devices 145 and 155 rendering bipolar transistor 135 conducting. This establishes a discharge for capacitor 54 by way of transistor 135 and diode 164 and for capacitor 55 by way of transistor 135 and diode 166. Although during discharge both field effect devices 145 and 155 are conducting, because of the relative resistances of bi-polar transistor 135 and field effect device 155 most of the discharge current flows through transistor 135.

It will be noted that the discharge currents of capacitors 54 and 55 flow through transistor 135 and divide equally between diodes 164 and 166 and these relatively high discharge currents flow respectively in clockwise and anti-clockwise paths so that the electromagnetic effects thereof effectively cancel out thus minimising radio frequency interference. The heating effect of current in the circuit 101 is largely confined to the capacitor discharge currents and therefore to the turn on time of the bi-polar transistors which lasts, typically 30 n. seconds. Also, typically, discharge of capacitors 54 and 55 takes place in 2μ seconds causing currents typically of the order of 100mA and resulting in rapid return of the actuator walls of channel 25 to their relaxed positions thereby developing ink drop ejection pressure in channel 25. Similar discharges firing all the odd numbered channels actuated in the same phase of the operation takes place at the same time as the discharges of capacitors 54 and 55. In the next cycle of operation, the same wave form is applied to the electrodes of the walls of the even numbered channels selected for actuation.

Figure 3 shows a fragment of an alternative design of two phase multiplexer circuit to that of Figure 2 and which is of C-Mos design. It will be seen that in the parallel paths 114,115,116, the diodes now shunt respective field effect transistors

194,195,196. The requisite logic signals for effecting operation of the circuit are the same as for the circuit of Figure 2 and are not shown.

In the quiescent state devices 124 to 126 are in a non-conducting condition and devices 194 to 196 are held in a conducting state by a logic signal applied to their gate electrodes.

In the first phase of the operation of the circuit of Figure 3, assuming channel 25 is chosen as one of the odd numbered channels for activation, capacitors 54 and 55 are charged during period τ_1 by reason of a logic signal being applied to the gate electrode of field effect devices 125 from the associated register, such as register 175 of Figure 2 and the signal at the gate electrode of device 195 is removed. At the end of a period determined by the signal from the ROM stored in the associated register the logic signal at the gate electrode of device 125 is removed to terminate charging of capacitors 54 and 55 at a level determined by the print status of channels on opposite side of channel 25 belonging to same channel group as channel 25 and, after the period τ_2, a logic signal is applied to the gate electrode of device 175 to render that device conductive and thereby to discharge the capacitors 54 and 55. It will be apparent that this circuit has the same advantageous features as were referred to in connection with the circuit of Figure 2.

An ink jet drop-on-demand printhead with connecting tracks and drive circuits built and operated on the principles described provides the following benefits:-

1. Each shear mode actuator wall participates in the operation of the channels on both sides in alternate channels. Each channel is actuated by both the active walls on its boundary. Each actuator wall is fired twice in the course of operating each print line of drops. The design therefore makes an efficient use of the piezo-electric actuators.

2. The connecting tracks joining the drive circuit to the actuators have a density of one track per ink channel, despite the fact that the two actuators that operate each channel have three drive tracks connected to operate them. Thus for example channel 25 connects with the drive circuit by way of track 75 but the actuator walls of that channel require tracks 74, 75 and 76 to operate them.

3. The high currents (100mA) which arise on the discharge of the wall actuators flow only in a localised loop in the printhead. Very little of the heat dissipated by this current is generated in the chip, namely that arising only during the switching period of the discharge transistor.

4. There is no common earth circuit through which the discharge currents are summed after discharging the piezo-electric actuators. In circuits in which the impulsive (drive or discharge) currents are routed in a common return loop, which are commonly used in prior ink jet drive systems, circuits to handle very substantial currents (64 or 128 x 100mA) have to be constructed. Such current magnitudes with frequent operation present a risk of burn-out failure.

5. The discharge currents flow and return in parallel closely spaced tracks in dipole pairs, in which the magnetic fields from the discharge currents substantially cancel. This reduces the magnitude of magnetic radiation to be expected very significantly compared with that generated in the common earth return loop.

6. Each channel in both the even and odd groups is operated with voltage signals of the same polarity, which can be selected according to the poling direction of the ceramic in the piezo-electric actuator. A drive chip having a single polarity of drive circuits is made up of only p- type components and less expensive in construction than a bipolar chip where both p and n type components are required.

7. The voltage signal which operates each channel is compensated to account for the print status of channels on opposite sides thereof.

It will be apparent to those skilled in the art that the switch devices of the integrated circuit could include instead of field effect and bi-polar transistors, silicon controlled rectifiers, four layer diodes or other forms of semi-conductor switch devices.

It will further be apparent to those skilled in the art that although the embodiments of the invention described with reference to Figures 1, 2 and 4 and Figures 1, 3 and 4 require that the printhead channels be arranged in two groups of interleaved channels with the channels of one group alternating with those of the other group, it is quite feasible to employ arrangements having more than two groups of channels. Thus in an arrangement where there are, say, three groups of interleaved channels, the circuits described would have, instead of the two phases of operation described for the circuits of Figures 2 and 3, three phases of operation in which selected channels of the respective groups would be actuated and there would therefore be at least two inactive channels between any two simultaneously actuated channels. For a given density of channels, the greater the number of groups the less acute the problem of cross-talk becomes. The time required to effect printing of a printline however becomes greater and this may complicate the printhead design because of the need spatially to offset the nozzles of each group from those of the

other groups. In the highest density of channels likely to be achievable it is envisaged that wall compliance will be such as to require cross-talk to be limited by both grouping of channels and compensation of the charging voltages of the channel capacitors in dependence upon the print status of adjoining chanels.

Claims

1. A multiplexer circuit for effecting in successive phases of operation thereof actuation of selected devices of respective groups of devices of a series of capacitance actuated devices, characterised in that said circuit comprises a series of parallel connected electrical paths to which the respective devices are adapted to be connected, said paths being adapted for connection in parallel with a signal generator, with two capacitors of each device connected between the path of the associated device and the respective paths on opposite sides of said path of said associated device and first and second switching means disposed in each path and adapted to be closed by respective logic signals applied thereto so that when the first and second switching means of one path are respectively closed and open and the first and second switching means of each of the paths on respective opposite sides of said one path are respectively open and closed, charging of the capacitors connected to said one path takes place and when thereafter the first and second switching means of said one path are respectively open and closed discharge of the capacitors connected to said one path takes place.

2. A multiplexer circuit as claimed in Claim 1, characterised in that said devices of said series of devices are arranged in two groups of interleaved devices.

3. A multiplexer circuit as claimed in Claim 2, characterised in that said devices of a first of said groups alternate in said series with respective devices of a second of said groups.

4. A circuit as claimed in any preceding claim, characterised in that a diode device is connected across the second switching means of each path and provides a conductive path for discharging capacitors connected between the path in which said diode is connected and the paths on respective opposite sides thereof.

5. A circuit as claimed in any preceding claim, characterised in that the first and second switching means are provided on a silicon chip integrated circuit, said switching means comprising transistor switches.

6. A circuit as claimed in Claim 5, characterised in that the transistor switches comprise field effect transistors.

7. A circuit as claimed in any preceding claim, characterised in that the second switching means of each path comprises first and second switching components of which the first switching component provides a by-pass path in parallel with the second switching component during charging of the capacitors connected between the path containing said second switching means and the paths on opposite sides thereof by way of the first switching means of said paths on opposite sides of the path containing said second switching means, whilst the second switching component provides a conductive path for discharging the capacitors connected to the path containing said second switching component after charging thereof by way of the first switching means contained in the same path as said second switching component.

8. A circuit as claimed in Claim 7, characterised in that the first and second switching means are provided on a silicon chip integrated circuit, the first switching means comprising a field effect transistor and the first and second switching components of the second switching means comprising respectively a field effect transistor and a field effect transistor controlling conduction of a bipolar transistor.

9. A circuit as claimed in any preceding claim, characterised in that in each phase of operation the capacitors connected to devices selected for actuation are charged in an initial part of a voltage waveform supplied from the signal generator after which the signal generator is disconnected from the circuit for a further interval of said waveform prior to discharge of the charged capacitors.

10. A circuit as claimed in any preceding claim, characterised in that the signal generator and the parallel electrical paths and the first and second switching means thereof are formed in a silicon chip integrated circuit.

11. A circuit as claimed in any one of Claims 1 to 10, characterised in that logic signal applying means are provided to effect switching into and out of conduction of the first and second switching means.

12. A circuit as claimed in Claim 11, characterised in that the logic signal applying means are adapted to apply signals to the first and second switching means to enable charging of the capacitors of each of the devices selected for actuation for a period dependent upon the actuated or non-actuated status of devices adjacent each of said selected devices.

13. A multi-channel array, electrically pulsed droplet deposition apparatus for depositing liquid droplets upon a surface, comprising a droplet de-

position head formed with electrically active material, a multiplicity of channels for liquid formed in said head and arranged in a plurality of groups, nozzles communicating with the respective channels, longitudinal channel side walls each serving to divide one channel from the next and electrically actuable means for effecting transverse displacement in opposite senses of said longitudinal sidewalls of each channel, said electrically actuable means comprising electrodes in each channel on respective facing surfaces of the longitudinal channel side-walls, conductive means connecting the electrodes in each channel, said electrodes and said longitudinal channel side-walls forming a series of capacitors each consisting of one of said longitudinal channel side walls and the electrodes on opposite sides thereof and a multiplexer circuit for effecting in successive phases of operation actuation of said longitudinal channel walls of selected channels in each of the channel groups, said circuit comprising a series of parallel electrical paths, said capacitors being connected respectively between successive paths of said electrical paths, a signal generator connected across said parallel electrical paths, first and second switching means disposed in each of said paths, and logic signal applying means for effecting conduction of said first and second switching means, so that when the first and second switching means of one path are respectively closed and open and the first and second switching means of each of the paths on opposite sides of said one path are respectively open and closed charging of the capacitors connected to said one path takes place and when thereafter the first and second switching means of said one path are respectively open and closed discharge of said capacitors takes place.

14. A pulsed droplet deposition apparatus as claimed in Claim 13, characterised in that said channels are arranged in a plurality of groups of interleaved channels.

15. A pulsed droplet deposition apparatus as claimed in Claim 14, characterised in that said channels are provided in two groups and the channels of a first of said two groups alternate with respective channels of a second of said groups.

16. A pulsed droplet deposition apparatus, as claimed in any one of Claims 13 to 15, characterised in that the signal generator is adapted during charging of said capacitors to apply a signal to the capacitors of the selected channels which is of relatively slowly increasing voltage and the logic signal applying means are adapted to effect disconnection of the signal generator from the capacitors of said selected channels when a predetermined charge voltage is reached and after an interval to actuate the switching means to effect rapid discharge of the charged capacitors whereby during charging of the capacitors of the selected channels the longitudinal side walls of the said channel are displaced outwardly relatively slowly and during discharge of the capacitors the channel walls are rapidly returned.

17. A pulsed droplet deposition apparatus as claimed in any one of Claims 13 to 16, characterised in that the logic signal applying means are adapted to apply signals to the first and second switching means in each of said parallel paths to which the capacitors of selected channels are connected to enable charging of the capacitors of each selected channel for a period to provide a voltage level thereon dependent upon the selected or non-selected status of adjacent channels and the group containing the selected channels.

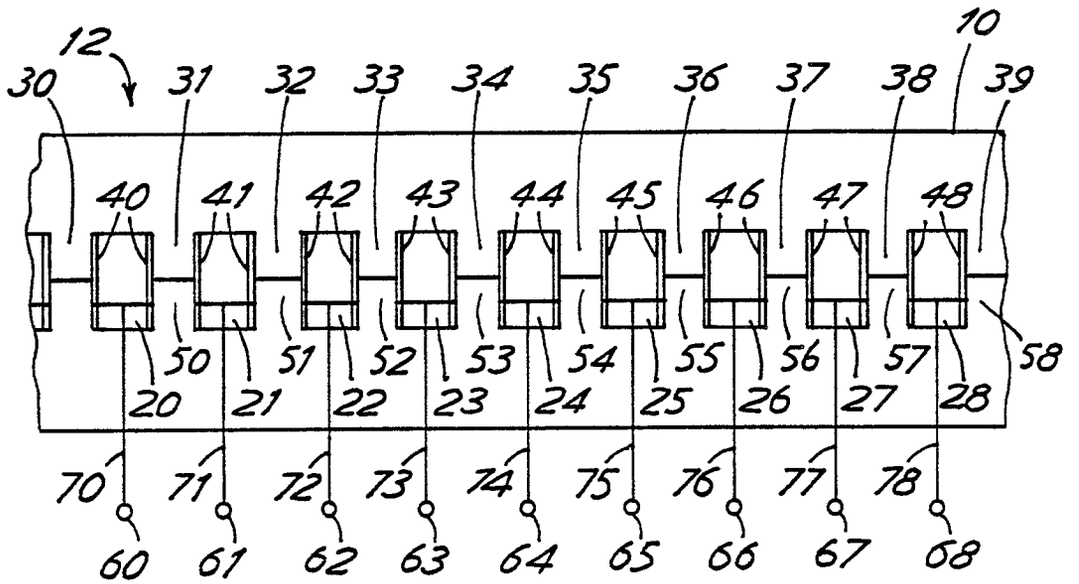
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FIG.1

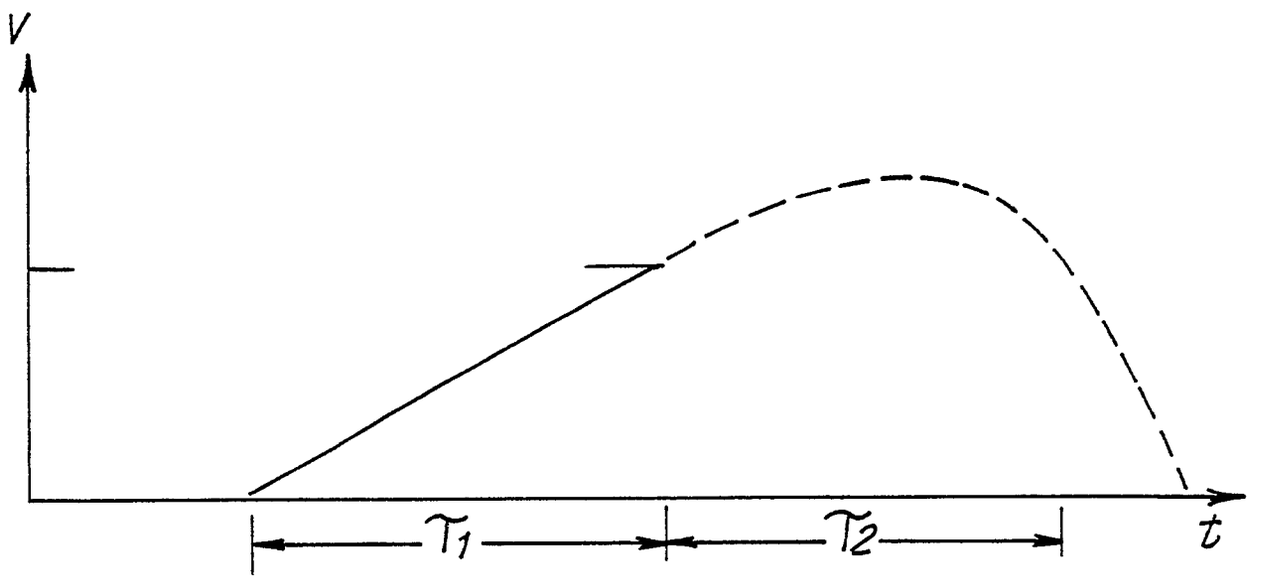
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FIG.4

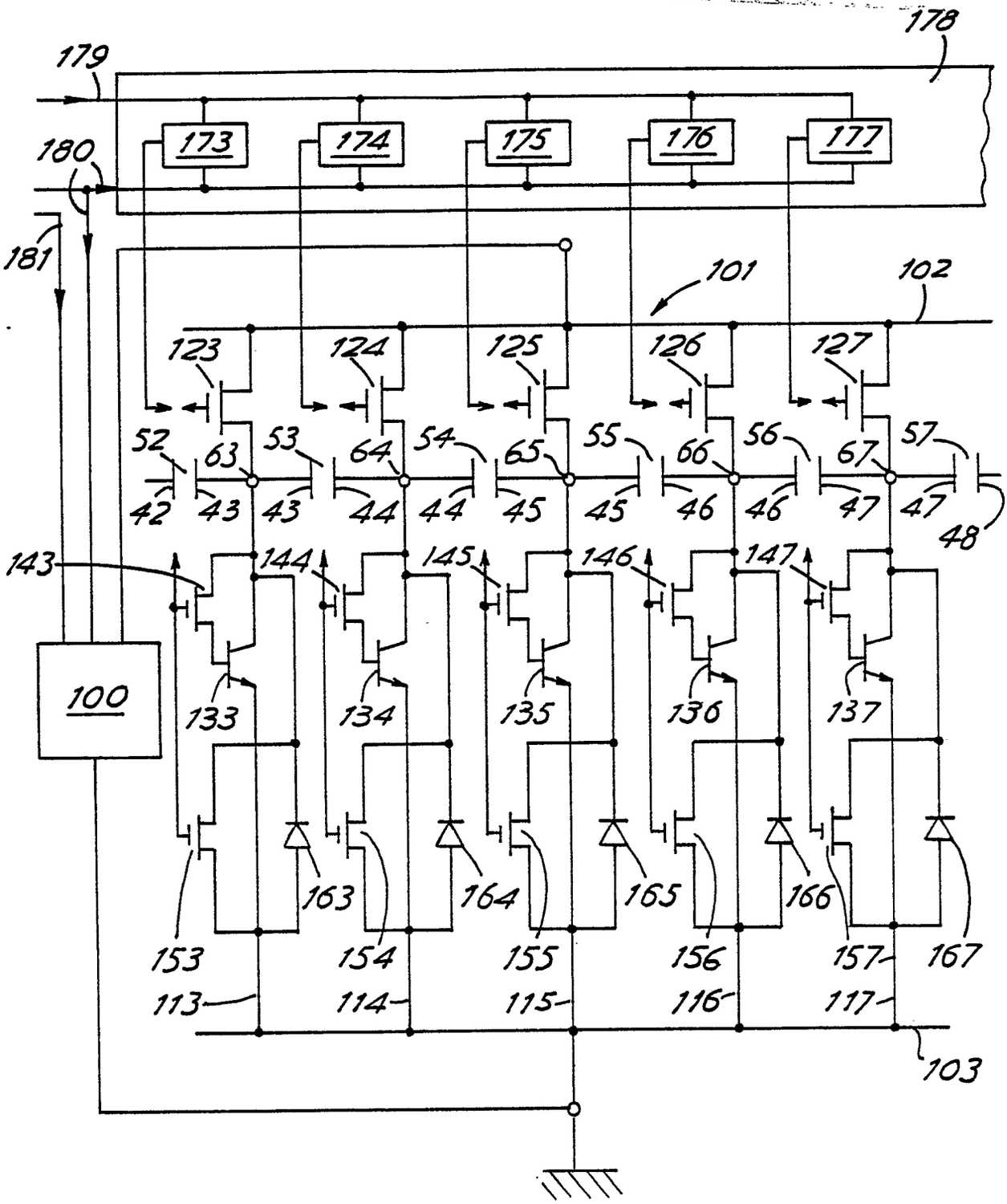
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FIG.2

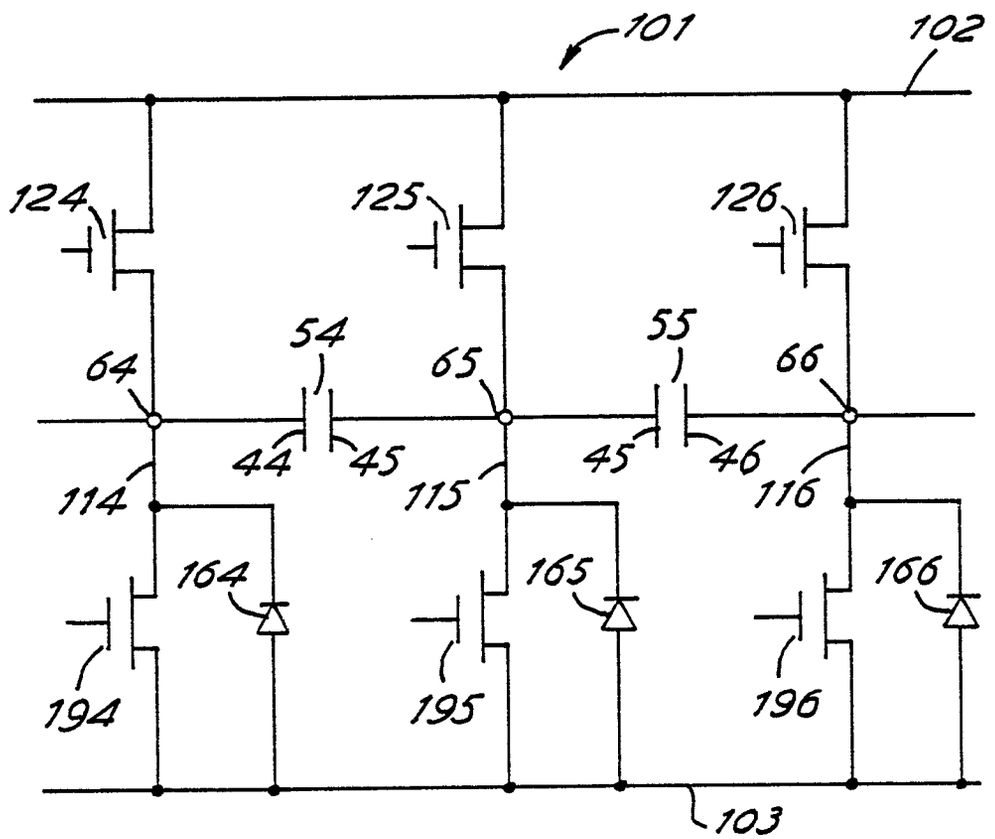

FIG.3