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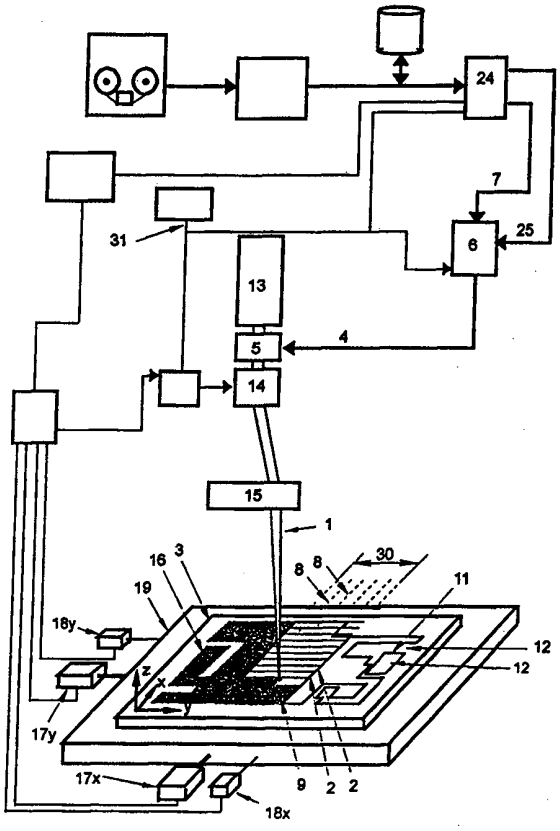
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(54) Title: APPARATUS FOR A LASER WRITER FOR COMPLEX MICROLITHOGRAPHIC PATTERNS WITH A DELAY CIRCUIT

(57) Abstract

The invention relates to a method and an apparatus for producing microlithographic patterns, in particular to the writing of photomasks for and direct writing of computer displays, microelectronic devices, and precision photoetching. It is also applicable to optical devices and a variety of electronic interconnection structures such as multichip modules. Other applications are possible, such as printing and graphics, as well as laser projection displays. More specifically the invention comprises a method and apparatus for writing of lithographic patterns with raster scanning technique comprising the use of an electronic clock to control the modulation of the beam where the placement in the scanning directions of pattern elements is controlled by time delays of at least one clock signal by fractions of a clock period where said clock period is divided into a number of preferably equally spaced delay time values by means of a delay-locked loop (DLL) and a particular delay time value is chosen according to a digital control word.



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Apparatus for a laser writer for complex microlithographic patterns with a delay circuit.

Field of the invention

The invention relates to a method and an apparatus for producing microlithography, in particular to the writing of photomasks for and direct writing of computer displays, microelectronic devices, and precision photo-etching, with the use of a time delay circuit such as is known from European Patent EP 0 467 076, for example. It is also applicable to optical devices and a variety of electronic interconnection structures such as multichip modules. Other applications are possible, such as printing and graphics, as well as laser projection displays.

Background of the invention

There is a development towards an ever-increasing number of features on photomasks, and increasingly sophisticated designs. For both computer displays, consumer TV screens and microelectronic products there is a rapid development towards at the same time larger sizes and smaller elemental cells. The development is most dramatic with semiconductor memories where a photomask could contain a billion elemental geometries or more.

Another issue is the necessity of a small address grid. The writing system for semiconductor masks must be capable of writing features specified in units of 10 nm (nanometers) or less. It has been disclosed in European Patent EP 0 467 076 by the same applicant that a combination of time delays and analog power modulation can be used to achieve an arbitrarily small address grid. The same patent also discloses the use of several beams and parallel data paths to increase the through-put of the writing system.

Naturally there is hereby a need for a very exact and reliable time delay circuit, something which has been

a problem in the prior art which uses integrating delay circuits, creating the delay as the time needed to change an integrating capacitor to a determined level. There is also a problem with synchronization between the delay circuit and the clock pulse generator, and with complicated and time-consuming tuning adjustments, that is necessary in every new installation, and also when there have been changes in the clock rate etc.

Further these known delay circuits are not fast enough in changing the time value, leading to a deterioration of the performance of the apparatus. The known delay circuits are also sensitive to interference.

It is therefore an object with the present invention to provide an apparatus of the above mentioned type with an improved delay circuit.

This object is fulfilled with an apparatus according to claim 1. Other features and advantages with the present invention will be appreciated from the dependent claims, and from the following detailed description of a preferred embodiment of the invention with reference to the attached drawings.

Brief summary of the invention

The present invention relates to a method and apparatus for writing of lithographic patterns with raster scanning technique comprising the use of an electronic clock to control the modulation of the beam where the placement in the scanning directions of pattern elements is controlled by time delays of at least one clock signal by fractions of a clock period. The invention is characterised in that said clock period is divided into a number of equally spaced time values by means of a delay-locked loop and a particular time value is chosen according to a digital control word. Hereby several advantages are obtained, such as no need for tuning adjustments, an automatical adjustment to the clock and stability against interference.

According to a preferred embodiment of the invention the delay circuit comprises N delay elements, each providing an additional delay of 1/N of the clock period, whereby N is digitally adjustable between at least two predetermined values, preferably 50, 60 and 64. Hereby the clock period can be exactly divided by several different numbers, diminishing the problem with rounding errors.

According to another preferred embodiment of the invention the delay circuit comprises N delay elements, where N is a number such that $N = 2^n$ when n is an positive integer, whereby any time period can be digitally represented by a binary word for the number of complete clock periods and a binary word for the additional delay as a number of 1/N fractions of a clock period. Hereby any period of time becomes very easy to state and communicate.

According to another preferred embodiment of the present invention the delay circuit is used for providing an address resolution significantly higher than what is given by the electronic clock, by time delay in the respective clock periods.

According to still another preferred embodiment of the invention the delay circuit is used to delay the input clock signal of the electronic clock for certain logic components, such as components for adjusting the beam relative to other beams in the case of multiple beam writing, or components for fine adjustment of the placement of the whole pattern in the scanning direction.

Brief description of the drawings

Figure 1 shows an apparatus for producing a surface pattern or structure according to the prior art.

Figure 2 shows an embodiment of a modulator driver logic that can be used in the apparatus of fig 1.

Figure 3 shows the delay circuit to be used in the invention according to a prefered embodiment.

Figure 4 shows a time chart illustrating the operation for the delay circuit in fig 3.

Figure 5 shows another embodiment of the delay circuit according to the invention.

Preferred embodiments

Reference will now be made to Fig. 1 showing an apparatus according to the prior art for producing surface patterns or structures on photosensitively coated supports or substrates. In the illustrated embodiment, the substrate 3 is disposed on an object table 19 which is movable in the X- and Y-directions. A writing head with a focusing lens 15 and a deflector device 14 is arranged to be stationary in the X- and Y-directions.

A laser beam source 13 produces a laser beam which is modulated in regard to its power and in particular its intensity by a modulator device 5. The focusing lens 15 focuses on the laser beam and forms a focused laser beam as indicated at 1, which is directed on to the surface of the substrate 3.

For monitoring the positioning of the object table 19, the apparatus has position monitoring devices 18x and 18y which monitor the positioning of the object table 19 in the X- and Y-directions relative to the writing head (deflector device 14 and focusing lens 15). Together with electric motors 17x and 17y, the position monitoring devices 18x and 18y form a servo mechanism which produces the precisely controlled movement of the object table 19.

The servo mechanism produces stripes 30 of a given width when the laser beam 1 scans along the scan lines 2 in the X-direction at a constant speed. When a respective stripe 30 is completed, the X-servo mechanism performs a retrace stroke movement into the starting position and the object table 19 is then moved in the Y-direction by the width of a stripe by the electric motor 17y.

The laser beam from the source 13 is passed through the acousto-optical modulator 5 which is actuated by a

high-frequency modulation drive signal 4. The modulation drive signal 4 is supplied by the modulator driver logic means 6. The intensity or power of the modulation drive signal 4 is controlled by an analog modulation drive signal of a digital-analog converter. The digital-analog converter which is disposed in the modulator driver stage or logic means 6, as shown in Fig. 3, is controlled by a power control signal 7 by way of a storage device which is preferably in the form of a register, for storage of the digital power control word required for producing the control effect.

Generally, the data delivery means includes a clock having a predetermined clock period between clock pulses, so as to establish a regular train of clock pulses. A data processing unit is provided for accepting input data and computing or establishing beam intensity data and beam position data for an edge in the pattern to be written. Both the beam intensity data and the beam position data are established in a digital format. The apparatus also includes as part of the data delivery means a signal processing unit for converting the beam position data to an equivalent time for positioning the laser beam along the scan line during scanning. Particularly, this equivalent time is converted as an integer number of clock pulses plus a fractional remainder. To create a time pulse corresponding to the equivalent time, digital counting means may be provided for generating a timing pulse at a time corresponding to the integer number of clock pulses and a time delay circuit may be provided for incurring to the timing pulse a time delay equal to the fractional remainder. Once the corresponding time pulse is created, a circuit may be used for setting the modulator input signal to the digital beam intensity data at the arrival of the timing pulse.

Reference will be made at this point to Fig. 2 showing a preferred embodiment of the modulator drive logic means 6 described above with reference to Fig. 1. It has

two storage devices for bit words, in the form of registers 605 and 608. The register 605 is loaded with intensity or power data 7 coming from the data delivery device 24 shown in Fig. 1. The register 608 is loaded with position or delay data 25 which also come from the data delivery device 24. That takes place on the basis of a transition caused by the clock signal 31. In that arrangement, a digital-analog converter 606 is also operated by power data previously stored in the storage device 607. It may also be in the form of a register. A digitally controlled delay circuit 609 transfers the clock signal 31 to its output side, with a delay which depends on the data stored in the register 608. After that delay the active edge of the clock signal is supplied at the output 610 of the delay circuit 609. The value stored in the register 605 is loaded into the register 607 and passed to the input side of the digital-analog converter 606. After an internal delay in the digital-analog converter 606, a fresh analog power control signal 4 occurs at the output of the modulator driver stage of the modulator device 5 (fig. 1).

In the prior art the delay circuits were digitally controlled analog delay circuits. These analog delay circuits have several drawbacks. For example the minimum time step is comparatively large, there is a strong need for individual adjustments to the clock, the latency period is significantly large, whereby there is a need for several delay circuits working by turns, there is a large sensitivity for external disturbances and the speed is very limited.

In fig 3 there is shown a delay circuit according to the present invention. The delay circuit comprises a delayed-locked-loop, which in turn comprises N serially connected delay elements 301, where N is an integer larger than two. Each delay elements delays a reference signal from the clock, with a quantum of time. This quantum of time is preferably the same for all the elements,

i.e. 1/N of a clock period. Naturally the delay circuit can also comprise several delayed-locked loops.

The circuit also comprises a phase comparator 302 connected to the output of the last delay element for receiving the routed delayed signal and the reference signal from the clock. Thereby the phase comparator 302 generates a control signal indicative of a difference between a phase of said routed delay signal and a phase of said reference signal. The output of the phase comparator is connected to said delay elements for transferring the control signal to the delay elements whereby each of the delay elements adjusts such that the phase of said reference signal is synchronized with the phase of said routed delay signal. That is, the delay circuit comprises a feedback system which automatically adjusts the amount of delay in each delay step.

Circuits using the delayed-locked-loop technique is known from e.g. US patent 4 338 569. These known circuits have been used in completely different areas, though: adjustment of clock skew and time measurements (mainly in the area of nuclear physics and the like).

The delay circuit of the invention also comprises a selecting part, preferably comprising a multiplexer 303 being connected to the delay elements for receiving the delayed signals generated by the delay elements 301 and to control the output of the delay circuit according to the desired fractional remainder.

To the input of the multiplexer 303 are connected the output signal from the respective delay elements. This is preferably accomplished with NAND-gates 304, such that the signal before and after each delay element 301 are connected to a NAND-gate 304, the output of which is forwarded to the multiplexer 303. In this way the input signals to the multiplexer 303 are very short pulses.

The signals between the different delay elements are illustrated in the time chart in fig 4.

The multiplexer also have a control word as input, and according to this control word the correct output is chosen. The multiplexer according to the invention preferably have a disable function, whereby a disable signal at a disable input can prevent any signal at the output. This is important in order to suppress a delay signal from the delay circuit, to e.g. prevent delayed signals from entering the next clock period, and so forth.

The output from the multiplexer 303 is preferably forwarded through a pulse stretcher 305. The pulse stretcher makes the output pulses from the delay circuit longer in time. This reduces the sensitivity to noise.

The delay value can be dynamically set by a delay control input (control word) to any value between 0 and N-1. N is preferably a number such that $N = 2^n$ where n is an positive integer. Hereby any time period can be digitally represented by a binary word for the number of complete clock periods and a binary word for the additional delay as a number of 1/N fractions of a clock period.

Further, N is preferably controlled by an input port and can be optionally set to any of the values 50, 60 or 64. The set input is not shown in picture 1. Hereby the clock period can be exactly divided by 2, 3, 4, 5, 6, 8, 10, 12, 15, 16, 20, 25, 30, 32, 50, 60 and 64. Possibly the value can also be set to 72, and thereby provide for an exact division by 9, 18, 24, 36 and 72. This is of great importance in avoiding rounding errors. Other values that can be used for N are: 25, 30, 32, 36, 40, 72, 80, 100, 120 and 128. Still further values are naturally possible, as long as they provide for an exact division by numbers that are useful for the intended application, and preferably several different such numbers.

The circuit is preferably designed with Emitter Coupled Logic (ECL) technology.

In fig 5 there is shown an alternative embodiment of the delay circuit according to the invention. The delay circuit of this embodiment also comprises a delay-locked

loop with serially connected delay elements 301 and a phase comparator 302. However, the delay circuit according to this embodiment comprises a second set of serially connected delay elements 501, whereby the control signal from the phase comparator 302 is not only sent back to the delay elements 301 in the first set but also to the delay elements 501 in the second set. With this arrangement the delay elements 501 in the second set will have the same delay time values as the delay elements 301 in the first set (e.g. 2 ns per element). With this embodiment the first set may have a first input, IN1, and the second set another input, IN2. Hereby there is a possibility to delay the second input signal, which may be asynchronous with the first input signal (e.g. the clock signal), with delay time values that are automatically adjusted to the first input signal.

The delay circuit according to the invention provides several advantages over the prior art, such as:

- more stable and robust against interference;
- no need for tuning adjustments;
- automatically adjusts to the clock;
- can be made very compact;
- digitally controlled division;
- higher clock frequency;
- no latency or waiting periods in e.g. capacitors.

For example, a clock with 50 Mhz provide a clock period T = 20 ns. If this period is to be divided by 60, the result is 333 ps per step. An expected deviation for the circuit according to the invention is about +/- 170 ps, compared to +/- 1000 ps for analog circuits. This clearly illustrates the diminished need for tuning adjustments with the circuit according to the invention.

The delay circuit of the invention accordingly provides a very exact division of the clock pulses, thereby producing a very exact time delay. The circuit also adapts to the clock signal, and is therefore always synchronized with the clock.

The delay circuit described above may also be used for other purposes in the writing of lithographic patterns with raster scanning technique. The delay circuit may be used to delay the input clock signal of the electronic clock for certain logic components, such as components for adjusting the beam relative to other beams in the case of multiple beam writing, or components for fine adjustment placement of the whole pattern in the scanning direction.

The terms and expressions which have been employed in the foregoing specification are used therein as terms of description and not of limitation, and there is no intention in the use of such terms and expressions of excluding equivalents of the features shown and described or portions thereof, it being recognized that the scope of the invention is defined and limited only by the claims which follow.

CLAIMS

1. Method for writing of lithographic patterns with raster scanning technique comprising the use of an electronic clock to control the modulation of the beam where the placement in the scanning directions of pattern elements is controlled by time delays by fractions of a clock period, c h a r a c t e r i s e d in that said clock is used to generate a number of preferably equally spaced delay time values by means of a delay-locked loop and a particular delay time value is chosen according to a digital control word.

2. Method according to claim 1, where the digital control word is changed dynamically during the writing of a pattern.

3. Method according to claim 1 or claim 2, c h a r a c t e r i s e d in that

said time delay circuit comprises a delayed-locked-loop, comprising:

at least N serially connected delay elements, where N is an integer larger than two, each delaying a reference signal from said clock, with a quantum of time, and

a phase comparator connected to the output of the N:th delay element for receiving the routed delayed signal and the reference signal, for generating a control signal indicative of the difference between a phase of said routed delay signal and a phase of said reference signal, and feedback means for transferring the control signal to the delay elements whereby each of the delay elements adjusts such that the phase of said reference signal is synchronized with the phase of said routed delay signal.

4. Method according to one of claims above, c h a r a c t e r i s e d in that said time delays are generated by a number of serially connected delay elements controlled by the control signal in the delayed-locked loop.

5. Method according to claim 3, c h a r a c t e r i s e d in that the clock signal is connected to serially connected delay elements controlled by said control signal and selecting a number of delay elements to delay said clock signal to the output according to said digital control word.

6. Method according to one of the claims above, c h a r a c t e r i s e d in that the delay circuit comprises N delay elements, each providing an additional delay of 1/N of the clock period, whereby N is digitally adjustable between at least two predetermined values, preferably chosen among the values 25, 30, 32, 36, 40, 50, 60, 64, 72, 80, 100, 120 and 128.

7. Method according to one of the claims above, c h a r a c t e r i s e d in that the clock period is divided in N increments (steps), where N is a number such that $N = 2^n$ when n is a positive integer, whereby any time period can be digitally represented by a binary word for the number of complete clock periods and a binary word for the additional delay as a number of 1/N fractions of a clock period.

8. Method according to one of the claims 1 to 7, c h a r a c t e r i s e d in that the delay circuit is used for providing an address resolution for pattern elements significantly higher than what is given by the electronic clock, by time delay in the respective clock periods.

9. Method according to one of the claims 1 to 7, c h a r a c t e r i s e d in that the delay circuit is used to delay the input clock signal of the electronic clock for certain logic components.

10. Method according to claim 9, c h a r a c t e r i s e d in that the logic components are components for adjusting the beam relative to other beams in the case of multiple beam writing.

11. Method according to claim 9, c h a r a c t e r i s e d in that the logic components are components for

fine adjustment placement of the whole pattern in the scanning direction.

12. An apparatus adapted for writing of lithographic patterns with raster scanning technique, comprising an electronic clock and a time delay circuit, c h a r a c t e r i s e d in that the time delay circuit is a delayed-locked-loop circuit, driven by the said clock, whereby the output from the delay circuit is determined by input data.

13. An apparatus according to claim 12, whereby it is intended for writing of complex patterns on a light sensitive surface by scanning at least one, by a modulator modulated, laser beam in parallel scan lines while moving along scan stripes in a direction perpendicular to the scan lines, the apparatus comprising:

data delivery means for controlling the input of said modulator while the laser beam is scanning, wherein the data delivery means includes

a clock with a predetermined clock period between the clock pulses;

a data processing unit for receiving input data and computing beam intensity data and beam position data each in digital format, for an edge in the pattern,

a signal processing unit for converting the beam position data to an equivalent time for positioning the laser beam along the scan line during scanning, and converting this equivalent time to an integer number of clock pulses plus a fractional remainder, and

a time delay circuitry to delay transition in the modulated data, producing said fractional remainder, for higher address resolution than corresponding to the data clock pulses.

14. An apparatus according to claim 12 or 13, c h a r a c t e r i s e d in that

said time delay circuit comprises a delayed-locked-loop, comprising:

N serially connected delay elements, where N is an

integer larger than two, each delaying a reference signal from said clock, with a quantum of time,

a phase comparator connected to the output of the N:th delay element for receiving the routed delayed signal and the reference signal, for generating a control signal indicative of a difference between a phase of said routed delay signal and a phase of said reference signal, and being feedback connected to said delay elements for transferring the control signal to the delay elements whereby each of the delay elements adjusts such that the phase of said reference signal is synchronized with the phase of said routed delay signal,

a multiplexer being connected to the delay elements for receiving the delayed signals generated by the delay elements and to control the output of the delay circuit according to the desired fractional remainder.

15. An apparatus according to one of claim 12-14, c h a r a c t e r i s e d in that said time delays are generated by a number of serially connected delay elements controlled by the control signal in the delayed-locked loop.

16. An apparatus according to claim 14, c h a r a c t e r i s e d in that the each delaying element delays the reference signal from said clock, with a quantum of time being 1/N of a clock period.

17. An apparatus according to one of claim 12-16, c h a r a c t e r i s e d in that the delay circuit comprises N delay elements, each providing an additional delay of 1/N of the clock period, whereby N is digitally adjustable between at least two predetermined values, preferably chosen among the values 25, 30, 32, 36, 40, 50, 60, 64, 72, 80, 100, 120 and 128.

18. An apparatus according to one of claim 12-17, c h a r a c t e r i s e d in that the delay circuit is produced with ECL (Emitter Coupled Logic) technology.

19. An apparatus according to one of claim 12-17, c h a r a c t e r i s e d in that the delay circuit is

produced with CMOS (Complementary Metal-Oxide Semiconductor) technology.

20. An apparatus according to one of claim 12-19, c h a r a c t e r i s e d in that the apparatus provides an address resolution in pattern elements significantly higher than what is given by the electronic clock by means of a time delay from said delay circuit in the respective clock periods.

21. An apparatus according to one of claim 12-19, c h a r a c t e r i s e d in that the apparatus is a multi-beam writer, where the delay circuit is adapted to delay the input clock signals of the electronic clock for adjusting a beam relative to the other beams.

22. An apparatus according to one of claim 12-19, c h a r a c t e r i s e d in that the delay circuit is used to delay the input clock signals of the electronic clock for fine adjustment of the placement of the whole pattern in the writing direction.

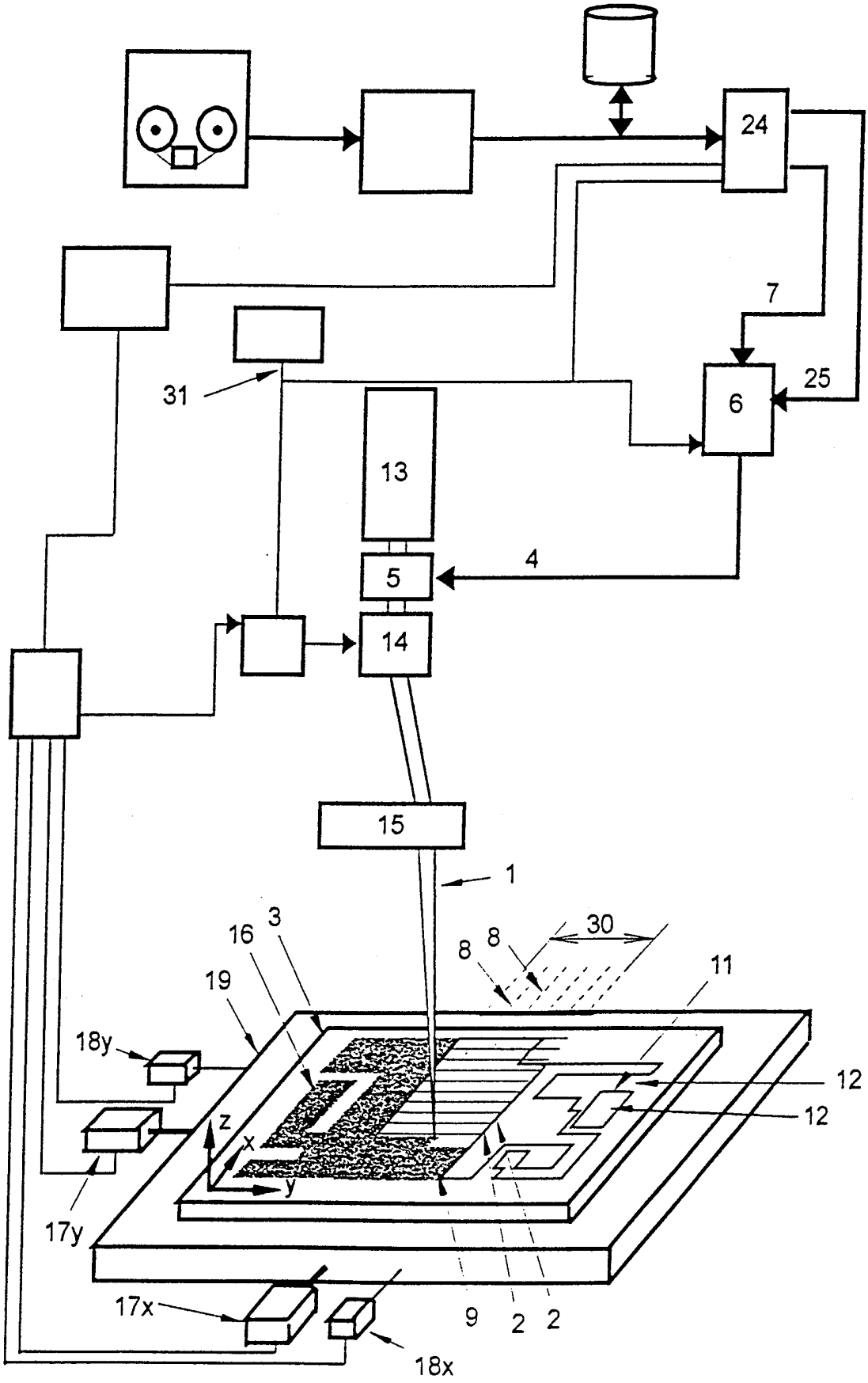

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Fig. 1

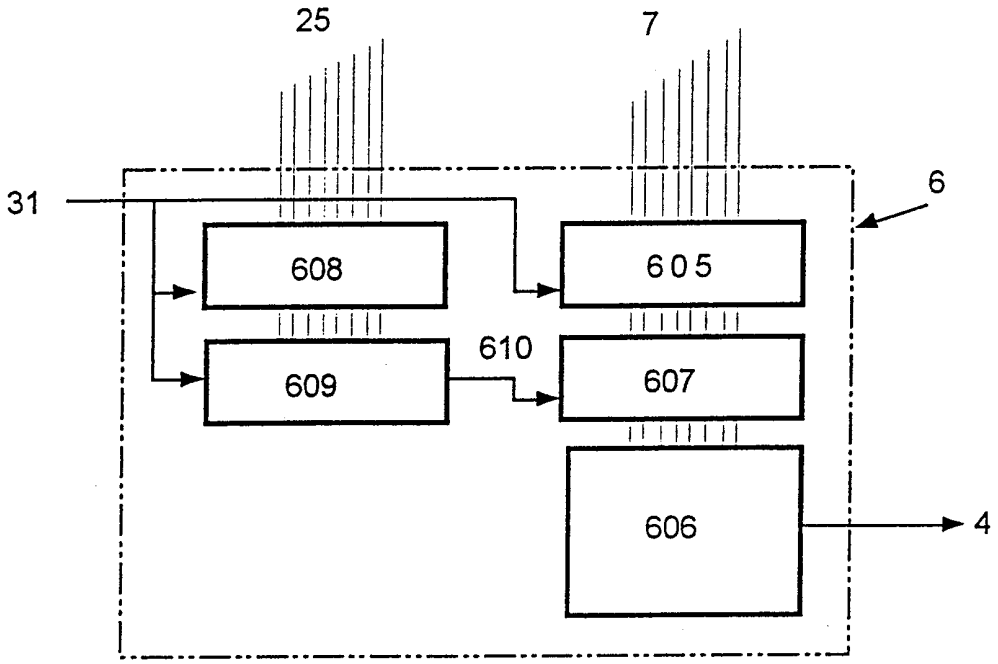


Fig. 2

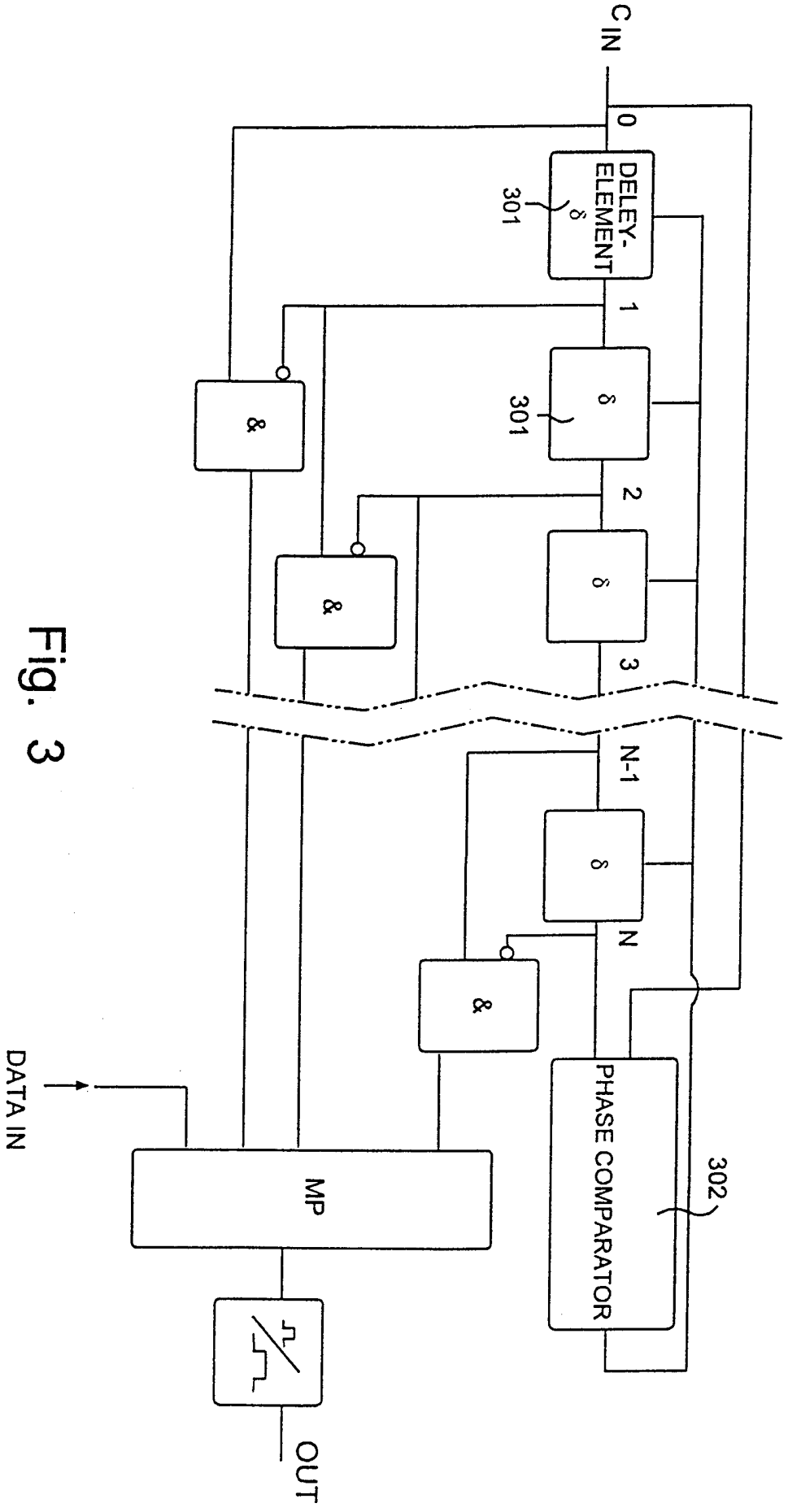

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Fig. 3

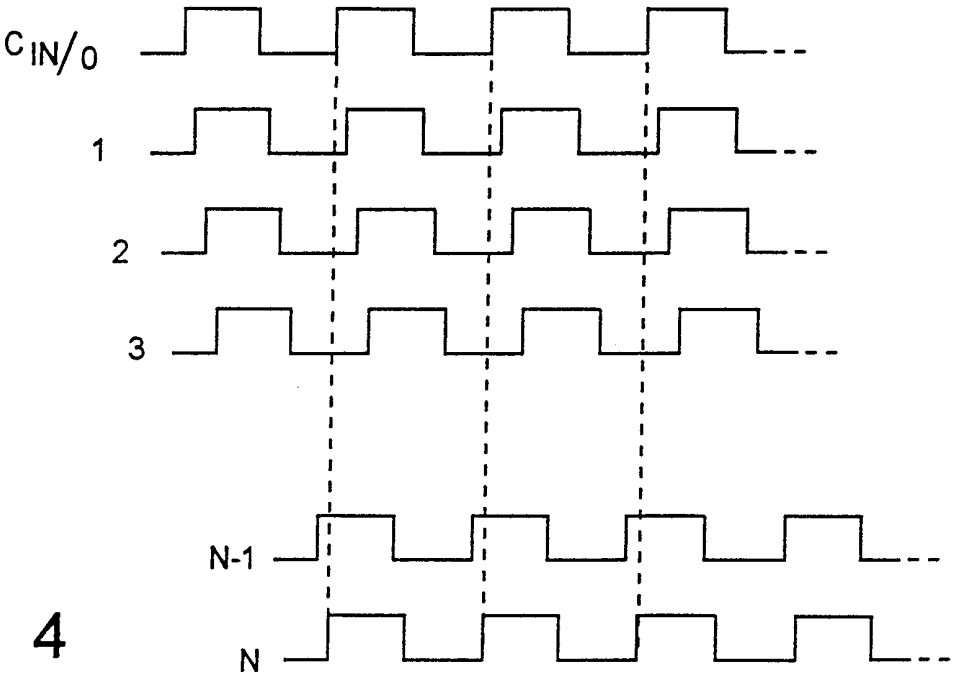


Fig. 4

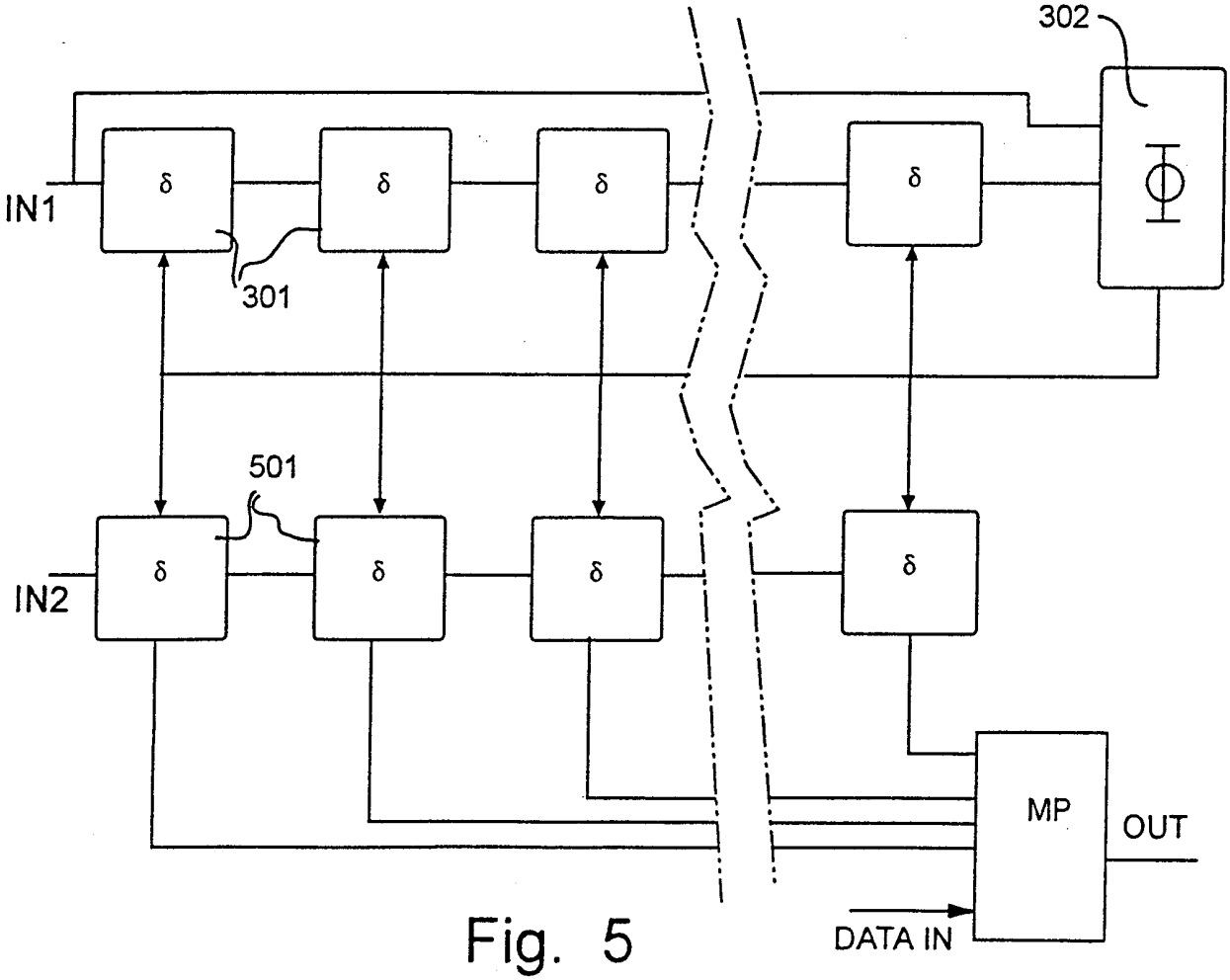


Fig. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 98/01835

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: G03F 7/20, H04N 1/04
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: G03F, H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

QUESTEL: EDOC, WPIL, JAPIO; DIALOG: DIALINDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4549222 A (GIUSEPPE FOGAROLI ET AL), 22 October 1985 (22.10.85), column 4, line 55 - column 5, line 57, figures 1,3 --	1-22
A	US 5635976 A (ANDERS THUREN ET AL), 3 June 1997 (03.06.97), column 8, line 7 - column 11, line 58, figures 3,6 -- --------	1-22

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
18 January 1999	27 -01- 1999
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Bengt Christensson Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

Information on patent family members

01/12/98

International application No.
PCT/SE 98/01835

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4549222 A	22/10/85	EP 0088555 A,B	14/09/83
		JP 1779507 C	13/08/93
		JP 4063584 B	12/10/92
		JP 58195361 A	14/11/83
US 5635976 A	03/06/97	NONE	