United States Patent

Hicks

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[54] SUBSTRATE BONDING BUMPS FOR LARGE SCALE ARRAYS

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[73] Assignee: **The United States of America as represented by the Secretary of the Navy**

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[21] Appl. No.: **848,448**

[52] **U.S. Cl.** ..... **117/212**, 117/38, 118/505, 317/234 M

[51] **Int. Cl.** **B44d 1/52**

[58] **Field of Search** 117/212, 38, 107; 317/234, 317/15.3; 118/504, 505

[56] **References Cited**

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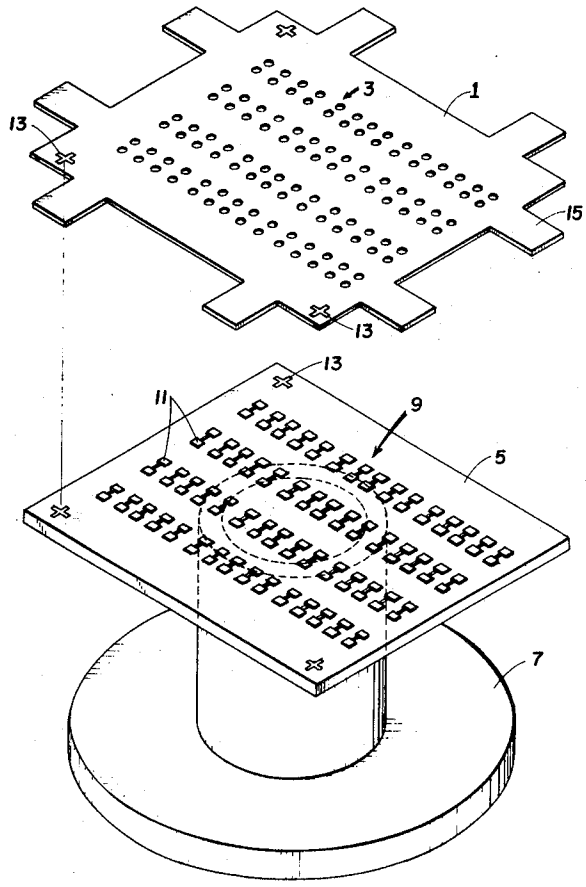
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[57] **ABSTRACT**

A method for producing reliable bonding bumps on large-scale array substrates and hybrid add-on components, the present invention is compatible with a wide variety of microcircuit components. Generally, the method envisions fabrication of bonding bumps by thin-film vacuum deposition through a mechanical mask. In particular, a first metal is deposited on a substrate to a desired thickness whereupon said first metal is then codeposited with a second metal. The bump is completed with the sole deposition of the second metal. A bump thus produced may be further processed to produce a "-solder-dipped bump" or may be used in the thin-film state for component mounting.

4 Claims, 12 Drawing Figures



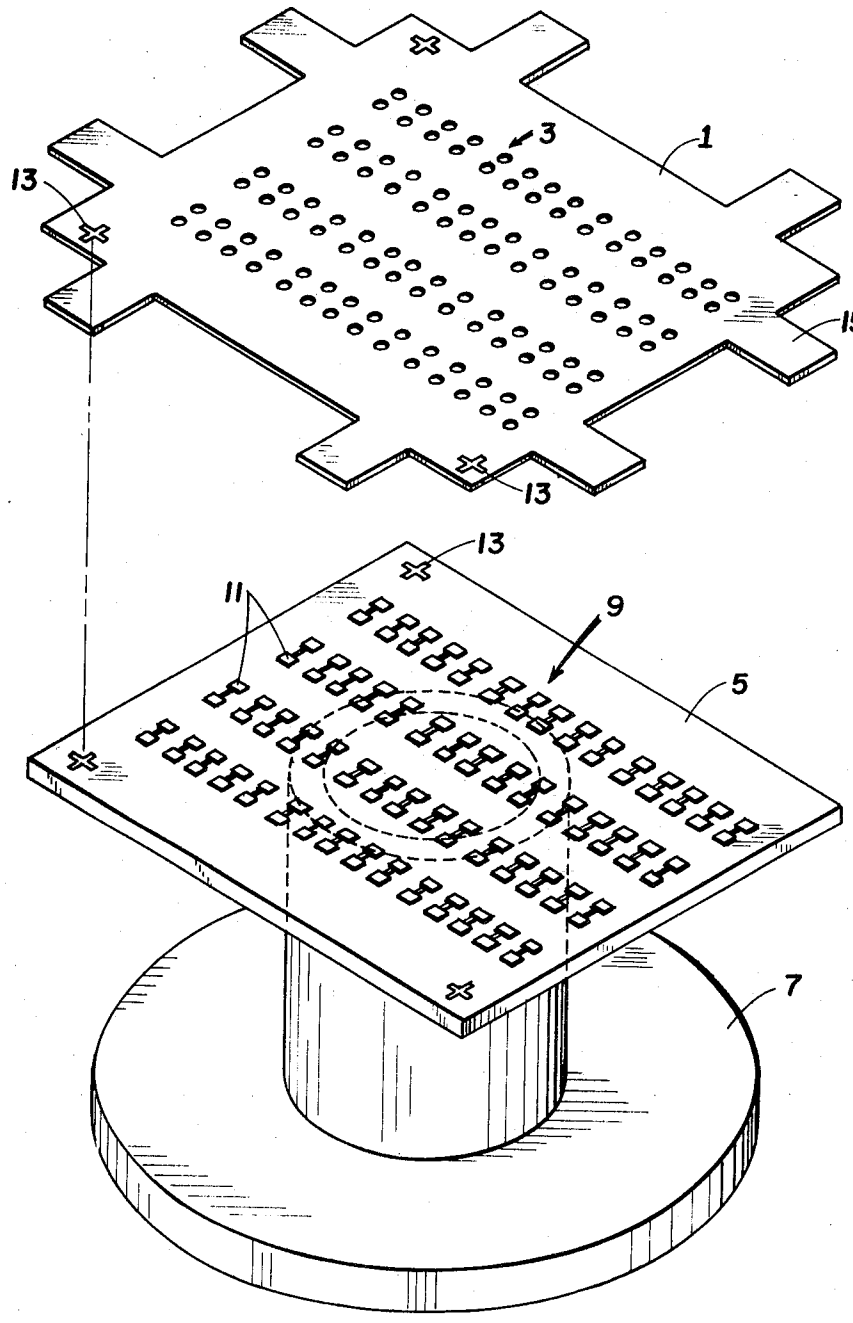


FIG. 1

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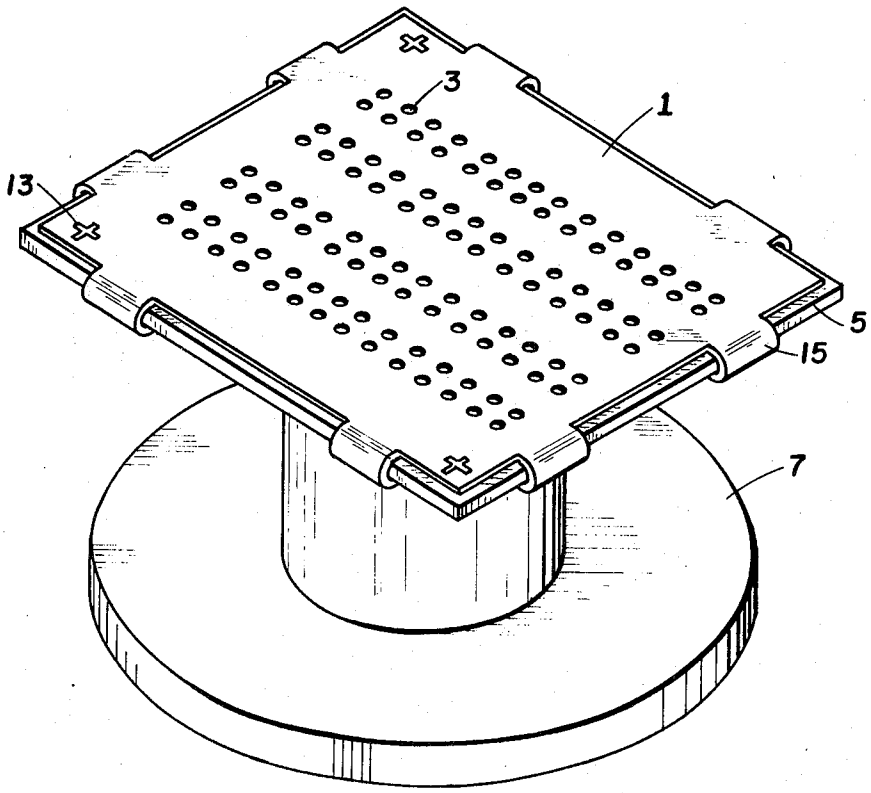
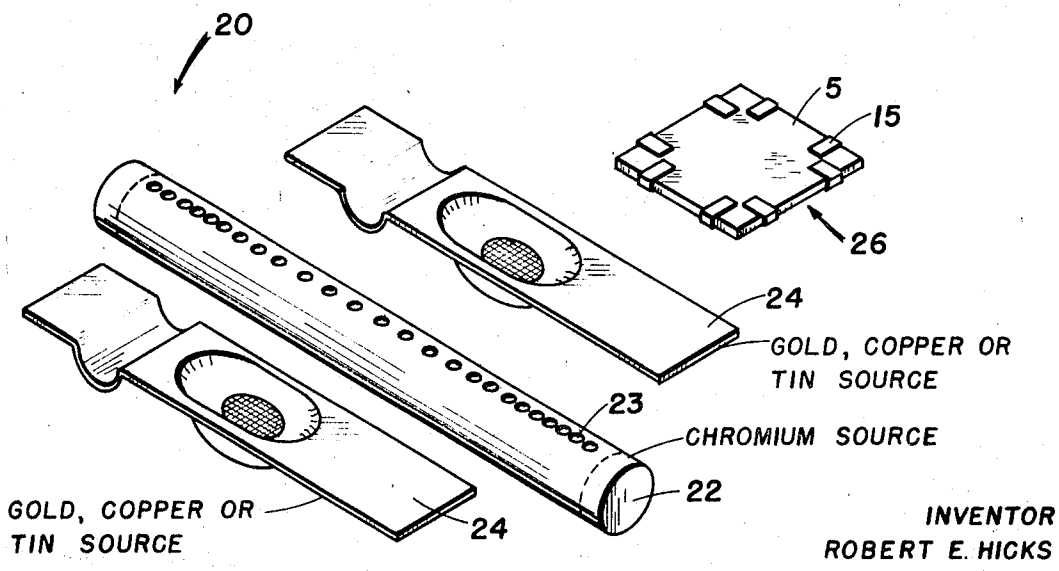


FIG. 2



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FIG. 3

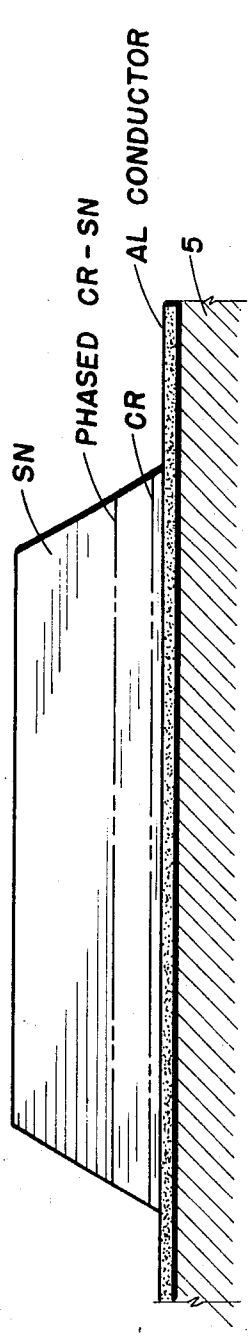


FIG. 4

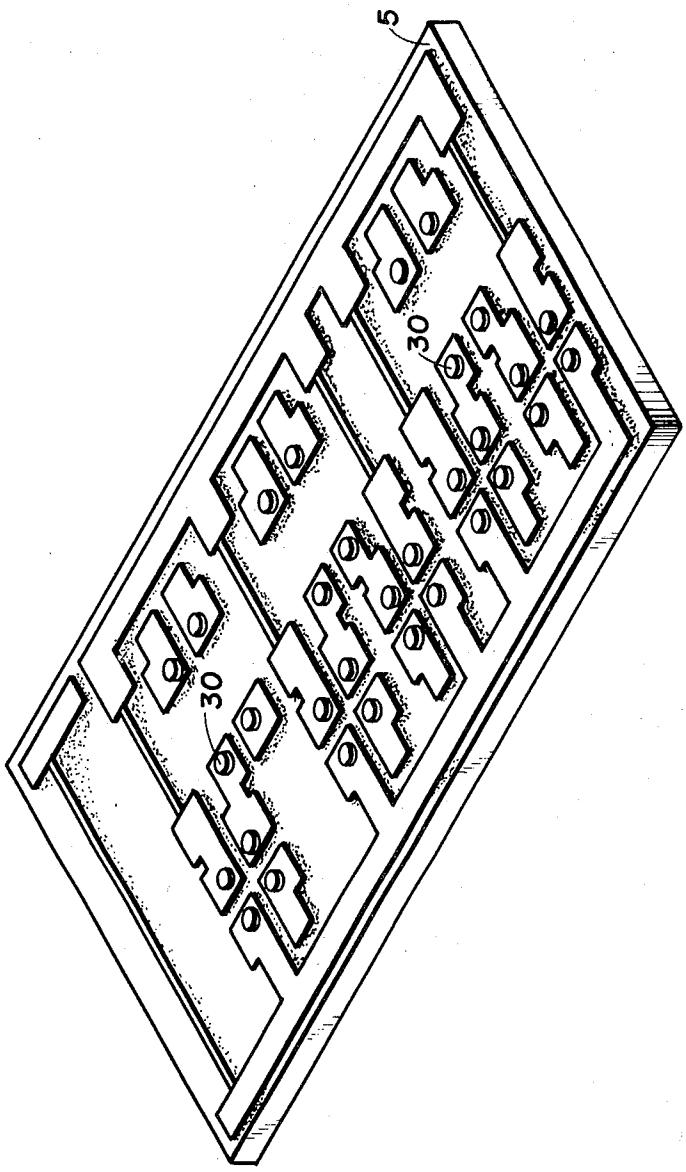


FIG. 5

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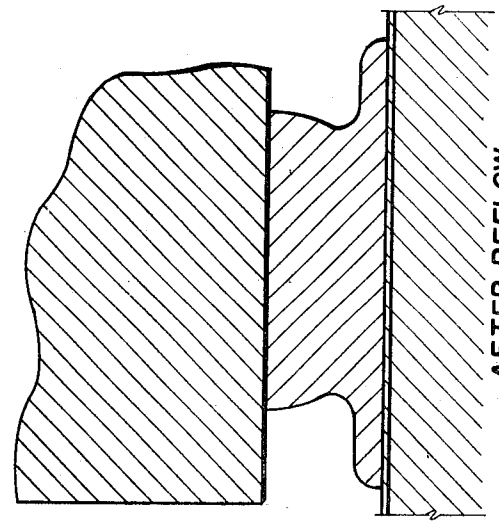


FIG. 6b

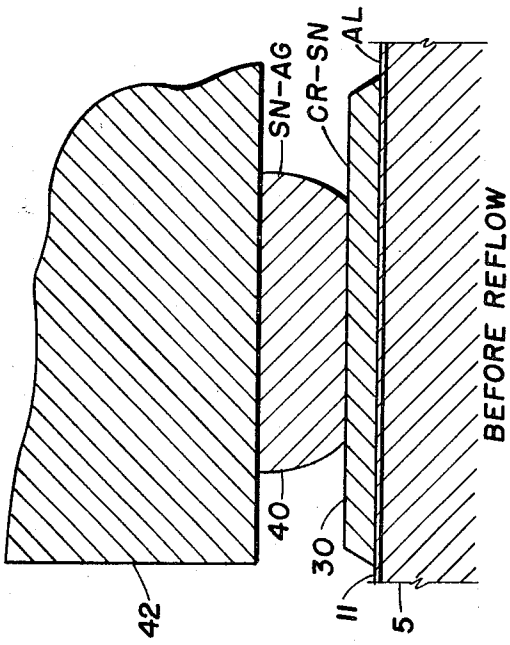


FIG. 6a

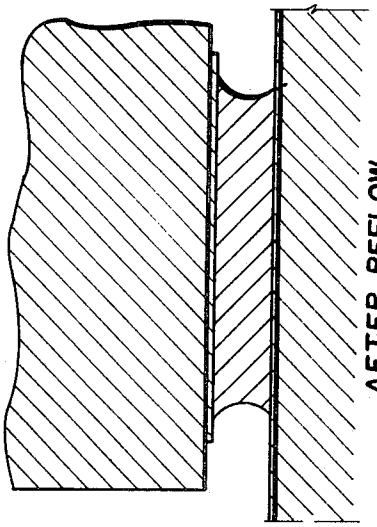


FIG. 7b

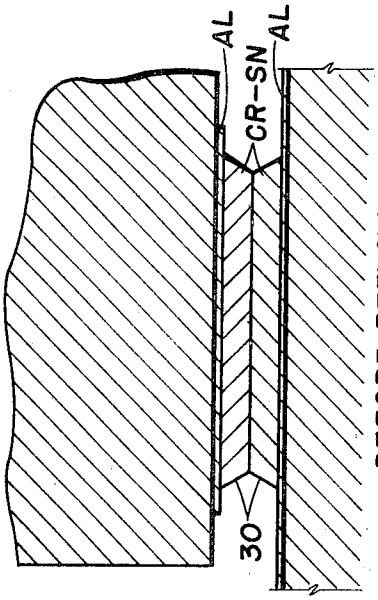


FIG. 7a

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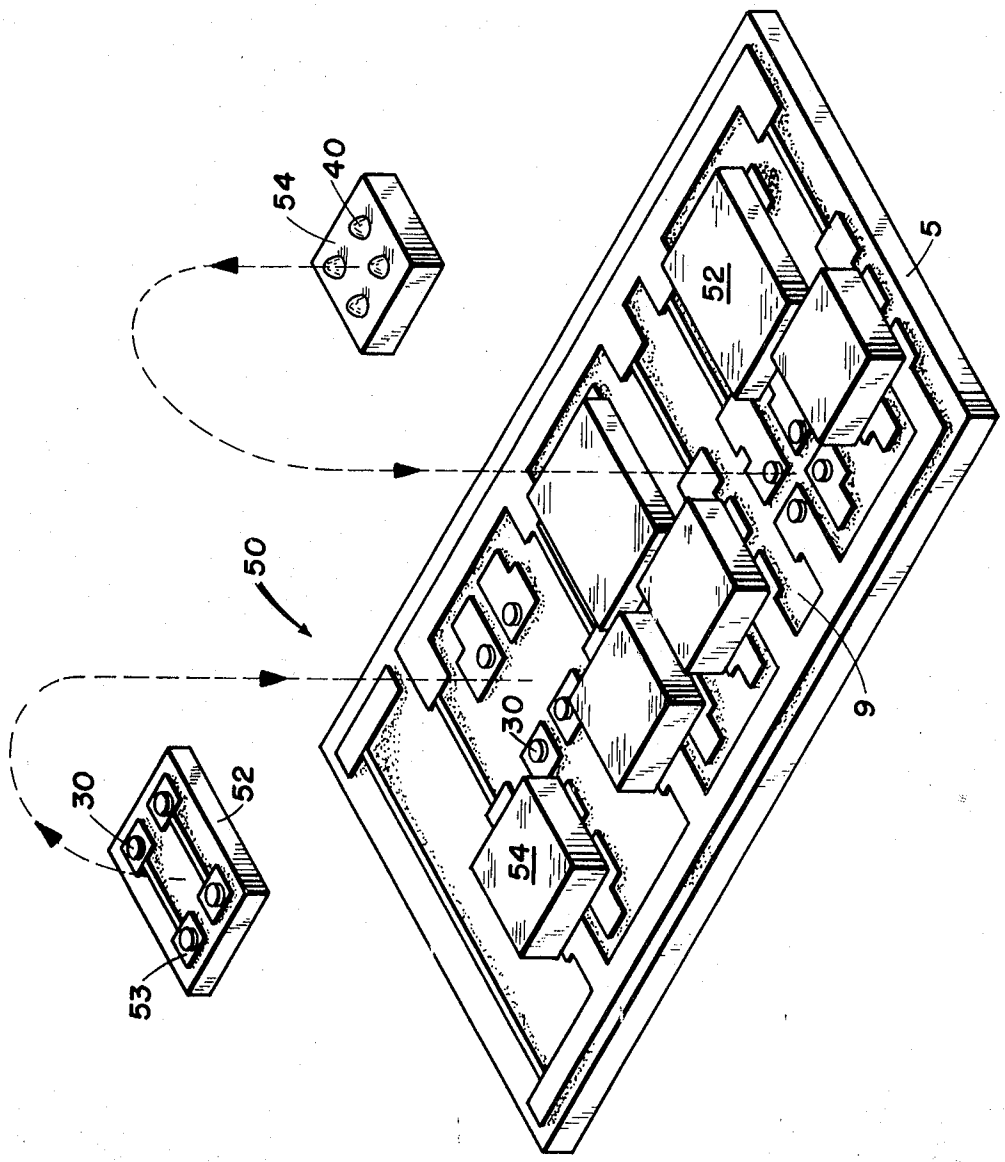


FIG. 8

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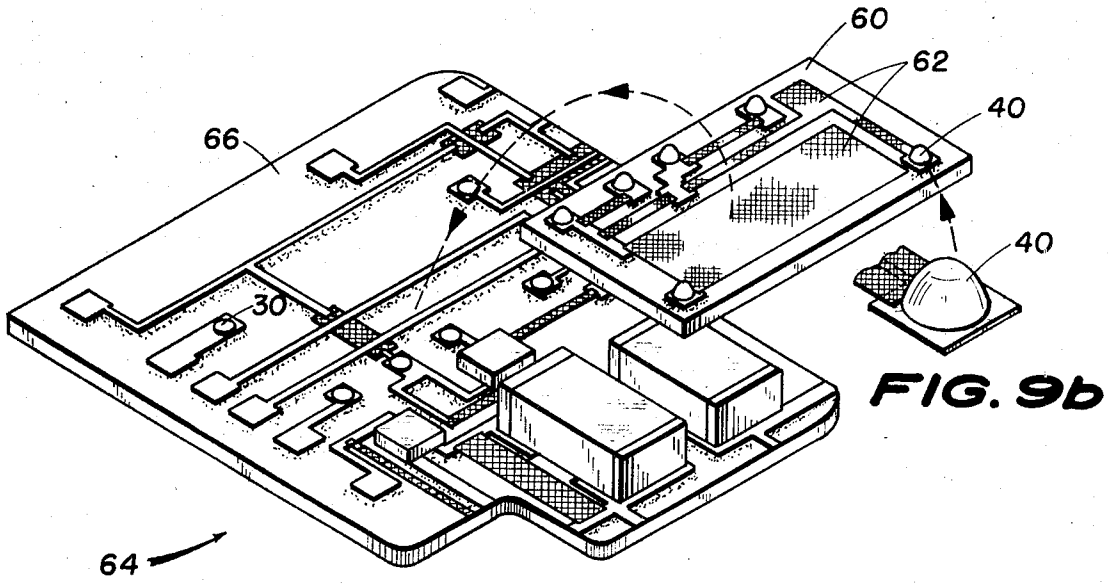


FIG. 9b

FIG. 9a

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SUBSTRATE BONDING BUMPS FOR LARGE SCALE ARRAYS

BACKGROUND AND SUMMARY OF THE INVENTION

Continuing developments in the field of microelectronic packaging techniques and materials applications have produced a variety of hybrid circuit designs. Recent trends favor elimination of bulky structures, flying leads, and high-temperature assembly processes. Progress has been made toward large-scale arrays with "face-down" bonded components having bonding bumps or beam leads amenable to assembly at room temperature. Restricting this progress has been the limited availability of hybrid add-on components with reliable bonding bumps. Thus, the present invention will be seen to provide methods for producing reliable bonding bumps which allow array assembly at room temperature.

Face-down bonding of hybrid components is, of course, one of a number of methods useful to fabricators of large-scale arrays. By providing bonding bumps on the array substrate rather than on the individual component, a significant step in adapting the large-scale array to an almost endless number of circuit applications is taken. In order to take full advantage of the wide selection of add-on components now available, a reliable method of face-down bonding which is universally compatible with any or preferably all of these components must be provided. Such a method should be a room temperature procedure, thereby allowing components having critical requirements to be packaged without degradation.

The invention envisions production of bonding bumps on large-scale array substrates by thin-film vacuum deposition of suitable metals. Deposition is effected through a mechanical mask which allows a desired bump pattern to be deposited onto the substrate. Generally, a flat thin-film metallic bump is produced which may be used in the thin-film state for hybrid array assembly or which may be submitted to a solder dip process to produce a generally hemispherical dipped bump. According to the several embodiments of the method, the thin-film bump is preferably comprised of a phased metallized gradient structure, fabrication of the bumps occurring by the sequential singular and simultaneous deposition of at least two different metals.

It is therefore a primary object of the invention to provide methods for producing reliable bonding bumps for large-scale array fabrication.

It is also an object of the invention to provide a reliable method for fabricating large-scale arrays at room temperature.

It is a further object of the invention to provide bonding bumps for large-scale arrays and which comprise a phased metallized gradient structure.

Further objects and advantages will become more readily apparent in light of the description of the preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an exploded perspective of the substrate and mask before attachment;

FIG. **2** is a perspective of the substrate-mask assembly mounted on a vacuum pedestal;

FIG. **3** is a perspective showing generally the relationship of the substrate-mask assembly to the vacuum evaporation source during metallic deposition;

FIG. **4** is a schematic in section of a thin film bonding bump produced by one embodiment of the present method;

FIG. **5** is a perspective of a typical substrate having bonding bumps disposed at particular locations on a conductor pattern on the substrate;

FIGS. **6***a* and **6***b* are detail sections illustrating bonding procedures joining a dipped bump to a thin film bump;

FIGS. **7***a* and **7***b* are detail sections illustrating bonding procedures joining two thin film bumps;

FIG. **8** is a perspective illustrating hybrid microcircuit component mounting to a substrate by means of bonding bumps produced according to the present method; and

FIGS. **9***a* and **9***b* are perspectives illustrating a particular hybrid packaging arrangement in which bonding bumps produced by the present method are useful, FIG. **9***b* in particular depicting an enlarged view of a solder dipped bump.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a method for producing bonding bumps on a substrate, the method generally comprising the steps of:

1. affixing a patterned mask to the substrate onto which bonding bumps are to be placed; and
2. depositing metallic conductive material through the mask and onto the substrate.

The general method encompasses a number of embodiments, particularly including:

1. the deposition of copper onto a conductive layer previously located on the substrate:
2. the three-step deposition of at least two metallic conductive materials onto the substrate; the first step comprising deposition of a first metal to a desired thickness, the second step comprising codeposition of the first metal and a second metal, and the third step comprising deposition of the second metal only, the process producing a phased metallized gradient structure; and,
3. the production of a solder dipped bump by subjecting the bumps produced in (1) and (2) immediately above to a solder dip bath.

It can be seen from the above that production of reliable bonding bumps is best accomplished through the use of thin films which are preferably vacuum deposited. A bump pattern may be produced on a substrate or on a microelectronic component by vacuum deposition techniques. The methods disclosed herein are preferably effected by use of a mechanical mask which establishes a precise geometric pattern for the bump locations. A suitable mask, such as is seen at **1** in FIG. **1**, has a bump pattern **3** comprising holes through which deposition of metal occurs. The desired pattern **3** is produced by standard photolithographic processes which are commonly used to define substrate metallization geometries. Although the bumps to be produced by the mask **1** of FIG. **1** are seen to be round, bump shape is not limited to circular structures but may readily take the form of rectangles or other desired geometries. Reliable and well-defined bumps as small as 0.005 inch in diameter have been formed using the mask.

To further describe FIG. **1**, the mask **1** is shown prior to attachment to a substrate **5** onto which the bumps are to be deposited. The mask is preferably formed from 0.001- or 0.002-inch thickness Kovar. The substrate **5** is held within a vacuum deposition chamber (not shown) on a vacuum pedestal **7** and is seen to have a conductor pattern **9** disposed on its surface. The conductor pattern **9** may be formed by vacuum deposition or any other technique suitable to the production of an electrically conductive pattern on a substrate. Aluminum is the most commonly used conductive material for producing a thin film conductor pattern on a substrate. The conductor pattern **9** is seen to have a multiplicity of conductive pads **11** onto which the bonding bumps will be formed.

Attachment of the mask **1** to the substrate **5** is accomplished by lowering the mask onto the substrate **5** and by aligning registrations **13** which are disposed on the mask **1** and on the substrate **5**. Accurate alignment of the registrations **13** may be aided by the use of a microscope. After accurate alignment of mask and substrate, support tabs **15** on the mask **1** are bent around the edges of the substrate **5**. FIG. **2** shows the mask **1** properly attached to the substrate **5**.

Prior to metallic deposition, the substrate **5** is heated to 400° C., glow discharge cleared, and subsequently cooled to 25° C. Metal deposition is preferably effected through use of a vacuum evaporation source, shown generally at **20** in FIG. **3**. The relationship of the substrate-mask assembly **19** to the evaporation source **20** is shown in the FIG. **3**, that is, the substrate-mask assembly **19** is disposed face-on to the evapora-

tion source **20**. The evaporation source **20** is seen to consist of two types of metal evaporators **22** and **24**. Metal evaporator **22** is seen to comprise a typical cylindrical evaporation source having regularly spaced perforations **23** disposed face-on to the object on which deposition is to be made. The metal evaporators **24** are seen to be dish-type metal evaporators, one of which is preferably disposed on each side of the evaporator **22**.

According to the present method, a first metal is evaporated from the evaporator **22**, through the mask **1**, and onto the conductive pads **11** disposed on the substrate **5**. After the first metal has been deposited to the desired thickness, the evaporation of a second metal from the evaporators **24** is initiated, the first and second metals being coevaporated from the evaporators **22** and **24** respectively to form a phased metallized gradient structure. Codeposition onto the substrate **5** continues until a desired thickness of the codeposited metals is formed onto the previously deposited first metal. Deposition of the first metal is then discontinued, deposition of the second metal continuing until a desired thickness of said second metal surmounts the previously deposited material.

A bonding bump thus produced is seen in FIG. **4** at **30**. The particular bump **30** shown in the drawing is formed with chromium as the first metal and tin as the second metal. Desired thickness for this particular combination of metals is 600 A for the chromium layer **32**, 20,000 A for the phased chromium-tin layer **34**, and 80,000 A for the tin layer **36**.

The bump **30** can also be comprised, as may be necessary for a particular application, of other combinations of depositable metals. In particular, copper and gold may be readily substituted as the second metal, thus producing a chromium-copper or chromium-gold bump.

Of particular note in the production of the chromium-tin bump **30** is the desirability of observing the tin deposition during the process. This observation is easily accomplished by means of a 25×75 cm. glass microscope slide (not shown) placed approximately 5 cm. below the plane of the substrate and at an angle of 45° to the vertical. The purpose of the glass microscope slide is to monitor the thin film temperature rise during evaporation of tin. Since tin has a relatively low melting point of 232° C. and since thermal radiation from the dual tin evaporators **24** can heat the substrate-mask assembly **19** to temperatures considerably hotter than 232°, the evaporation source **20** must be shut off at the first sign of tin melt. Melt of the tin deposit can readily be observed along the bottom edge of the microscope slide. When the substrate-mask assembly **19** has cooled sufficiently, the tin evaporation is continued. The time required for cooling may extend up to 45 minutes without affecting the quality of the tin film.

Upon removal of the substrate-mask assembly **19** from the vacuum evaporator, the masks **1** are dismounted and the substrates **5** bearing the bonding bumps **30** submitted to dicing, testing, inspection, and the further steps in the typical hybrid assembly process. FIG. **5** shows a typical substrate **5** having bonding bumps **30** disposed at the proper locations on the conductor pattern **9**.

The bumps **30** may be used immediately for mounting hybrid microcircuit components by the method described above. Alternatively, the bumps **30** may be further processed to produce a solder dipped bump. In this process, the substrate **5** is taken directly from the vacuum deposition chamber and, after removal of the mask **1**, dipped into a solder bath containing the desired bump alloy melt to form a raised solder-dip bump. This process minimizes vulnerability of the freshly deposited bumps **30** to surface contamination. A solder flux coating may be applied to the surface of the substrate **5** prior to dip into the solder bath. The solder flux coating may comprise a 50 percent solution of Kester Solder Flux No. 1544 and Kester AP–20 Resin Residue Remover. The solder flux is removed immediately after dipping in the solder bath by immersing the dipped substrate **5** in AP–20 bath and scrubbing with a small camel hairbrush. Three sequential baths in boiling methanol followed by an acetone rinse is usually sufficient to clean the dipped substrate **5**. Dipped bumps are most advantageously formed from a solder bath alloy of 96 percent tin to 4 percent silver. The proper temperature for the alloy during dipping is 230° to 235° C. The immersion time should be limited to a maximum of 3 seconds, although only about 1 second is necessary to wet properly the bump locations and to produce consistent bump sizes. FIG. **9***b* shows the spherical nature of a typical dipped bump **40**.

Both the thin film bump **30** and the dipped bump **40** are useful for bonding of hybrid add-on components in hybrid assemblies. Mounting by use of the bumps **30** and **40** may be accomplished by either a one- or two-step process, that is, by ultrasonic bonding or by ultrasonic bonding followed by reflow on a heated column. In FIG. **6***a*, a dipped tin-gold bump **40** formed on a hybrid component **42** is seen after ultrasonic bonding to a chromium-tin thin film bump **30** formed on aluminum conductor pad **11** of the substrate **5**. FIG. **6***b* shows the bonded bumps of FIG. **7***a* after reflow on a heated column in a controlled atmosphere.

FIG. **7***a* depicts two ultrasonically bonded thin film bumps **30** before reflow. Although the strength of the bonded bumps **30** shown in FIG. **7***a* is sufficient for some applications, the bumps **30** may be reflowed to produce the component-substrate mounting shown in FIG. **7***b*.

FIG. **8** shows a typical hybrid assembly at **50** which comprises a substrate **5** having conductor pattern **9** disposed on its surface. Thin film bumps **30** are seen on the pattern **9** as means for mounting a resistor chip **52** and a transistor chip **54**. The resistor chip **52** has thin-film bumps **30** formed on conductors **53** on the chip surface. Similarly, the transistor chip **54** has dipped bumps **40** formed on the chip surface. The disposition of the bonding bumps **30** and **40** on the substrate **5** and on the chips **52** and **54** allow facile and reliable chip mounting. The arrows in the drawing demonstrate the "face-down" nature of the mounting technique.

FIG. **9***a* presents a special hybrid packaging problem which is readily solved through use of the present methods. A particular hybrid circuit array required a plurality of critical resistors having a large spread in ohmic value. The temperature coefficients of the resistors were closely matched and the value tolerance necessarily held to better than 5 percent. Hybrid design considerations indicated that a low yield could be expected if the resistors were included on the substrate with all of the other thin-film elements. Therefore, the critical resistors were designed to fit onto a separate substrate **60**. Thus, yield problems of the critical components could be divorced from the main substrate fabrication effort. This "piggyback" substrate **60** bearing the critical resistors **62** was thus mounted "face-down" on a large-scale hybrid array **64** using bonding bumps produced according to the present method. The bonding bumps on the "piggyback" substrate **60** were chosen to be dipped tin-gold bumps **40**, an enlarged view of one of which is seen in FIG. **9***b*. The bonding bumps on the "mother" substrate **66** are chosen to be chromium-tin film bumps **30**.

A bonding bump useful for some applications is perhaps more readily produced than the phased metallic bumps previously described. This bump is a thin film copper bump deposited through a mask in a fashion similar to that described hereinabove. However, prior to copper deposition, the substrate temperature is increased to approximately 500° C. and glow discharge cleaned, the copper being rapidly deposited while the substrate is at the elevated temperature. Drawbacks of the method include possible degradation of thin film elements previously deposited on the substrate. The thin film copper bump thus produced may be subjected to the solder dip process previously described to produce a dipped bump. However, the thin film of copper must be at least 0.0005 inch thick in order to prevent absorption of all of the copper into the melted alloy dip.

It will be understood that the above-described methods for producing bonding bumps for the assembly of hybrid microcircuit arrays are operable with a number of different

metals and variations in technique from the specific steps described hereinabove are within the scope of the invention as recited in the appended claims.

I claim:

1. A method for producing bonding bumps for reliable mounting of hybrid microcircuit components to a substrate, comprising

forming a pattern of holes in a mask composed of a metallic material having a coefficient of expansion less than that of the substrate,

aligning said patterned mask on a substrate bearing a conductive pattern,

affixing the mask to a substrate by bending supporting tabs on said mask around the edges of the substrate,

depositing a first conductive substance to a first thickness through the holes in the mask and onto the conductive pattern,

codepositing a second conductive substance with said first conductive substance to form a second thickness of a phased gradient structure surmounting said first-deposited material,

discontinuing the deposition of said first conductive substance and continuing the deposition of said second conductive substance to complete the structure of the bonding bump, the successive depositions to which the mask and substrate are subjected causing the substrate to become more firmly held by the mask.

2. The method of claim 1 wherein said first conductive substance comprises chromium metal and the second conductive substance comprises tin.

3. The method of claim 1 wherein said first conductive substance comprises chromium metal and the second conductive substance comprises copper.

4. The method of claim 1 wherein said first conductive substance comprises chromium metal and the second conductive substance comprises gold.

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