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(54) **PULSE FORMING CONVERTER**

(76) Inventor: **Donald Joe Deaton**, Huntsville, AL (US)

Correspondence Address:
Russell Carter Gache
Sirote & Permutt, P.C.
Po Box 55727
Birmingham, AL 35255-5727 (US)

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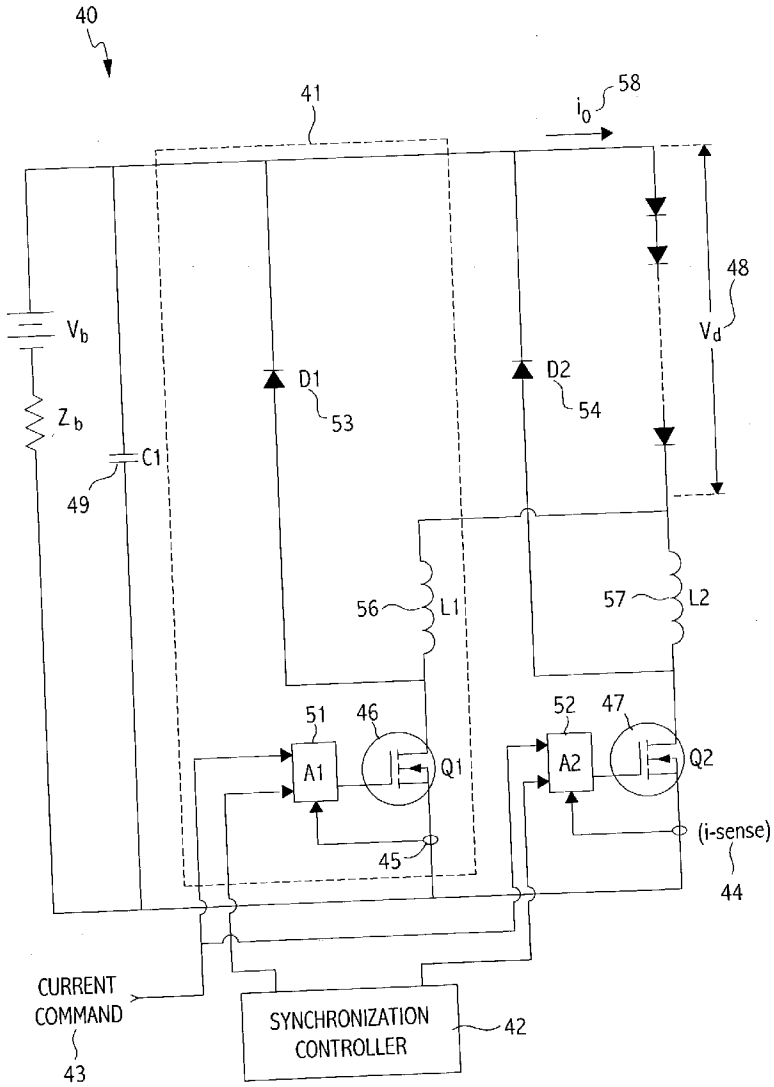
(52) **U.S. Cl.** **327/427**

(57) **ABSTRACT**

A scalable, interleaved pulse forming converter is disclosed having two Buck swithing converter modules each contributing half to the total load of the circuit to produce a programmable current pulse. Synchronization pulses to the two modules are set 180 degrees out of phase of each other to reduce ripple current. The invention is susceptible to various interleaved modifications to further reduce ripple current and increase power, as well as to electrically isolate the load from input or battery ground.



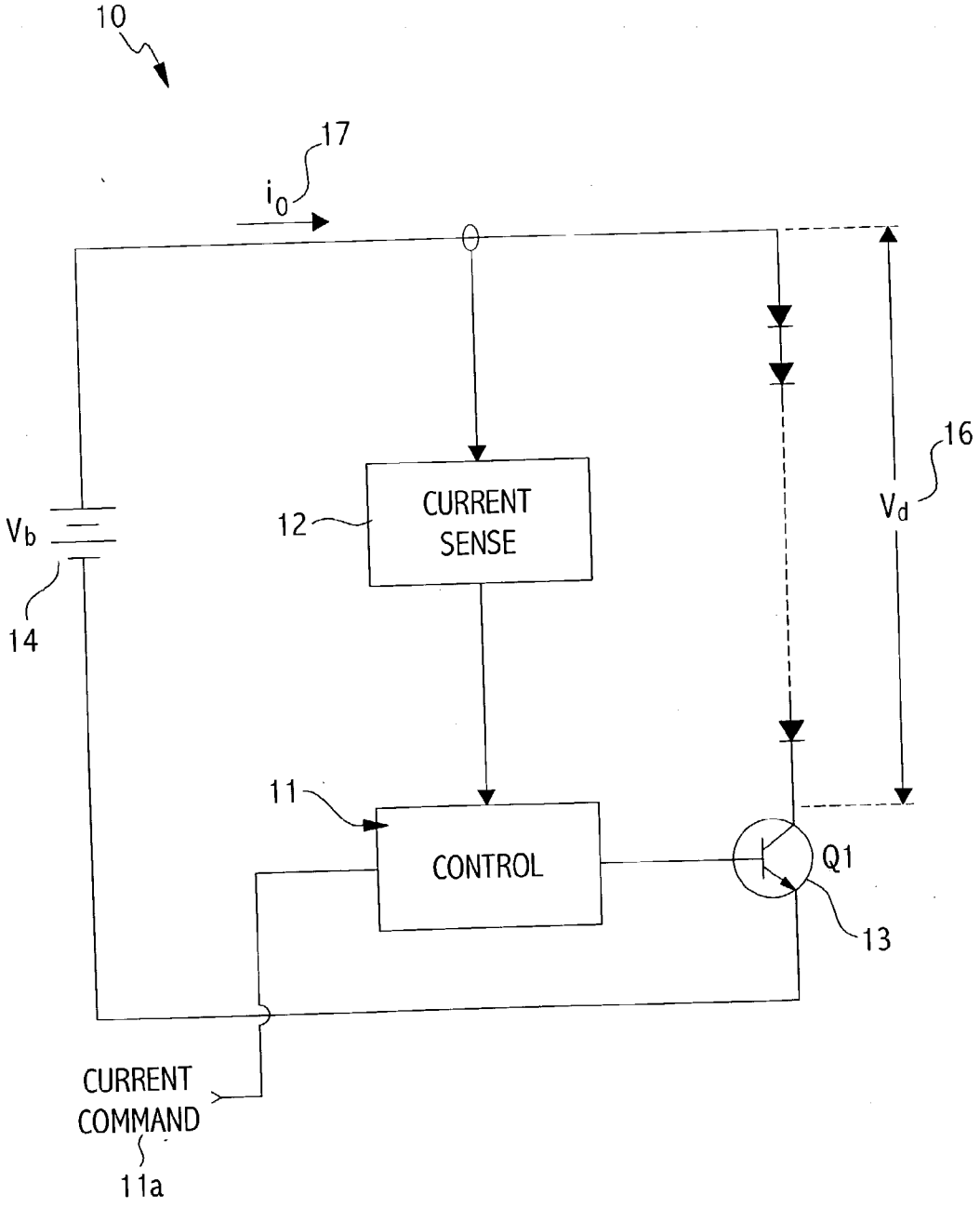

10
17
i_0
16
V_d
12
CURRENT SENSE
V_b
14
11
CONTROL
Q1
13
CURRENT COMMAND
11a

FIG. 1

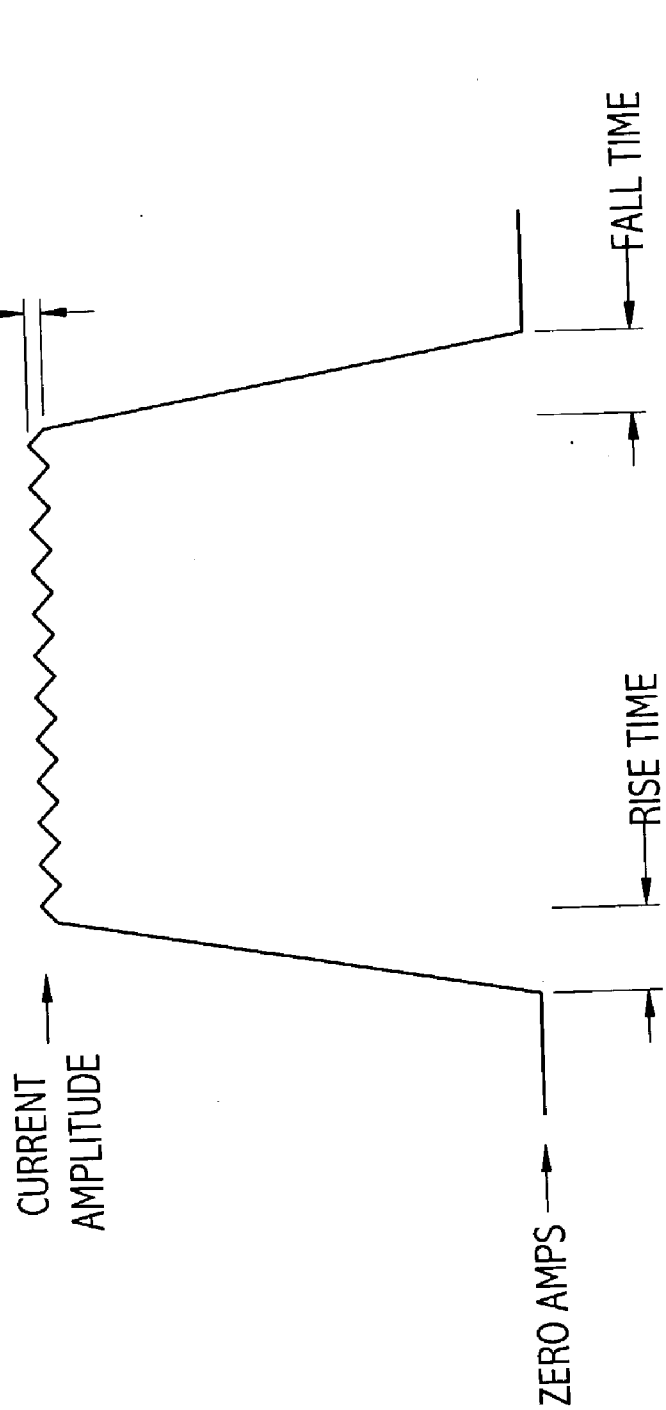

CURRENT RIPPLE
FALL TIME
RISE TIME
CURRENT AMPLITUDE
ZERO AMPS

FIG. 1A

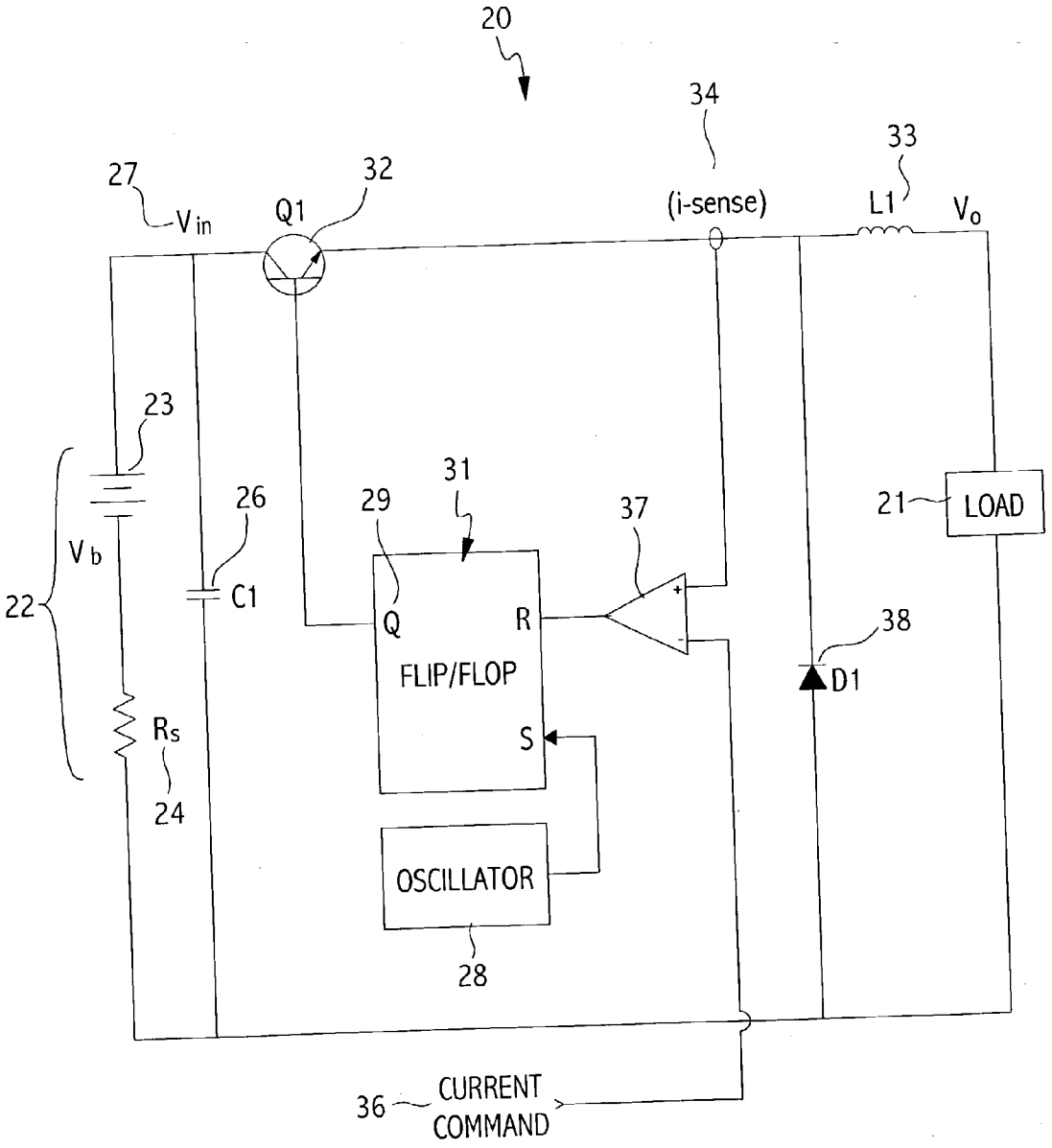

20
34
33
27
Vin
Q1
32
(i-sense)
L1
Vo
23
31
26
29
37
21
LOAD
Vb
22
C1
Q
R
38
FLIP/FLOP
D1
Rs
S
24
OSCILLATOR
28
36
CURRENT
COMMAND

FIG. 2

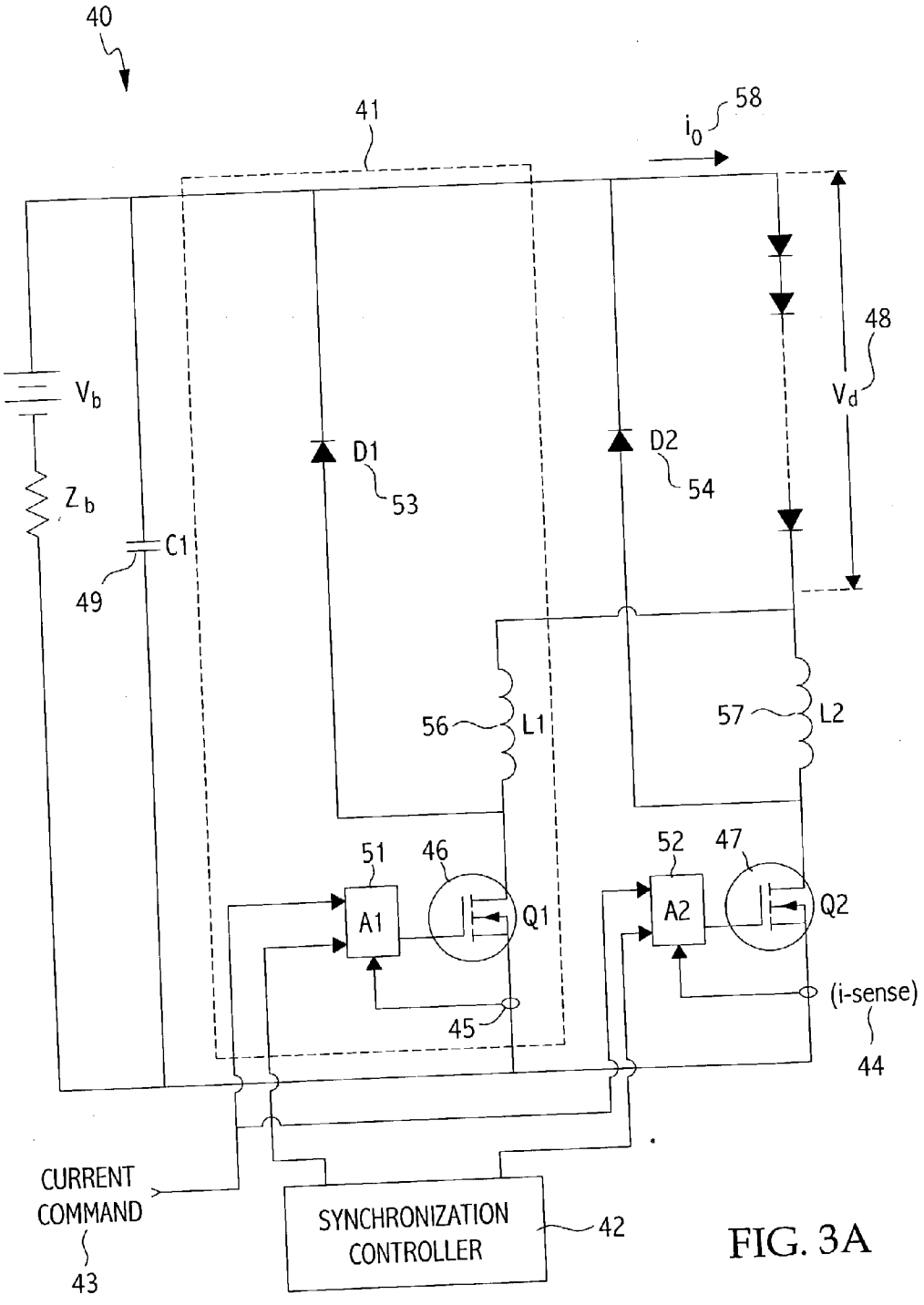

40
41
58
i_0
48
V_d
V_b
Z_b
C1
49
D1
53
D2
54
56
L1
57
L2
51
46
52
47
A1
Q1
A2
Q2
45
(i-sense)
44
CURRENT COMMAND
43
SYNCHRONIZATION CONTROLLER
42

FIG. 3A

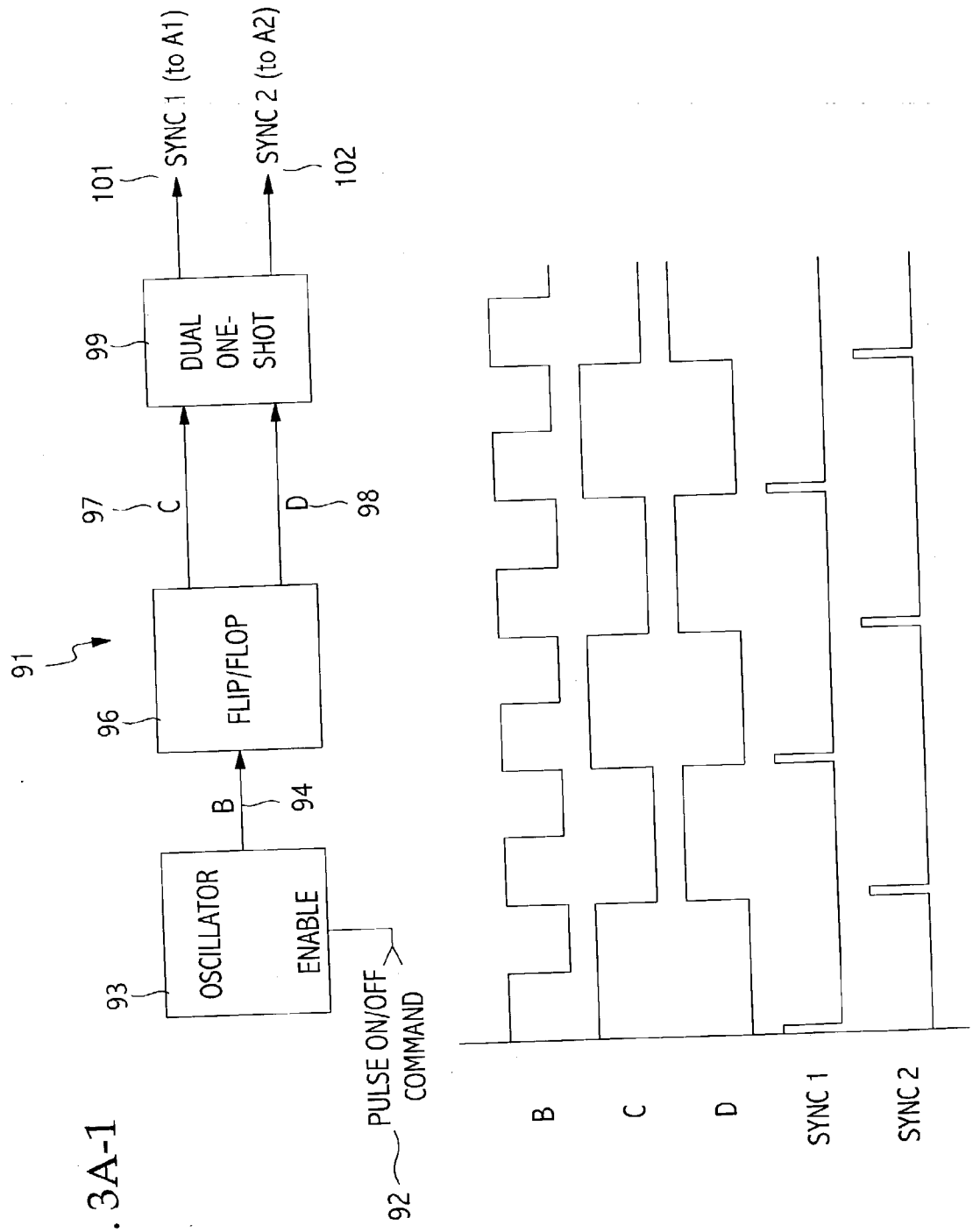

SYNC 1 (to A1)
SYNC 2 (to A2)
101
102
99
DUAL ONE-SHOT
97
C
D
98
91
96
FLIP/FLOP
B
94
93
OSCILLATOR
ENABLE
PULSE ON/OFF COMMAND
92
B
C
D
SYNC 1
SYNC 2

FIG. 3A-1

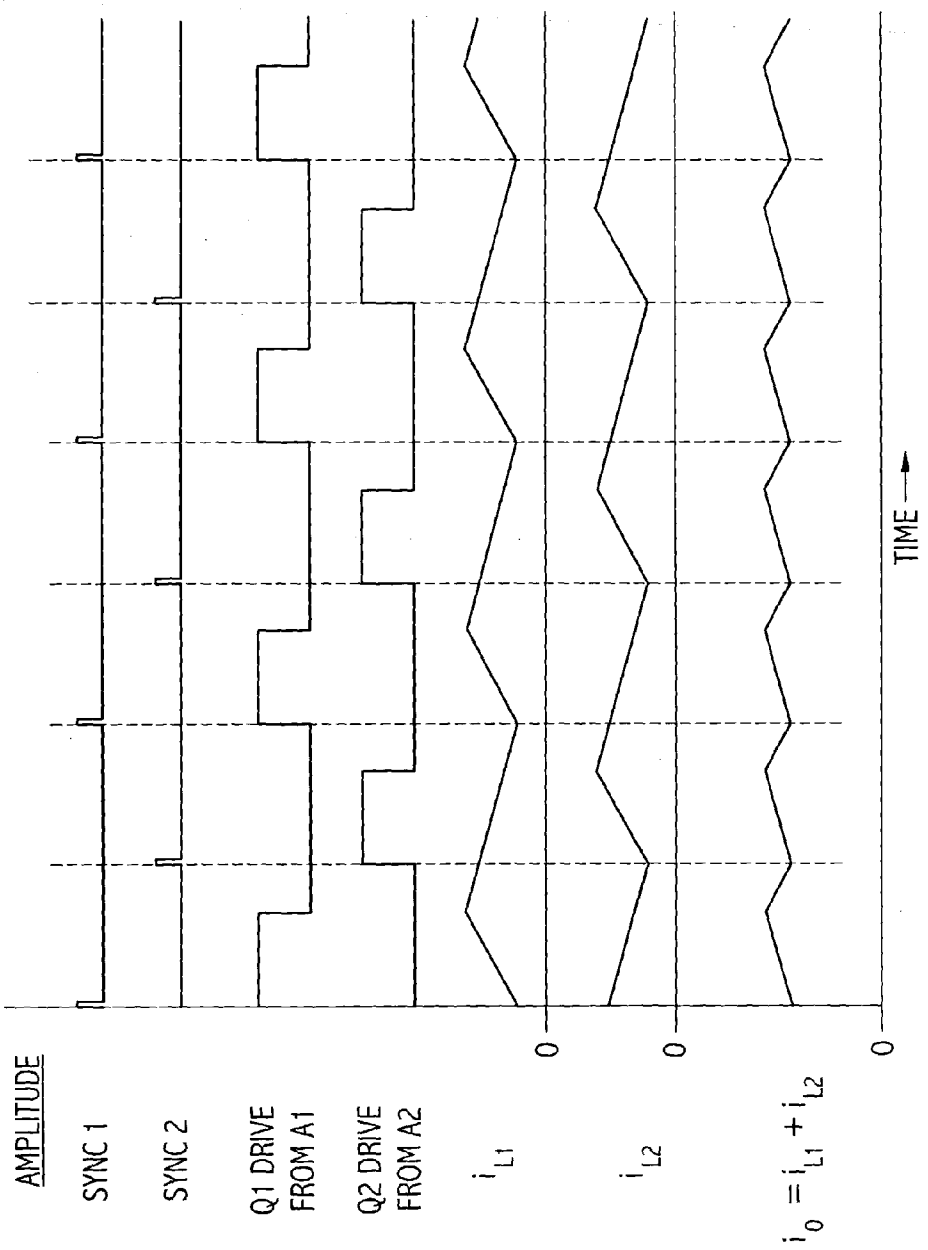

AMPLITUDE
SYNC 1
SYNC 2
Q1 DRIVE FROM A1
Q2 DRIVE FROM A2
i_{L1}
i_{L2}
$i_o = i_{L1} + i_{L2}$
0
0
0
TIME

FIG. 3B

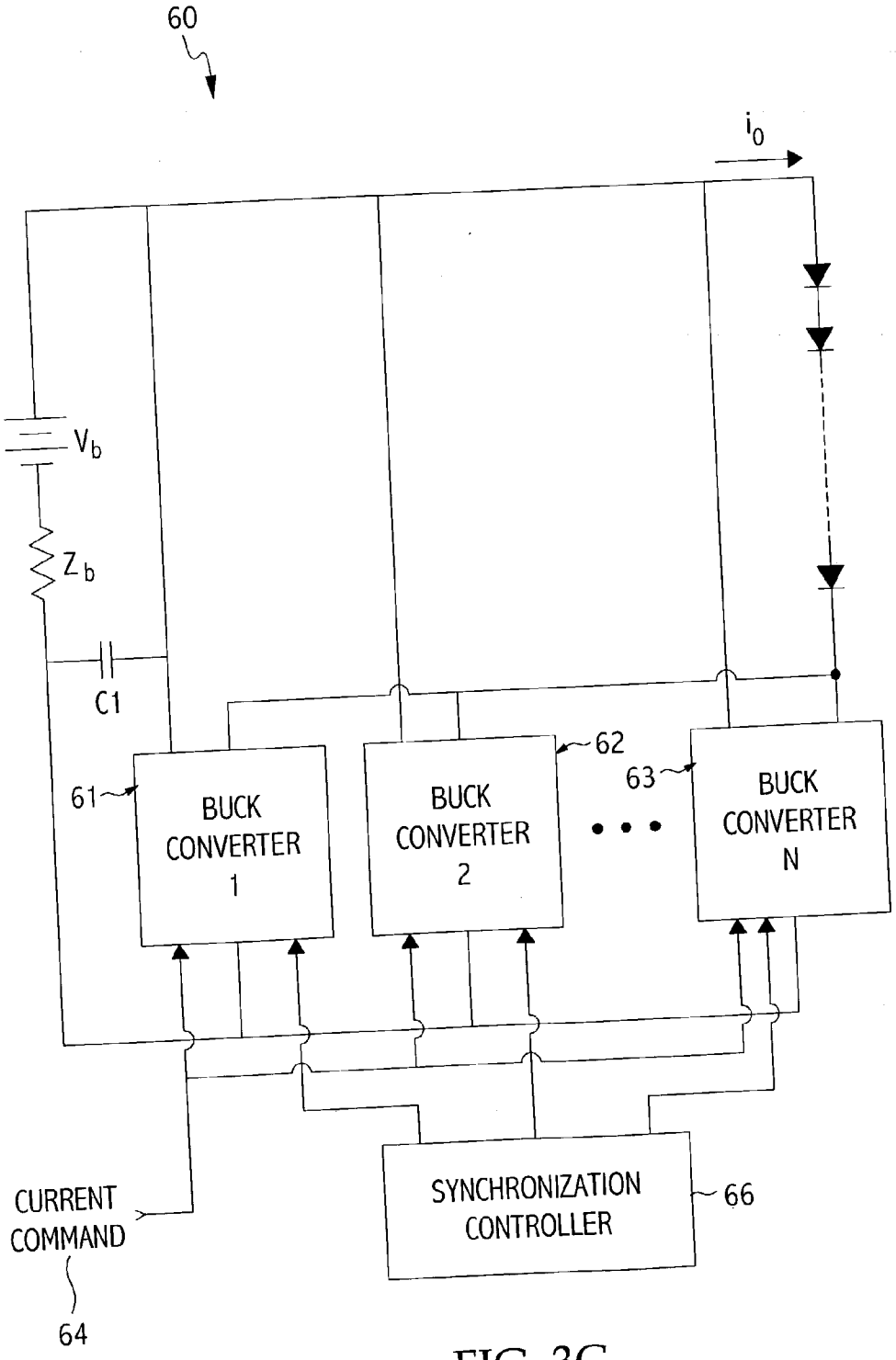

60
i_0
V_b
Z_b
C1
61
BUCK CONVERTER 1
BUCK CONVERTER 2
62
63
BUCK CONVERTER N
CURRENT COMMAND
64
SYNCHRONIZATION CONTROLLER
66

FIG. 3C

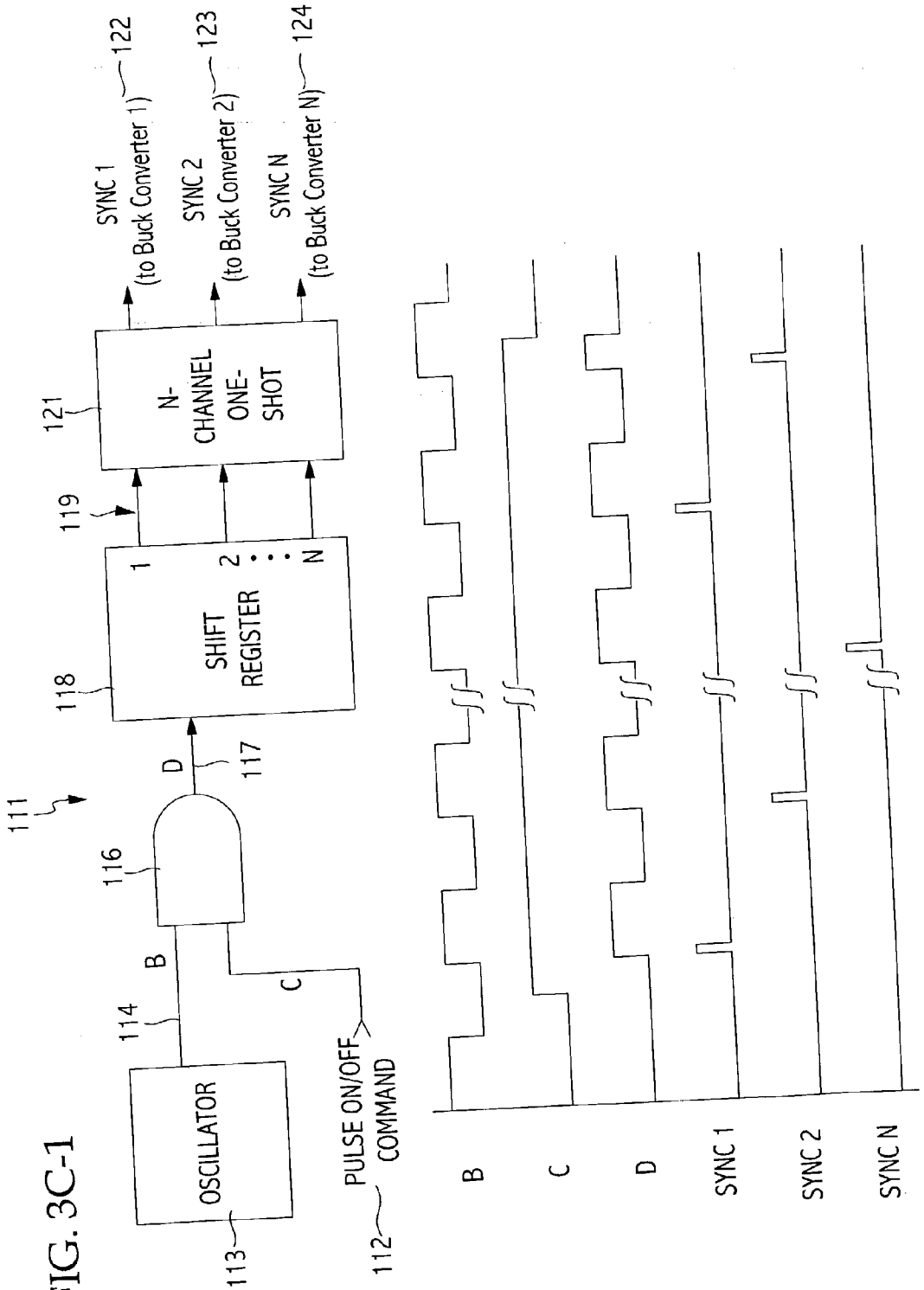

111
OSCILLATOR
113
114
B
116
D
117
C
PULSE ON/OFF COMMAND
112
118
SHIFT REGISTER
1
2
N
119
121
N-CHANNEL ONE-SHOT
SYNC 1 (to Buck Converter 1)
122
SYNC 2 (to Buck Converter 2)
123
SYNC N (to Buck Converter N)
124
B
C
D
SYNC 1
SYNC 2
SYNC N

FIG. 3C-1

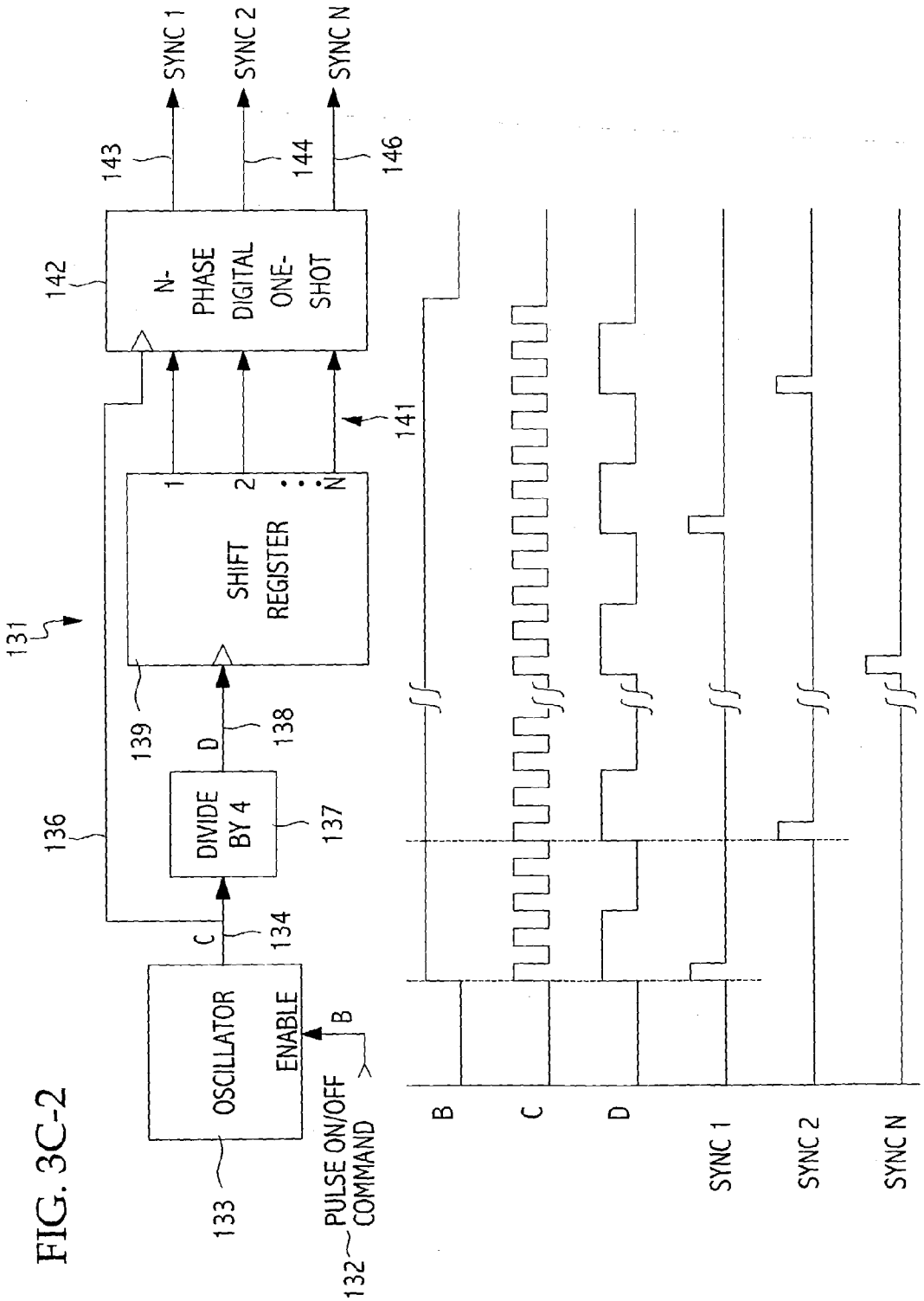

SYNC 1
SYNC 2
SYNC N
143
144
146
142
N-PHASE DIGITAL ONE-SHOT
141
131
SHIFT REGISTER
1
2
N
139
D
138
136
DIVIDE BY 4
137
C
134
OSCILLATOR
ENABLE
B
133
PULSE ON/OFF COMMAND
132
B
C
D
SYNC 1
SYNC 2
SYNC N

FIG. 3C-2

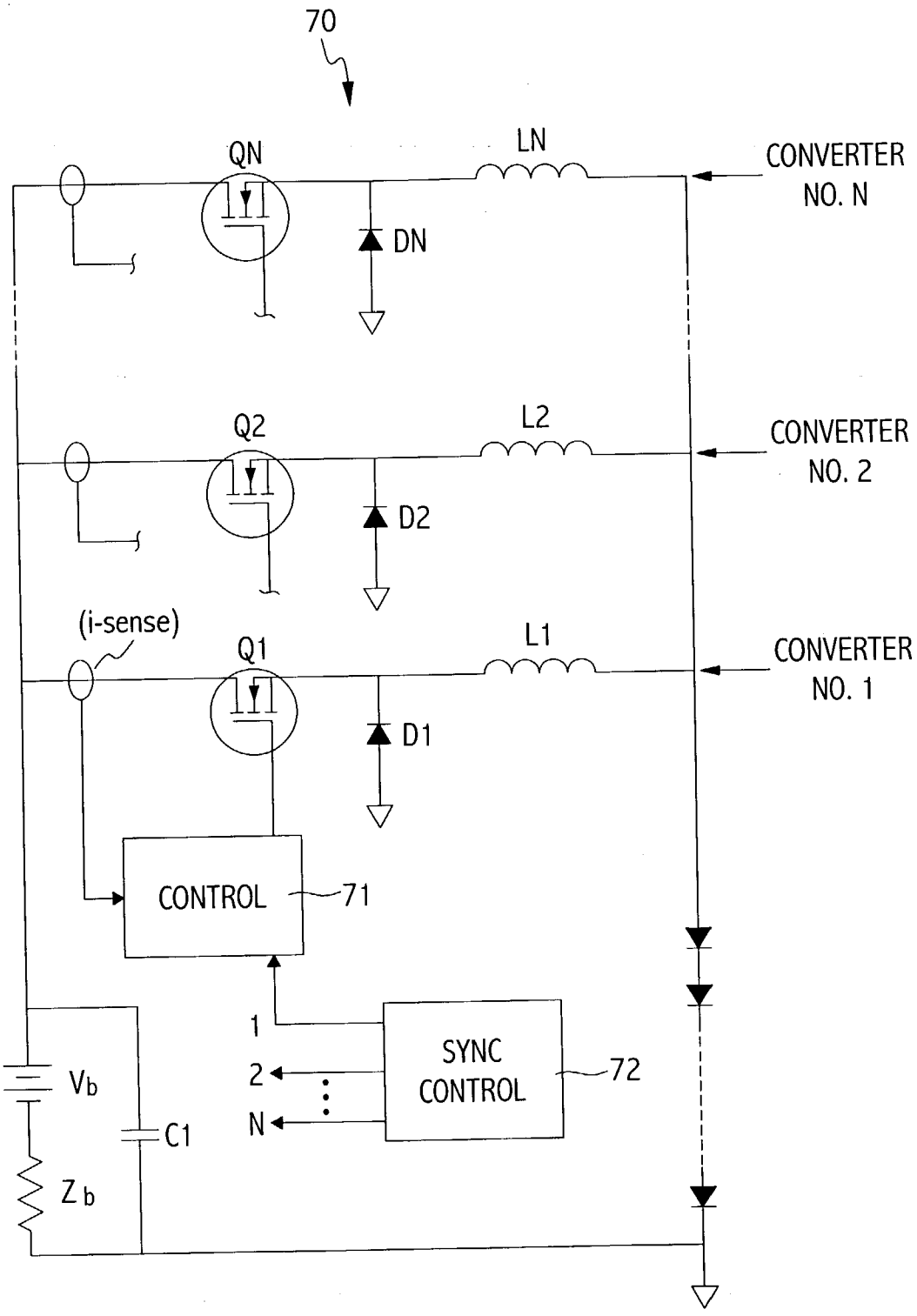

70
QN
LN
CONVERTER NO. N
DN
Q2
L2
CONVERTER NO. 2
D2
(i-sense)
Q1
L1
CONVERTER NO. 1
D1
CONTROL
71
1
2
N
SYNC CONTROL
72
Vb
C1
Zb

FIG. 4

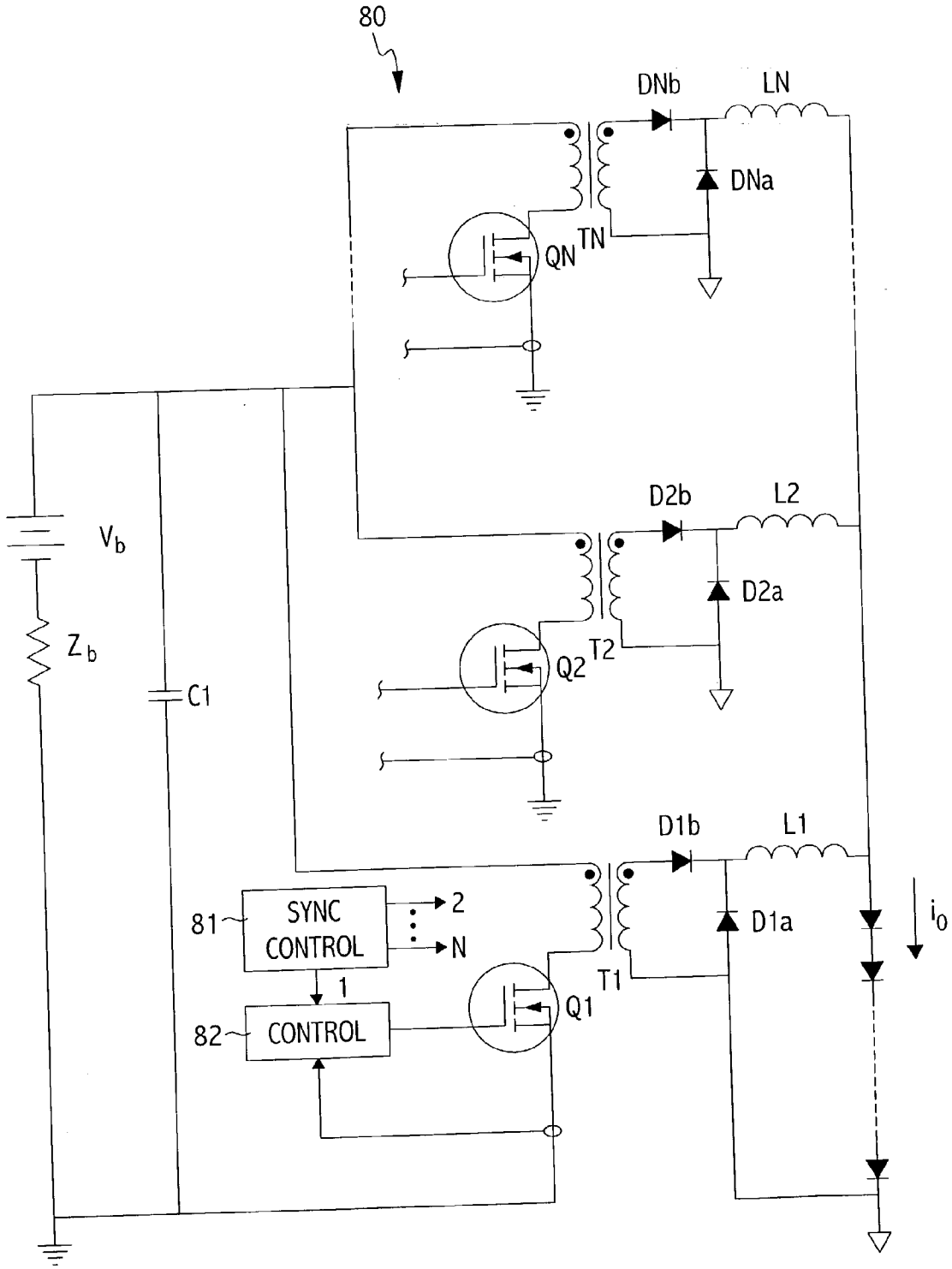

80
DNb
LN
DNa
QN
TN
D2b
L2
D2a
Q2
T2
Vb
Zb
C1
D1b
L1
D1a
io
81
SYNC CONTROL
2
N
1
82
CONTROL
Q1
T1

FIG. 5

PULSE FORMING CONVERTER

[0001] This application claims the benefit of filing priority under 35 U.S.C. §119 and 37 C.F.R. §1.78 of the co-pending U.S. Provisional Application Serial No. 60/388,539 filed Jun. 13, 2002, for and Improved Pulse Forming Converter. All information diclosed in that prior pending provisional application is incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates generally to pulse forming networks. In particular, the present invention relates to pulse forming converters and pulse generating interleaved converters.

BACKGROUND OF THE INVENTION

[0003] A Pulse Forming Converter ("PFC") is an electronic circuit that generates high power current pulses or voltage pulses that are delivered to an electrical load. Part of the goal of a PFC is to shape electrical pulses in terms of amplitude, pulse width, and duty cycle. PFC's are utilized to drive a variety of loads, including resistive loads, leading and lagging power factor loads and non-linear loads such as high power laser diodes. However, currently many types of PFC's operate with relatively low efficiency, and some even require a great deal of cooling support hardware.

[0004] Designers of PFC's esteem the following characteristics of PFC's, which heretofore have been elusive to achieve with today's circuits:

[0005] 1. Generate current pulses (or voltage pulses) with precisely controlled amplitude and/or pulse width;

[0006] 2. Programmable pulse amplitude;

[0007] 3. Programmable pulse width;

[0008] 4. Programmable duty cycle or repetition rate;

[0009] 5. High efficiency;

[0010] 6. Lightweight;

[0011] 7. Fast pulse rise time and fall time;

[0012] 8. Low current ripple;

[0013] **FIG. 1** shows a linear pulse generator **10** that is a foundation example of the elements in a PFC. It consists of an amplifier which is a control mechanism **11** having a current command input **11***a*, a current sense device **12**, a power transistor **13** and a power source **14** shown as a battery. The amplifier uses feedback to compare the sensed current with a current command and adjusts the drive to the power transistor to obtain the desired pulse amplitude and pulse width at the load. Such loads **16** may vary, but are shown in the Figure as a series of laser diodes. For clarity of discussion, **FIG. 1A** shows a typical current pulse with portions defined that are important characteristics for a PFC.

[0014] One undesirable characteristic of linear pulse generators is high power dissipation. The power dissipated in the power transistor is equal to the product of the voltage across the transistor switch **13** times the load current **17**. This high power dissipation limits the amount of power that can be obtained from this device. Cooling hardware that is heavy and occupies a large volume may even be needed to maintain an acceptable operating temperature in the power transistor **13**.

[0015] **FIG. 2** shows a good example of pulse forming network **20** utilizing a Buck switching converter. The Buck switching converter shown is used to regulate direct current (DC) in a load by regulating a DC current to a load **21** that is equal to a steady state commanded current. The load **21** can be a resistor, or a reactive load such as a resistor and capacitor in parallel. It can also be any of several electrical devices including DC motors and laser diodes. The power source **22** is shown as a battery **23** with series resistance Rs **24**. The power can be from other sources including a DC generator or rectified utility power. Capacitor C**126** reduces ripple on input voltage Vin **27**.

[0016] Operation of the Buck switching converter is as follows. An oscillator **28** sends out pulses at a fixed frequency. The first pulse sets the output Q **29** of the flip/flop **31** high. This turns on transistor switch **32**, which is shown as a bi-polar transistor, but may be other suitable transistors such as field effect transistors ("FETs") or power MOSFETs. A voltage equal to (Vin−Vo) is applied across the inductor L1 **33**. The current in L1 increases at a rate defined by (Vin−Vo)/L1.

[0017] The current in the transistor switch is measured by current sensor **34**. The sensed current is compared to current established by commanded current **36** at comparator **37**. When the sensed current exceeds the commanded current, the output of the comparator **37** resets the output Q **29** of the flip/flop **31** to a low value that turns off the transistor switch **32**. Diode D**138** conducts and provides a path for current to continue to flow through the inductor to the load **21** after switch **32** has been turned off. With the transistor **32** off, the inductor current decreases at a rate of Vo/L1.

[0018] When the next pulse is sent by the oscillator **28**, the transistor **32** is turned on and the process repeats. In this way, the Buck switching converter **20** can regulate peak current into a load. This control method is known as "pulse-width-modulation" because the "on" time of the transistor is modulated to control the output.

[0019] The Buck switching converter **20** can be used as a pulse generator by gating it on and off. An advantage of the Buck switching converter **20** over the linear pulse generator **10** is high efficiency. Because the transistor switch is either ON or OFF, it has low power dissipation. This reduces the cooling requirement.

[0020] A disadvantage of the Buck switching converter pulse generator **20** is slow rise time. The pulse rise time is inversely proportional to the inductor value. In other words, decreasing the value of L1 reduces rise time. The penalty for decreasing the value of L1 is increased load ripple current.

[0021] Therefore, what is needed is a pulse forming converter that has improved efficiency over existing designs while maintaining fast waveform rise times, low ripple current in the load, and low weight and size.

SUMMARY OF THE INVENTION

[0022] In summary, the present invention comprises a scalable, interleaved pulse forming converter having 2 Buck switching converter modules each contributing half to the

total load of the circuit. Synchronization pulses to the two modules are set 180 degrees out of phase of each other to reduce ripple current. Additional embodiments are shown in which module interleaving may be utilized to further reduce ripple current and increase power, as well as to electrically isolate the load from input or battery ground.

[0023] Other features and objects and advantages of the present invention will become apparent from a reading of the following description as well as a study of the appended drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] A pulse forming converter incorporating the features of the invention is depicted in the attached drawings which form a portion of the disclosure and wherein:

[0025] **FIG. 1** is a circuit diagram showing the basic elements in a linear pulse generator;

[0026] **FIG. 1A** shows a typical current pulse with portions defined that are important characteristics for a PFC;

[0027] **FIG. 2** is a circuit diagram of a common switching converter;

[0028] **FIG. 3A** is a circuit diagram of an improved pulse forming converter;

[0029] **FIG. 3A-1** is an example of a synchronization controller for the circuit diagram in **FIG. 3A** with comparable waveforms;

[0030] **FIG. 3B** is a waveform diagram showing expectant signals associated with the circuit shown in **FIG. 3A**;

[0031] **FIG. 3C** is a circuit diagram of the embodiment shown in **FIG. 3A** of the improved pulse forming converter generalized to N phases;

[0032] **FIG. 3C-1** is an example of a synchronization controller for the circuit diagram in **FIG. 3C** with comparable waveforms;

[0033] **FIG. 3C-2** is another example of a synchronization controller for the circuit diagram in **FIG. 3C** with comparable waveforms;

[0034] **FIG. 4** is a circuit diagram of the embodiment shown in **FIG. 3C** with the load connected to ground; and,

[0035] **FIG. 5** is a circuit diagram of embodiment shown in **FIG. 3C** with isolated outputs.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0036] Referring to the drawings for a better understanding of the function and structure of the invention, **FIG. 3A** shows the preferred embodiment 40 of the present PFC invention.

[0037] The preferred embodiment consists of 2 Buck switching converter modules each contributing half of the total load current. For clarity, a dashed line **41** surrounds one of the two Buck converter modules in **FIG. 3A** enclosing the primary elements for Buck converter modules referenced in **FIG. 3C**. Power switches Q1 **(46)** and Q2 **(47)** are shown as power MOSFETs, but may be any suitable power transistor meeting the power and switching demands of the load V_d **(48)**. The load **48** is shown in **FIG. 3A** as a series string of solid state laser diodes, but can be any type of load requiring pulsed current or voltage. Power switches Q**146** and Q**247** require a voltage rating greater than the source voltage Vb and a current rating greater than ½ i_0 peak. Diodes D**153** and D**254** also require a voltage rating greater than Vb and a current rating greater than ½ i_0 peak. Capacitor C**149** requires a voltage rating greater than Vb.

[0038] The individual Buck controller modules A1**(51)**-A2**(52)** operate as previously described, but with special synchronization such that they are interleaved and pulse width modulated to control current. Current sensors ("i-sense") **44** and **45** accurately sense current flow at the position in the circuit as shown through the use of a hall effect traducer or other suitable current sensors. Each current sensor has a current rating greater than ½ i_0 peak. Controllers A1 and A2 are synchronized so that Q1 turns on at time to and Q2 turns on at t_0+T/2, with T equal to the pulse width clock period. The synchronization pulses generated by synchronization controller **42** to the 2 modules are set 180 degrees out-of-phase with each other. This causes the load ripple current to sum together in a manner that cancels the ripple to a great degree.

[0039] **FIG. 3A-1** shows one strategy **91** for implementing the synchronization controller **42** along with waveforms which clarify the controller operation. A load current pulse is initiated by a logic high signal via an ON/OFF command pulse **92** into the enable input of the oscillator **93** as shown. The pulse ON/OFF command **92** stays high for the duration of the output load current pulse. A high frequency pulse train (typically 100 kHz to 10 MHz) B **94** is generated by the oscillator **93** and is sent to a flip/flop **96**. The flip/flop **96** generates two signals, C **97** and D **98**, which are out of phase. A dual "one-shot" (i.e. a dual monostable multivibrator with Schmitt-trigger input, such as an LS123 IC) **99** receives these signals and generates signal SYNC **1101** which is a narrow pulse that occurs at the rising edge of signal C **97**. The one-shot **99** also generates signal SYNC **2102** which is a narrow pulse that occurs at the rising edge of signal D **98**. SYNC **1101** and SYNC **2102** switch the two Buck converters 180 degrees out-of-phase in order to minimize ripple current in the output load pulse. The output load pulse is terminated when the pulse ON/OFF command **92** is set to logic low. A series of output pulses can be generated with programmable pulse widths and duty cycles by switching the pulse ON/OFF command **92** high and low with desired timing. These control commands can be generated in several ways, including microprocessor control, discrete digital logic or with a programmable logic device, as is known.

[0040] Theoretically, current ripple is completely cancelled at 50% duty cycle for the 2 converter PFC **40**. At duty cycles other than 50%, the ripple current is reduced compared to the individual inductor currents, but is not completely eliminated. The input ripple current is also reduced compared to a single Buck switching converter. This reduces the ripple current requirement on capacitor C1 **(49)**, allowing the use of a smaller capacitor.

[0041] The current command signal **43** sets the output pulse amplitude by providing the reference to each Buck converter's internal comparator as described in circuit **20**. The pulse amplitude can be programmed to different amplitudes as desired by adjusting the current command voltage.

This programming can be done by various means such as adjusting a potentiometer, or from a D-to-A ("digital-to-analog") converter that receives the amplitude setting from a computer, as is known.

[0042] An alternate method for controlling pulse width and duty cycle is to set the current command signal **43** to zero, set the power ON/OFF command to logic high, and set the current command signal **43** to the desired command amplitude for a desired pulse width time, then back to zero. This can be repeated at the desired repetition frequency to control duty cycle.

[0043] The present invention uses the described interleaved converter technique to generate high power pulses with fast rise and fall times, and low ripple currents. For example, if we compare the 2 inductors in the 2 stage PFC **40** to the single inductor in the previously discussed Buck switching converter **20**. In general, the weight of the magnetic core in an inductor is proportional to the square of the current in the inductor. By using 2 inductors each operating at half the load current, the sum of the weight of the 2 cores in the 2 stage PFC is ½ the weight of the single core in the equivalent single stage Buck switching converter. Because the 2 inductors are in parallel, the pulse rise time for the 2 stage PFC is half the time for the 1 stage Buck switching converter. **FIG. 3B** shows typical waveforms resulting from the circuit **40** described in **FIG. 3A**.

[0044] **FIG. 3B** depicts a snapshot of waveforms in the middle of a pulse with the synchronization controller **42** setting the switching frequencies of Q1(**46**) and Q2(**47**) to turn each on when 180° out-of-phase as shown. In response, ripple currents in inductors L1(**56**) and L2(**57**) are 180° out-of-phase and output current i_0(**58**) equals the sum of currents in L1 and L2.

[0045] An undesirable phenomenon known as sub-harmonic oscillation can occur in current regulating Buck converters at higher duty cycles. A standard technique applicable to DC to DC Buck converters, adding slope compensation, is effective to prevent this phenomenon in the interleaved Buck converters, such as depicted herein.

[0046] The present invention can be generalized for any number of interleaved converter modules. **FIG. 3C** shows another embodiment **60** of the invention with N interleaved converter modules. Each module **61-63** is connected as shown and receives current command signals from current command source **64** as in circuit **20**. Synchronization pulses are sent to each module from synchronization controller **66** and are out-of-phase with each other so the load ripple current is minimized.

[0047] **FIG. 3C-1** shows one strategy **111** for implementing the synchronization controller **66** shown in **FIG. 3C**, along with resultant waveforms during its operation. A load current pulse is initiated by a logic high signal from a pulse ON/OFF command C **112** with the pulse ON/OFF command **112** staying high for the duration of the output load pulse. A high frequency pulse train (typically 100 kHz to 10 MHz) B **114** from the oscillator **113** is passed by an AND gate **116** and a signal D **117** sent to a shift register **118**. The shift register **118** has "N" parallel outputs **119** and performs the function of dividing the input frequency of signal D **117** by "N" and time shifting each successive output by one input clock cycle. The N-channel one-shot **121** receives these signals **119** and generates output signals SYNC **1122**, SYNC **2123**, through SYNC N **124** as shown. These sync signals **122-124** are spaced (360/N) degrees out-of-phase in order to minimize ripple current in the output load pulse. The output load pulse is terminated when the pulse ON/OFF command **112** is set to logic low. A series of output pulses can be generated with programmable pulse widths and duty cycles by switching the pulse ON/OFF command **112** high and low with the desired timing. These control commands can be generated in several ways, including microprocessor control, discrete digital logic or with a programmable logic device, as is known. Current command signals are generated from current command source **64** as in circuit **40**.

[0048] **FIG. 3C-2** shows the preferred strategy **131** for implementing the synchronization controller **66** along with waveforms which clarify the controller operation. A load current pulse is initiated via a logic high signal from pulse ON/OFF command B **132** with the command staying high for the duration of the output load pulse (i.e. the pulse propagated through the load). A high frequency clock signal labeled C **134** (typically 100 kHz to 10 MHz) is generated by an oscillator **133**. The clock signal C **134** is divided by four in element **137** and sent D **138** to a shift register **139**. The shift register **139** has "N" parallel outputs **141** and performs the standard function of dividing the input frequency by "N" and time shifting each successive output by one cycle. The N-phase digital one-shot **142** receives these signals **141** and generates output signals SYNC **1143**, SYNC **2144** through and including SYNC N **146** as shown. These sync signals **143-146** are spaced (360/N) degrees out-of-phase in order to minimize ripple current in the output load pulse. The output load pulse is terminated when the pulse ON/OFF command **132** is set to a logic low. A series of output pulses can be generated with programmable pulse widths and duty cycles by switching the pulse ON/OFF command **132** high and low with desired timing. These pulse ON/OFF control commands **132** can be generated in several ways, including microprocessor control, discrete digital logic, or with a programmable logic device, as are known.

[0049] Referring now to **FIG. 4**, one will see that the circuit shown in **FIG. 3C** has been reconfigured to permanently connect the load to circuit ground. This configuration **70** is required in some applications for equipment safety or operational reasons. The command controller **71** and sync controller **72** for configuration **70** are the same as for configuration **60** with one modification. Since the power transistors Q1, Q2 through QN are connected to Vb, an isolated transistor driver is needed for each transistor to protect the control circuit from high voltage.

[0050] **FIG. 5** shows embodiment **60** shown in **3**C with outputs isolated. This configuration **80** allows for delivering power pulses to loads that are not or cannot be grounded to the Vb source ground. The command controller **82** and sync controller **81** for configuration **80** are the same as for configuration **60**.

[0051] Lab observations implementing embodiment **40** shown in **FIG. 3A** in working prototypes driving laser diode loads resulted in the following values: (1) pulse amplitude is programmable from 35 amps to 55 amps at 90 volts to 160 volts; (2) pulse width is programmable from 50 microseconds to 5 milliseconds; (3) pulse repetition frequency is

programmable from 1 Hz to 200 Hz; and (4) rise time and fall time are approximately 20 microseconds each with current ripple of +/−12% maximum. The input voltage Vb ranged from 200 volts to 350 volts (see the definitions in the waveform of **FIG. 1A**).

[**0052**] Lab observations implementing embodiment **60** shown in **FIG. 3C** having 5 Buck converter modules and driving laser diode loads resulted in the following values: (1) pulse amplitude is programmable from 90 amps to 140 amps at 90 volts to 160 volts; (2) pulse width is programmable from 50 microseconds to 5 milliseconds; (3) pulse repetition rate is 1 Hz to 200 Hz; (4) rise time and fall time are approximately 20 microseconds each; and (5) current ripple is +/−5% maximum. For this example, the Input voltage Vb ranged from 200 volts to 350 volts (again, see the definitions of the waveform in **FIG. 1A**).

[**0053**] The successful lab prototypes of embodiment **60** with the 5 interleaved Buck converters (N=5) utilized elements having the following values: the oscillator frequency was 600 kHz, the input filter capacitor C**1** was 10 microfarads, inductors L1 through L5 each measured 30 microhenrys, the power transistors (i.e. power MOSFETs) Q**1**-Q**5** and the power diodes D**1**-D**5** each had voltage ratings of 600 volts and current ratings of 50 amps.

[**0054**] The disclosed PFC invention is not limited to the Buck converter topology, but is susceptible to other switching converter topologies used for building DC output power supplies which can be interleaved to form a PFC. These converter topologies include the Forward, Boost, Flyback, Push-Pull, Half-Bridge, Full-Bridge, Sepic and Buck-Boost.

[**0055**] While I have shown my invention in one form, it will be obvious to those skilled in the art that it is not so limited but is susceptible of various changes and modifications without departing from the spirit thereof.

Having set forth the nature of the invention, what is claimed is:

1. A circuit for providing an electrical pulse to a load, comprising:

a. a first Buck converter circuit;

b. a second Buck converter circuit connected to said first Buck converter circuit, each said Buck converter circuit adapted to receive a current command signal for establishing an internal reference voltage within each said Buck converter circuit;

c. means for applying a voltage across said first and said second Buck converter circuits;

d. a capacitor connected in parallel with said voltage means for reducing ripple in said voltage across said first and said second Buck converter circuits; and,

e. a synchronization controller operationally connected to each said Buck converter circuit for initiating electrical pulses in each said Buck converter circuit in interleaved fashion to produce a controllable pulse across said load.

2. A pulse forming circuit as recited in claim 1, wherein each said Buck converter circuit is connected to a common load ground and wherein each said Buck converter circuit includes an isolated transistor driver.

3. A pulse forming circuit as recited in claim 2, wherein said synchronization controller comprises an oscillator responsively enabled via an on/off command signal; a flip flop connected to an output of said oscillator, said flip flop including dual outputs; and a dual one-shot connected to said dual outputs of said flip flop for generating dual interleaved synchronization signal outputs to said two Buck converters.

4. A pulse forming circuit as recited in claim 1, wherein each said Buck converter circuit has an isolated output such that said load is not grounded to said voltage means.

5. A pulse forming circuit as recited in claim 4, wherein each said Buck converter circuit comprises:

a. a load driving transistor;

b. a controller operationally connected to said transistor for switching on said same, said controller adapted to receive said current command signal and operationally connected to said synchronization controller;

c. means operationally connected to said controller for sensing output current levels of said transistor;

d. an inductor operationally connected between said voltage means and said load; and,

e. a diode operationally connected to said voltage means and in parallel with said inductor to permit current flow through said load upon said transistor switching off.

6. A pulse forming circuit as recited in claim 5, wherein said synchronization controller comprises an oscillator responsively enabled via an on/off command signal; a flip flop connected to an output of said oscillator, said flip flop including dual outputs; and a dual one-shot connected to said dual outputs of said flip flop for generating dual interleaved synchronization signal outputs to said two Buck converters.

7. A pulse forming circuit as recited in claim 1, wherein each said Buck converter circuit comprises:

a. a load driving transistor;

b. a controller operationally connected to said transistor for switching on said same, said controller adapted to receive said current command signal and operationally connected to said synchronization controller;

c. means operationally connected to said controller for sensing output current levels of said transistor;

d. an inductor operationally connected between said voltage means and said load; and,

e. a diode operationally connected to said voltage means and in parallel with said inductor to permit current flow through said load upon said transistor switching off.

8. A pulse forming circuit as recited in claim 7, wherein each said transistor controller comprises an RS flip flop connected to said transistor through its Q output; a comparator having inputs connected to said current sensing means and said current command signal, and having its output connected to an R input of said flip flop; and wherein said flip flop has its S input connected to said synchronization controller.

9. A pulse forming circuit as recited in claim 8, wherein said synchronization controller comprises an oscillator responsively enabled via an on/off command signal; a divide by four circuit for dividing said oscillator output by four; a shift register operationally connected to an output of said divide by four circuit and adapted for outputting 1-N pulses

in response to said oscillator output; and an N-phase one-shot circuit for receiving outputs from said shift register and outputting 1-N synchronization signals to each said Buck converter.

10. A pulse forming circuit as recited in claim 9, further including additional 3 to N Buck converter circuits each connected to one another and each adapted to receive a current command signal for establishing an internal reference voltage, and each operationally connected to said synchronization controller for initiating electrical pulses in each said Buck converter circuit in interleaved fashion to produce a controllable pulse across said load.

11. A pulse forming circuit as recited in claim 10, wherein said a load driving transistor comprises a power MOSFET.

12. A pulse forming circuit as recited in claim 10, wherein said a load driving transistor comprises a field effect transistor.

13. A pulse forming circuit as recited in claim 10, wherein said a load driving transistor comprises a bipolar transistor.

14. A pulse forming circuit as recited in claim 1, wherein each said Buck converter circuit comprises:

a. a load driving transistor;

b. a controller operationally connected to said transistor for switching on said same, said controller adapted to receive said current command signal and operationally connected to said synchronization controller;

c. means operationally connected to said controller for sensing output current levels of said transistor;

d. means operationally connected between said voltage means and said load for inducing a current in said load upon switching said transistor off; and,

e. means operationally connected to said voltage means and in parallel with said induction means to provide a current flow path through said load upon said transistor switching off.

15. A pulse forming circuit as recited in claim 14, wherein each said transistor controller comprises an RS flip flop connected to said transistor through its Q output; a comparator having inputs connected to said current sensing means and said current command signal, and having its output connected to an R input of said flip flop; and wherein said flip flop has its S input connected to said synchronization controller.

16. A pulse forming circuit as recited in claim 15, wherein each said Buck converter circuit has an isolated output such that said load is not grounded to said voltage means.

17. A pulse forming circuit as recited in claim 1, further including additional 3 to N Buck converter circuits each connected to one another and each adapted to receive a current command signal for establishing an internal reference voltage, and each operationally connected to said synchronization controller for initiating electrical pulses in each said Buck converter circuit in interleaved fashion to produce a controllable pulse across said load.

18. A pulse forming circuit as recited in claim 17, wherein each said Buck converter circuit comprises:

a. a load driving transistor;

b. a controller operationally connected to said transistor for switching on said same, said controller adapted to receive said current command signal and operationally connected to said synchronization controller;

c. means operationally connected to said controller for sensing output current levels of said transistor;

d. an inductor operationally connected between said voltage means and said load; and,

e. a diode operationally connected to said voltage means and in parallel with said inductor to permit current flow through said load upon said transistor switching off.

19. A pulse forming circuit as recited in claim 18, wherein each said transistor controller comprises an RS flip flop connected to said transistor through its Q output; a comparator having inputs connected to said current sensing means and said current command signal, and having its output connected to an R input of said flip flop; and wherein said flip flop has its S input connected to said synchronization controller.

20. A circuit for providing an electrical pulse to a load, comprising:

a. first means for converting a voltage source into an electrical pulse;

b. second means connected to said first pulse means for converting a voltage source into an electrical pulse, each said pulse means adapted to receive a current command signal for establishing an internal reference voltage within each said pulse means;

c. means for applying a voltage across said first and said second pulse means;

d. means connected to said voltage means for reducing ripple in said voltage across said first and said second pulse means; and,

e. means connected to each said pulse means for initiating an electrical pulse in each said pulse means in synchronous interleaved fashion such that a pulse of desired characteristics is generated across said load.

21. A pulse forming circuit as recited in claim 20, wherein each said pulse means comprises:

a. a load driving transistor;

b. a controller operationally connected to said transistor for switching on said same, said controller adapted to receive said current command signal and operationally connected to said synchronization means;

c. means operationally connected to said controller for sensing output current levels of said transistor;

d. means operationally connected between said voltage means and said load for inducing a current in said load upon switching said transistor off; and,

e. means operationally connected to said voltage means and in parallel with said induction means to provide a current flow path through said load upon said transistor switching off.

22. A pulse forming circuit as recited in claim 21, wherein each said transistor controller comprises an RS flip flop connected to said transistor through its Q output; a comparator having inputs connected to said current sensing means and said current command signal, and having its output connected to an R input of said flip flop; and wherein said flip flop has its S input connected to said synchronization means.

23. A pulse forming circuit as recited in claim 22, wherein said synchronization means comprises an oscillator responsively enabled via an on/off command signal; a divide by four circuit for dividing said oscillator output by four; a shift register operationally connected to an output of said divide by four circuit and adapted for outputting 1-N pulses in response to said oscillator output; and an N-phase one-shot circuit for receiving outputs from said shift register and outputting 1-N synchronization signals to each said pulse means.

24. A pulse forming circuit as recited in claim 23, further including additional 3 to N Buck pulse means each connected to one another and each adapted to receive a current command signal for establishing an internal reference voltage, and each operationally connected to said synchronization means for initiating electrical pulses in each said pulse means in interleaved fashion to produce a controllable pulse across said load.

25. A pulse forming circuit as recited in claim 24, wherein said a load driving transistor comprises a power MOSFET.

26. A pulse forming circuit as recited in claim 24, wherein said a load driving transistor comprises a field effect transistor.

27. A pulse forming circuit as recited in claim 24, wherein said a load driving transistor comprises a bipolar transistor.

28. A pulse forming circuit as recited in claim 20, wherein each said pulse means comprises a converter circuit selected from the group consisting of Forward, Boost, Flyback, Push-Pull, Half-Bridge, Full-Bridge, Sepic, and Buck-Boost.

29. A pulse forming circuit as recited in claim 20, further including additional 3 to N pulse means each connected to one another and each adapted to receive a current command signal for establishing an internal reference voltage, and each operationally connected to said synchronization means for initiating electrical pulses in each said pulse means in interleaved fashion to produce a controllable pulse across said load.

30. A pulse forming circuit as recited in claim 29, wherein each said pulse means comprises:

a. a load driving transistor;

b. a controller operationally connected to said transistor for switching on said same, said controller adapted to receive said current command signal and operationally connected to said synchronization means;

c. means operationally connected to said transistor controller for sensing output current levels of said transistor;

d. an inductor operationally connected between said voltage means and said load; and,

e. a diode operationally connected to said voltage means and in parallel with said inductor to permit current flow through said load upon said transistor switching off.

31. A pulse forming circuit as recited in claim 30, wherein each said transistor controller comprises an RS flip flop connected to said transistor through its Q output; a comparator having inputs connected to said current sensing means and said current command signal, and having its output connected to an R input of said flip flop; and wherein said flip flop has its S input connected to said synchronization means.

32. A circuit for providing an electrical pulse to a load, comprising:

a. a first Buck converter circuit;

b. a second Buck converter circuit connected to said first Buck converter circuit, each said Buck converter circuit adapted to receive a current command signal for establishing an internal reference voltage within each said Buck converter circuit;

c. means for applying a voltage across said first and said second Buck converter circuits;

d. means connected to said voltage means for reducing ripple in said voltage across said first and said second Buck converter circuit; and,

e. wherein each said Buck converter circuit is adapted to receive an interleaved synchronization signal for initiating electrical pulses in each said Buck converter circuit to create a pulse of desired characteristics across said load.

33. A pulse forming circuit as recited in claim 32, wherein each said Buck converter circuit has an isolated output such that said load is not grounded to said voltage means.

34. A pulse forming circuit as recited in claim 33, wherein each said Buck converter circuit comprises:

a. a load driving transistor;

b. a controller operationally connected to said transistor for switching on said same, said controller adapted to receive said current command signal and adapted to receive said synchronization signal;

c. means operationally connected to said controller for sensing output current levels of said transistor;

d. an inductor operationally connected between said voltage means and said load; and,

e. a diode operationally connected to said voltage means and in parallel with said inductor to permit current flow through said load upon said transistor switching off.

35. A pulse forming circuit as recited in claim 34, wherein each said Buck converter circuit is adapted for driving laser diode loads.

36. A pulse forming circuit as recited in claim 35, wherein each said transistor controller comprises an RS flip flop connected to said transistor through its Q output; a comparator having inputs connected to said current sensing means and said current command signal, and having its output connected to an R input of said flip flop; and wherein said flip flop has its S input is adapted to receive said synchronization signal.

37. A pulse forming circuit as recited in claim 32, further including additional 3 to N Buck converter circuits each connected to one another and each adapted to receive a current command signal for establishing an internal reference voltage and each adapted to receive said synchronization signal for initiating electrical pulses in each said Buck converter circuit in interleaved fashion to produce a controllable pulse across said load.

38. A pulse forming circuit as recited in claim 37, wherein each said Buck converter circuit comprises:

a. a load driving transistor;

b. a controller operationally connected to said transistor for switching on said same, said controller adapted to receive said current command signal and adapted to receive said synchronization signal;

c. means operationally connected to said transistor controller for sensing output current levels of said transistor;

d. an inductor operationally connected between said voltage means and said load; and,

e. a diode operationally connected to said voltage means and in parallel with said inductor to permit current flow through said load upon said transistor switching off.

39. A pulse forming circuit as recited in claim 38, wherein each said transistor controller comprises an RS flip flop connected to said transistor through its Q output; a comparator having inputs connected to said current sensing means and said current command signal, and having its output connected to an R input of said flip flop; and wherein said flip flop has its S input adapted to receive said synchronization signal.

40. A circuit for providing an electrical pulse to a load, comprising:

a. first means for converting a voltage source into an electrical pulse;

b. second means connected to said first pulse means for converting a voltage source into an electrical pulse, each said pulse means adapted to receive a current command signal for establishing an internal reference voltage within each said pulse means;

c. means for applying a voltage across said first and said second pulse means;

d. means connected to said voltage means for reducing ripple in said voltage across said first and said second pulse means; and,

e. each said pulse means adapted to receive an interleaved synchronization signal for initiating electrical pulses in each said pulse means to create a pulse of desired characteristics across said load.

41. A pulse forming circuit as recited in claim 40, wherein each said Buck converter circuit comprises:

a. means for driving a load;

b. a controller operationally connected to said load driving means for switching on said same, said controller adapted to receive said current command signal and adapted to receive said synchronization signal;

c. means operationally connected to said controller for sensing output current levels of said load driving means;

d. means operationally connected between said voltage means and said load for inducing a current in said load upon switching said load driving means off; and,

e. means operationally connected to said voltage means and in parallel with said induction means to provide a current flow path through said load upon said load driving means switching off.

42. A pulse forming circuit as recited in claim 41, further including additional 3 to N pulse means each connected to one another and each adapted to receive a current command signal for establishing an internal reference voltage and each adapted to receive said synchronization signal for initiating electrical pulses in each said pulse means in interleaved fashion to produce a controllable pulse across said load.

43. A pulse forming circuit as recited in claim 42, wherein each said pulse means is adapted for driving laser diode loads.

44. A pulse forming circuit as recited in claim 43, wherein each said pulse means has an isolated output such that said load is grounded separately from said voltage means.

45. A pulse forming circuit as recited in claim 44, wherein each said pulse means is connected to a common load ground and wherein each said driving means is isolated from said load.

46. A pulse forming circuit as recited in claim 40, wherein each said pulse means comprises a converter circuit selected from the group consisting of Forward, Boost, Flyback, Push-Pull, Half-Bridge, Full-Bridge, Sepic, and Buck-Boost.

47. A pulse forming circuit as recited in claim 40, further including additional 3 to N pulse means each connected to one another and each adapted to receive a current command signal for establishing an internal reference voltage and each adapted to receive said synchronization signal for initiating electrical pulses in each said pulse means in interleaved fashion to produce a controllable pulse across said load.

48. A pulse forming circuit as recited in claim 47, wherein said driving means comprises a solid-state power switch.

49. A method for creating an electrical pulse across a load, comprising the steps of:

a. applying a voltage across at least two connected Buck converter circuits;

b. providing a reference voltage to control output pulse amplitude for each said Buck converter circuits;

c. applying a synchronization signal in an interleaved manner to each said Buck converter; and,

d. initiating a pulse from each Buck converter responsive to said synchronization pulse for a specified duration such that a pulse of controllable quality is generated across said load.

50. A method as recited in claim 49, wherein said step of initiating a pulse from each Buck converter further comprises controllably summing each pulse generated by each Buck converter to produce a pulse across said load of desirable quality.

51. A method as recited in claim 50, wherein said step of initiation of a pulse from each Buck converter comprises:

a. receiving said synchronization signal into a control element;

b. turning on a load driving element responsive to said reception of said synchronization signal to generate current across said load;

c. sensing current level in an output of said load driving element and generating a current level signal responsive thereof;

d. comparing said current level signal to a reference signal sent to said Buck converter and generating a signal responsive thereof;

e. turning off said load driving element conditionally responsive to said signal generated in said comparing step; and,

f. repeating steps a-e to produce a train of desired pulses from said Buck converter.

52. A method as recited in claim 51, wherein said step of providing a reference voltage to said Buck converter comprises:

a. initiating an oscillator in response to an on/off command signal;

b. receiving a signal into a shifting capable memory element capable of outputting 1-N signals where N is equal to the number of existing Buck converter circuits responsive to signals sent by said oscillator; and,

c. receiving outputs from said shifting capable memory element and issuing synchronization signals from a one-shot circuit element to each of said Buck converters.

53. A method for creating an electrical pulse across a load, comprising the steps of:

a. applying a voltage across at least two connected circuits capable of generating a pulse across a load;

b. providing a reference voltage to control output pulse amplitude for each said pulse circuit;

c. applying a synchronization signal in an interleaved manner to each said pulse circuit; and,

d. initiating a pulse from each pulse circuit responsive to said synchronization pulse for a specified duration such that a pulse of controllable quality is generated across said load.

54. A method as recited in claim 53, wherein said step of initiating a pulse from each pulse circuit further comprises controllably summing each pulse generated by each pulse circuit to produce a pulse across said load of desirable quality.

55. A method as recited in claim 54, wherein said step of initiation of a pulse from each pulse circuit comprises:

a. receiving said synchronization signal into a control element;

b. turning on a load driving element responsive to said reception of said synchronization signal to generate current across said load;

c. sensing current level in an output of said load driving element and generating a current level signal responsive thereof;

d. comparing said current level signal to a reference signal sent to said pulse circuit and generating a signal responsive thereof;

e. turning off said load driving element conditionally responsive to said signal generated in said comparing step; and,

f. repeating steps a-e to produce a train of desired pulses from said pulse circuit.

56. A method as recited in claim 55, wherein said step of providing a reference voltage to said pulse circuit comprises:

a. initiating an oscillator in response to an on/off command signal;

b. receiving a signal into a shifting capable memory element capable of outputting 1-N signals where N is equal to the number of existing pulse circuits responsive to signals sent by said oscillator; and,

c. receiving outputs from said shifting capable memory element and issuing synchronization signals from a one-shot circuit element to each of said pulse circuits.

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