



- (51) **International Patent Classification:**
G11C 13/00 (2006.01) *G11C 11/00* (2006.01)
- (21) **International Application Number:**
PCT/US2015/067241
- (22) **International Filing Date:**
22 December 2015 (22.12.2015)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
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- (81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) **Title:** HIGH PERFORMANCE RRAM

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(57) **Abstract:** Embodiments are directed to a resistive random access memory (RRAM) element that includes a top electrode; a bottom electrode; a dielectric material disposed between the top electrode and the bottom electrode; and a conductive filament in the dielectric material electrically connected to the top electrode, the conductive filament including a first width proximate the top electrode larger than a second width proximate the bottom electrode. In some embodiments, the first width includes a larger number of conductive elements than the second width. A wide filament can be formed for a sleep mode that can maintain a threshold conductance (LRS) under no or low power conditions by having a larger number of conductance elements in the no or low power mode than when in a normal operational mode.

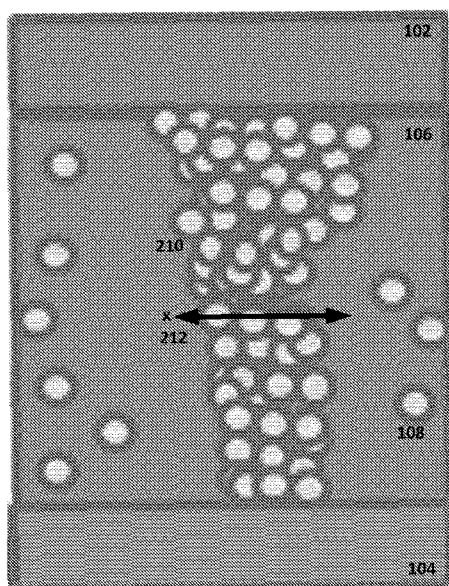


FIG. 2



Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

HIGH PERFORMANCE RRAM

TECHNICAL FIELD

[0001] This disclosure pertains to a high performance resistive random access memory (RRAM), and, more particularly, a high performance RRAM with a sleep mode.

BACKGROUND

[0002] In memory systems, there is often a trade-off between performance and retention. For RRAM, higher performance (faster switching) can occur with a corresponding loss of retention. RRAM designed for non-volatility can experience lower switching performance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. 1 is a schematic diagram of a resistive random access memory element with a formed, thin filament.

[0004] FIG. 2 is a schematic diagram of a resistive random access memory element with a formed, wide filament.

[0005] FIG. 3 is a schematic diagram of a resistive random access memory element with a broken, wide filament.

[0006] FIG. 4 is a schematic diagram of a resistive random access memory element with a reformed filament that is wide near one electrode and thin near the other electrode.

[0007] FIG. 5 is a graphical representation of the voltage and current for forming a wide filament for sleep mode and resetting the wide filament.

[0008] FIG. 6 is a process flow diagram for creating a resistive random access memory element that includes a sleep mode wide filament.

[0009] FIG. 7 is a process flow diagram for operating a resistive random access memory element with a sleep mode.

[0010] FIG. 8 is a schematic block diagram of an interposer implementing one or more embodiments of the disclosure.

[0011] FIG. 9 is a schematic block diagram of a computing device built in accordance with an embodiment of the disclosure.

[0012] FIG. 10 is a schematic block diagram of a controller for operating a resistive random access memory element with a sleep mode.

[0013] FIG. 11 is a schematic diagram of an array of resistive random access memory elements in accordance with embodiments of the present disclosure.

[0014] FIG. 12 is a schematic diagram of a cross section of an array of resistive random access memory elements in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

[0015] In this disclosure, the unique properties of resistive random access memory (RRAM) elements are used to enable bits that can switch between “high performance” states and “non-volatile” states. The non-volatile states can be useful to save battery power during sleep mode while retaining the state of the RRAM element. The sleep mode can achieve a non-volatile state using a formed filament having a width or density larger than an operating filament. The wide filament can be created by applying a higher voltage across the dielectric material to create a larger number of conduction elements that make up the filament than the number used for high performance switching. The resulting “sleep mode” filament can be physically wider than a typical operating filament or can be physically similar in size, while having a higher “density” of conduction elements.

[0016] FIG. 1 is a schematic diagram of a resistive random access memory (RRAM) element 100 with a formed, thin filament. The RRAM 100 includes a first electrode 102 and a second electrode 104. A dielectric 106 is disposed between the first electrode 102 and the second electrode 104. The dielectric 106 can be considered a switching medium in which a conductive path 110, or filament 110, can be formed, set, and reset, thereby facilitating switching the RRAM memory element from a high resistive state (HRS) to a low resistive state (LRS), and vice versa. The filament 110 can be formed and set using voltage of a first polarity and can be broken or reset using voltage of a second polarity, opposite the first polarity. The filament can be an oxygen vacancy filament for an oxide-based dielectric.

[0017] A voltage having a first polarity can be applied across first electrode 102 and the second electrode 104. The voltage of a first polarity can cause the formation of conduction elements 108 within the dielectric 106. For example, for an oxide dielectric, the conduction elements 108 can include oxygen vacancies created by the reduction of oxygen atoms in the dielectric 106 by a voltage having a first polarity being applied across the first electrode 102 and second electrode 104. The conduction elements 108 can form a conduction path between the first electrode 102 and the second electrode 104. The conduction path can

also be referred to as filament 110. The filament 110 can be broken (or reset) by applying a voltage of opposite polarity to oxidize the dielectric 106 to fill the vacancies.

[0018] The filament 110 can have a length defined by the distance between electrodes (e.g., the thickness of the dielectric). The filament 110 can also have a width 112 defined by a number of conduction elements 108 along a direction x substantially perpendicular to the length. The width 112 of the filament 110 is a function of the voltage level applied across the first electrode 102 and the second electrode 104 during formation. For high performance switching, the width is kept small by applying a first voltage level to form the filament and capping the current that flows through the resulting filament to a predetermined value. Keeping the width of the filament small can allow for the use of a lower voltage to form, set, and reset the filament, which makes switching between HRS and LRS fast.

[0019] In some embodiments, the filament 110 can have a tapered shape. The term “tapered” is used to describe a filament that has more conduction elements proximate to the first electrode than there are proximate to the second electrode. The tapered shape promotes fast switching by allowing for fast setting and resetting of the filament as well as a stable filament while in a low resistance state. The relatively few number of conduction elements near one electrode allows for fast setting and resetting; while the relative large number of conduction elements near the other electrode reduces the impact of conduction element drift during the low resistance state.

[0020] For RRAM with a sleep mode or a low power mode, where the memory may go for long periods of time in a LRS state with little or no power, the RRAM element may lose its state because of vacancy drifting. Even a small number of conduction element drift can cause the filament to break or to increase in resistance to a point that inadvertently transitions the RRAM memory element from an LRS to HRS.

[0021] This disclosure describes creating a sleep mode filament that is wider (i.e., more conduction elements 108) than a filament used for high performance switching. The wider sleep mode filament 110 would include more conduction elements 108 along a direction substantially perpendicular to the length of the filament 110.

[0022] FIG. 2 is a schematic diagram of a resistive random access memory (RRAM) element 200 with a formed, wide filament. The RRAM 200 includes similar structural features as RRAM element 100. The RRAM 200 has already had a filament formed, similar to filament 110. In RRAM element 200, a sleep mode filament 210 is been formed to have a

width 212 that is larger than the width 112 of filament 110. The width of filament 210 can be formed by applying a voltage across the first electrode 102 and the second electrode 104 to increase the number of conduction elements 108. The resulting current through the filament 110 will increase to a value beyond the set compliance current (but below the full breakdown level for the dielectric), which indicates the formation of the wide filament 210. This “sleep mode” voltage or “wide filament voltage” $V(t)$ causes more conduction elements to populate the filament than the set voltage $V(s)$, the result being that the effective width 212 of the filament 210 is greater than the width 112 of the high performance filament 110. In some embodiments, the sleep mode voltage $V(t)$ and resulting current $I(t)$ can be substantially higher than a typical set current (e.g., $I(t)$ can be in a range from 250 μA to 1 mA, whereas $I(s)$ is typically in a range from 25 μA to 250 μA).

[0023] The wide filament 210 can retain the LRS after the RRAM element loses power or has to operate under low power or power savings conditions (e.g., for a time period on the order of hours). The larger number of conduction elements 108 that make up the filament 210 allow for some amount of drift without completely compromising the integrity of the filament 210. Therefore, even with some drift, the conductive channel formed by the filament 210 is retained, which retains the LRS of the RRAM element 200.

[0024] FIG. 3 is a schematic diagram of a resistive random access memory (RRAM) element 300 with a broken, wide filament. After returning from sleep mode, the RRAM element 300 may be switched from the LRS to the HRS by applying a voltage to “break” the filament 210. Breaking the filament 210 may include causing oxidation of the dielectric 106 by applying an electric field across the dielectric 106 from the first electrode 102 to the second electrode 104 (or vice versa). Oxidizing the dielectric 106 causes oxygen vacancies to fill by, e.g., moving oxygen atoms into the vacancies of the dielectric structure. When oxygen vacancies are filled at locations in contact with one of the electrodes, the filament 212 will break, resulting in a broken filament 310. The broken filament 310 can be considered highly resistive and forms a high resistive state (HRS) for the memory element 300. The width 312 of the broken filament 310 can be similar to width 212 or can be slightly smaller because of the oxidation process. Additionally, the broke filament 310 can be characterized by a discontinuity 314 in the conductive channel between the two electrodes.

[0025] The voltage needed to break the wide filament $I(tr)$ is larger than a typical reset voltage $V(r)$ by one or two orders of magnitude.

[0026] FIG. 4 is a schematic diagram of a resistive random access memory (RRAM) element 400 with a reformed filament that is wide near one electrode and narrow near the other electrode. The broken wide filament 310 can be “set” using a set voltage $V(s)$ that is lower than the sleep mode voltage $V(t)$. This is because the filament 410 does not require a current level to form the filament across the entire thickness of the dielectric 106. Rather, only a portion of the filament 410 is reformed, such as the portion that was oxidized during the reset procedure.

[0027] The result is a filament 410 that has a shape that is wide 412 through much of its length and is narrow 414 near the second electrode 104. The shape can be described as a tapered shape. The filament 410 can be set and reset using lower voltages, $V(s)$ and $V(r)$, respectively, where $V(s) < V(t)$ and $V(r) < V(tr)$, though clamping reset currents is unnecessary because reset will cause an abrupt drop in current as HRS is entered. The filament 410 can achieve high performance because of the narrow portion 414, which can be switched between LRS and HRS quickly. The filament 410 can also retain the LRS for longer periods of time because of the increased width of the filament 410 along much of its length.

[0028] Typically, filaments can be imaged from the top down by conductive atomic force microscopy or Electron beam Induced Current (EBIC)-like techniques. Filaments can be imaged in cross-section by transmission electron microscopy (TEM) or Atom Probe Microscope techniques. Typically filaments can appear in imaging to be on the order of 10 nm diameter at the wider end and at the narrow end could be as small as 1 nm or even smaller. In length, filaments are as long as the thickness of the memory element dielectric that resides between the electrodes. The so-called “wide filament” described herein can appear in imaging to be larger than 10 nm. The exact size of the wide filament can depend on the formation parameters (e.g., voltage, current, time, etc.).

[0029] Returning to the specific filament 410 of FIG. 4, the size of the widest part can exceed 10 nm, but the narrowest part can be on the order of less than 5 nm or less (i.e., resembling the narrow portions of a typical filament – e.g., that described in FIG. 1).

[0030] In some implementations, the wide filament may include more densely packed vacancies versus a typical filament with less densely packed vacancies. Filaments with more densely packed vacancies would also have different resistance even though the physical size would be same as a typical filament. Imaging a filament with higher density may look the

same as a typical filament, but would have a different electrical response. Electrical characterizations can be used to distinguish a typical filament from a “dense” filament (i.e., a filament with higher density of vacancies than a typical filament).

[0031] A dense filament can also be used to delay the decay of a filament, thereby preserving the low resistance state (LRS) of the memory element. The dense filament would be resilient to vacancy drifting in a similar manner as a “wide” filament. That is, small numbers of vacancy drift will not impact the conductivity of the filament to the point where the memory element conductivity causes a state change from LRS to HRS.

[0032] FIG. 5 is a graphical representation 500 of the voltage and current for forming a wide filament for sleep mode and resetting the wide filament. The filament can be formed using a first voltage $V(f)$. For initial formation of the filament (i.e., a so-called virgin dielectric), the voltage $V(f)$ is sufficiently high to begin dielectric breakdown. A clamp can be used to set a compliance current $I(f)$ once current starts to flow through the formed filament to 1) monitor filament formation for high performance switching and 2) prevent complete dielectric breakdown.

[0033] To reset the filament, a reset voltage $V(r)$ can be applied across the dielectric via the electrodes.. Reset voltage $V(r)$ can be of an opposite polarity than $V(f)$ for a bipolar device, or can be the same polarity for a unipolar device. The reset voltage $V(r)$ causes the RRAM element to enter a high resistive state (HRS) because the reset voltage breaks the filament, which is the conductive channel between the electrodes.

[0034] To set the filament, a set voltage $V(s)$ can be applied across the dielectric via the electrodes. The set voltage $V(s)$ can be lower than forming voltage $V(f)$ because the dielectric has already undergone some dielectric breakdown. The voltage $V(s)$ can cause a current $I(s)$ to flow through the resulting filament. The current $I(s)$ is clamped to prevent full dielectric breakdown while permitting the reformation of a connected filament that can operate with high performance (e.g., fast switching, narrow width). The set voltage causes the RRAM element to enter a low resistive state (LRS) because the set voltage $V(s)$ establishes a conductive channel between the electrodes.

[0035] To help maintain the LRS during sleep modes or low/no power modes, a sleep mode voltage $V(t)$ is applied across the electrodes to form a wide filament. The resulting current $I(t)$ that will flow through the formed wide filament is not clamped at the same value as $I(s)$, but rather is allowed to increase with increasing voltage $V(t)$, and clamped at a

predetermined level $I(t)$, where $I(\text{breakdown}) > I(t) > I(s)$. The result is a wider filament that can retain the LRS in sleep mode or low/no power modes.

[0036] To reset the wide filament, a wide reset voltage $V(\text{tr})$ can be applied across the dielectric via the electrodes. $V(\text{tr})$ can be the same polarity as $V(t)$ for a unipolar device or can be the opposite polarity as $V(t)$ for a bipolar device. The $V(\text{tr})$ is greater than $V(r)$ because of the thickness of the filament; more oxidation is required to break the filament because there are more oxygen vacancies in a wide filament. The current $I(\text{tr})$ will drop as the filament changes from low resistivity to high resistivity, so no current clamping is necessary for reset or thick reset.

[0037] Example current values are as follows: $I(s) = 25\text{-}250\ \mu\text{A}$; $I(t) = 200\ \mu\text{A}$ to 1 mA.

[0038] FIG. 6 is a process flow diagram 600 for creating a resistive random access memory element that includes a sleep mode wide filament. A first electrode is formed (602). The electrode can be a metal, a composite material, or other conductive surface. A dielectric material is formed on the first electrode (604). The dielectric can be an oxide-based dielectric formed by deposition techniques. A second electrode is formed on the dielectric (606). The second electrode can be a metal, a composite material, other conductive surface, semiconductive material or in some cases a non-conductive material.

[0039] A filament can be formed in the dielectric (608). A voltage $V(f)$ can be applied across the electrodes to form a filament. The voltage $V(f)$ can cause a current to pass through the formed filament, which can indicate 1) that the filament has been formed and 2) the conductance behavior of the filament and 3) the size of the filament. The current $I(f)$ can be clamped at a compliance current to prevent full dielectric breakdown. The resulting filament acts as a conductive channel, and has a first width and a length. The length can be defined by the approximate distance between electrodes. The width is defined by a number of conductive elements (e.g., oxygen vacancies) that form in a direction x substantially perpendicular to the length of the filament. For the high performance filament, the width is narrow, meaning that the number of vacancies in the x direction is limited by the compliance current $I(s)$. The formed filament causes the RRAM element to enter into a low resistive state (LRS).

[0040] The RRAM may enter a sleep mode or low power mode. The RRAM element that is in a LRS can mitigate drift by forming a wider filament in the x direction (610). The

wider filament can have sufficient conductive elements in the x direction so that drift of conductive elements out of the filament will not cause the filament to revert to an HRS (e.g., by breaking or otherwise changing the resistivity of the filament above a predetermined threshold value).

[0041] When exiting sleep mode, the wide filament can be read, or the wide filament can be reset (612). To reset the wide filament, a voltage $V(tr)$ can be applied to break the filament.

[0042] FIG. 7 is a process flow diagram 700 for operating a resistive random access memory element with a sleep mode. A first voltage $V(f)$ can be applied to form the filament (702), where the first voltage $V(f)$ causes a current $I(f)$ to flow through the filament. $I(f)$ is clamped at a compliance current $I(cc)$. Voltage $V(t)$ For purposes of this explanation, the formed filament can be considered to have placed the RRAM element in a low resistive state (LRS).

[0043] For entering a sleep mode or low/no power mode, the RRAM can form a wide filament by applying a second voltage $V(t)$ across the electrodes (704). Voltage $V(t)$ can cause the formation of conductive elements in the filament along an x direction. The additional conductive elements allow the filament to maintain the LRS in sleep mode or low/no power modes because the conductive channel can be maintained even when conductive elements drift away from the filament. The voltage $V(t) < V(f)$. The current $I(t)$ is clamped at a higher level as $I(cc)$ to allow for the formation of further conductive elements in the filament ($I(t) > I(f), I(cc)$).

[0044] Upon exiting the sleep mode or low/no power modes, the wide filament can be reset by applying a third (thick reset) voltage $V(tr)$, where $V(tr) > V(t)$. The current $I(tr)$ will drop abruptly when the filament transitions from the LRS to the HRS, so no clamping is necessary.

[0045] For switching from a HRS to a LRS in normal operation (not entering or exiting sleep mode), a fourth voltage (set voltage) $V(s)$ can be applied to reform the filament (708), where the first voltage $V(f)$ causes a current $I(f)$ to flow through the filament. $I(f)$ is clamped at a compliance current $I(cc)$. For purposes of this explanation, the formed filament can be considered to have placed the RRAM element in a low resistive state (LRS).

[0046] The filament can be reset by applying a fifth (reset) voltage $V(r)$, where $V(r) > V(s)$ (710). The voltage $V(r)$ can break the filament, which causes the RRAM element

to switch to a high resistive state (HRS). The current $I(r)$ will drop abruptly when the filament transitions from the LRS to the HRS, so no clamping is necessary for the reset.

[0047] In the this description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present disclosure may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0048] Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0049] The terms “over,” “under,” “between,” and “on” as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer “on” a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0050] Implementations of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may

be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

[0051] FIG. 8 is a schematic block diagram of an interposer implementing one or more embodiments of the disclosure. The interposer 800 is an intervening substrate used to bridge a first substrate 802 to a second substrate 804. The first substrate 802 may be, for instance, an integrated circuit die. The second substrate 804 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 800 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 800 may couple an integrated circuit die to a ball grid array (BGA) 806 that can subsequently be coupled to the second substrate 804. In some embodiments, the first and second substrates 802/804 are attached to opposing sides of the interposer 800. In other embodiments, the first and second substrates 802/804 are attached to the same side of the interposer 800. And in further embodiments, three or more substrates are interconnected by way of the interposer 800.

[0052] The interposer 800 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0053] The interposer may include metal interconnects 808 and vias 810, including but not limited to through-silicon vias (TSVs) 812. The interposer 800 may further include embedded devices 814, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 800.

[0054] In accordance with embodiments of the disclosure, apparatuses or processes disclosed herein may be used in the fabrication of interposer 800.

[0055] FIG. 9 is a schematic block diagram of a computing device built in accordance with an embodiment of the disclosure. The computing device 900 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, some or all of these components are fabricated

onto a single system-on-a-chip (SoC) die. The components in the computing device 900 include, but are not limited to, an integrated circuit die 902 and at least one communications logic unit 908. In some implementations the communications logic unit 908 is fabricated within the integrated circuit die 902 while in other implementations the communications logic unit 908 is fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that is shared with or electronically coupled to the integrated circuit die 902. The integrated circuit die 902 may include a CPU 904 as well as on-die memory 906, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STT-MRAM).

[0056] Computing device 900 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 910 (e.g., DRAM), non-volatile memory 912 (e.g., ROM or flash memory), a graphics processing unit 914 (GPU), a digital signal processor 916, a crypto processor 942 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 920, an antenna 922, a display or a touchscreen display 924, a touchscreen controller 926, a battery 928 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 930, a compass, a motion coprocessor or sensors 932 (that may include an accelerometer, a gyroscope, and a compass), a speaker 934, a camera 936, user input devices 938 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 940 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0057] Computing device 900 may also include a resistive random access memory (RRAM) 950. RRAM 950 may include one or more memory elements (ME) 952. Memory element 952 may be similar to the resistive random access memory element 100.

[0058] The communications logic unit 908 enables wireless communications for the transfer of data to and from the computing device 900. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 908 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16

family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 900 may include a plurality of communications logic units 908. For instance, a first communications logic unit 908 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communications logic unit 908 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0059] In various embodiments, the computing device 900 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 900 may be any other electronic device that processes data.

[0060] FIG. 10 is a schematic block diagram of a system 100 for controlling a resistive random access memory element with a sleep mode. System 100 includes a resistive random access memory (RRAM) 1002. The RRAM 1002 includes an array of RRAM elements, including RRAM element 1 1004, RRAM element 2 1006, through RRAM element N 1008. Each memory element can maintain a resistive state. The resistive state of an RRAM memory element is representative of a binary state of the RRAM element. For example, RRAM element 1 1004 can maintain a low resistive state (LRS), which can be indicative of a binary “ON” state. The LRS in RRAM element 1 1004 can be maintained in a low power or no power mode (or sleep mode) by forming a wide filament that is resilient to conductive element drift. The RRAM element 1 1004 can switch to a high resistive state (HRS), which is indicative of a binary “OFF” state. The HRS can be established by resetting the wide filament and can be maintained by forgoing the application of a voltage across the RRAM element electrodes. The LRS and HRS can be toggled to switch between the two memory states.

[0061] The RRAM element 2 1006 can similarly be toggled between memory states. Each RRAM element in the RRAM 1002 can maintain a state independent of other RRAM elements.

[0062] System 100 also includes a voltage controller 1010. Voltage controller 1010 can be implemented at least partially in hardware to provide voltage to each memory element 1004 for forming, setting, and resetting a filament. The voltage controller 1010 can include a voltage source and one or more circuit elements to regulate voltage and/or cap current applied to the memory element 1004. The voltage controller 1010 can include circuit elements to control the voltage applied for forming, setting, and resetting the narrow, operating filament. The voltage controller 1010 can also include circuit elements to cap the current for forming and resetting sleep mode filament, the current for the wide, sleep mode filament greater than a current cap for a narrow, operating filament. For example, a transistor, such as a MOSFET, can control the current through the memory element during SET program (from high resistance state to low resistance state). High current results in laterally larger filament than smaller current. Typically the memory element 1004 is connected to the drain of MOSFET and voltage V_{gs} (gate to source) of the MOSFET is used to set the proper currents during SET. Higher voltage results in higher current and laterally larger filament.

[0063] In some embodiments, the system 100 can also include a mode controller 1012. The mode controller 1012 can change the operation of the memory from a normal operation to a sleep mode or low power or power saving mode. The mode controller 1012 can toggle the RRAM 1002 from a normal operation to sleep mode, which would cause the voltage controller to apply the sleep mode voltage to create a thick filament (for LRS memory elements 1004). Transitioning to a sleep mode involves creating a wide filament for LRS memory elements by applying a voltage and allowing a higher current cap than for normal operation. The mode controller 1012 can also toggle the RAM 1002 from a sleep mode to a normal operation mode. In normal operation mode, for transitioning from LRS to HRS, the voltage controller 1010 would need to reset the wide filament using a voltage and current capped higher than the normal reset voltage and current cap. In normal operation, to set the filament again to an LRS, the voltage controller 1010 can apply a normal operating voltage and current cap.

[0064] Put simply, the voltage controller 1010 can apply a voltage and current for the following situations:

[0065] 1. forming a filament $V(f)$, $I(f)$

[0066] 2. setting a filament under normal operating conditions $V(s)$, $I(s)$

[0067] 3. resetting a filament under normal operating conditions $V(r)$, $I(r)$

[0068] 4. setting a wide, sleep mode filament $V(t)$, $I(t)$

[0069] 5. resetting the wide, sleep mode filament $V(tr)$, $I(tr)$.

[0070] FIG. 11 is a schematic diagram of an array 1104 of resistive random access memory (RRAM) elements 1102 in accordance with embodiments of the present disclosure. An array 1104 of RRAM memory elements 1102 can be formed on a wafer 1100, such as a silicon wafer. The memory elements 1102 are isolated from each other by an oxide 1106. The array of memory elements 1102 can be the components of an RRAM memory. FIG. 12 is a schematic diagram of a cross section of an array 1200 of resistive random access memory elements in accordance with embodiments of the present disclosure. The array 1200 can include a plurality of RRAM elements 1202 isolated from each other by oxide 1206. Each RRAM element 1202 includes a top electrode, bottom electrode, and dielectric, such as an oxygen exchange layer (OEL). The RRAM element 1202 can be accessed by a metal via 1208 disposed between the RRAM element 1202 and the edge of the wafer. Each metal via 1208 is isolated from each other by an interlayer dielectric (ILD) 1204. The RRAM element 1202 can be accessed from the transistor / silicon side 1212 of the wafer by a metal via 1210 disposed between the transistor / silicon side 1212. The metal vias 1210 are isolated by oxide 1206.

[0071] The following paragraphs provide examples of various ones of the embodiments disclosed herein:

[0072] Example 1 is a resistive random access memory (RRAM) element including a top electrode; a bottom electrode; a dielectric material disposed between the top electrode and the bottom electrode; a conductive filament in the dielectric material electrically connected to the top electrode, the conductive filament including a first width proximate the top electrode larger than a second width proximate the bottom electrode.

[0073] Example 2 may include the subject matter of example 1, wherein the first width includes a larger number of conductive elements than the second width.

[0074] Example 3 may include the subject matter of example 1 or 2, wherein the first width is greater than 10 nanometers.

[0075] Example 4 may include the subject matter of any of examples 1 or 2 or 3, wherein the second width is less than 5 nanometers.

[0076] Example 5 may include the subject matter of any of examples 1 or 2 or 3 or 4, wherein the conductive filament electrically connects the top electrode with the bottom electrode.

[0077] Example 6 may include the subject matter of any of examples 1 or 2 or 3 or 4 or 5, wherein the conductive filament includes a plurality of conductive elements.

[0078] Example 7 may include the subject matter of any of examples 1 or 2 or 3 or 4 or 5 or 6, wherein the plurality of conductive elements includes oxygen vacancies in the dielectric material.

[0079] Example 7 may include the subject matter of any of examples 1 or 2 or 3 or 4 or 5 or 6, wherein the dielectric includes an oxide-based dielectric.

[0080] Example 9 is a resistive random access memory (RRAM) comprising a first RRAM element comprising a dielectric material between a first electrode and a second electrode; and a second RRAM element comprising a dielectric material between a third electrode and a fourth electrode; the first RRAM element comprising a wide conductive channel electrically connecting the first electrode and the second in a low resistive state (LRS); and a second RRAM element in a high resistive state (HRS), wherein the third electrode and the fourth electrode are electrically unconnected.

[0081] Example 10 may include the subject matter of example 9, wherein the second RRAM element comprises a wide conduction channel formed in the dielectric between the third electrode and the fourth electrode, the third electrode and the fourth electrode electrically disconnected.

[0082] Example 11 may include the subject matter of examples 9, wherein the wide conductive channel comprises a tapered shape, wherein the wide conduction channel comprises a larger number of conduction elements proximate the first electrode than a number of conduction elements proximate the second electrode.

[0083] Example 12 may include the subject matter of any of examples 9 or 10 or 11, wherein the RRAM comprises a plurality of RRAM elements, and wherein the plurality of RRAM elements comprises the first and second RRAM elements.

[0084] Example 13 may include the subject matter of any of examples 9 or 10 or 11 or 12, wherein the first RRAM element comprises a wide conductive channel comprising a width greater than 10 nanometers.

[0085] Example 14 is a method for forming a resistive random access memory (RRAM) element, the method including providing a first electrode; providing a dielectric on the first electrode; providing a second electrode on the dielectric, wherein the dielectric is disposed between the first and second electrodes; forming a conductive channel of a first width in the dielectric by applying a first voltage across the first and second electrode, the voltage causing a first current through the formed conductive channel; forming a wide conductive channel of a second width in the dielectric by applying a second voltage across the first and second electrode, the second voltage causing a second current through the formed wide conductive channel, the second current greater than the first current, the second width is greater than the first width.

[0086] Example 15 may include the subject matter of example 14, wherein providing the first electrode includes depositing a metal layer on a substrate.

[0087] Example 16 may include the subject matter of any of examples 14 or 15, wherein the providing the dielectric includes forming an oxide layer on the first electrode.

[0088] Example 17 may include the subject matter of any of examples 14 or 15 or 16, wherein the first voltage includes a set voltage in a first direction, and the first current includes a set current, the method further including breaking the conductive channel by applying a reset voltage across the first and second electrodes, the reset voltage including a direction opposite the first direction, the reset voltage greater than the sleep mode voltage.

[0089] Example 18 may include the subject matter of any of examples 14 or 15 or 16 or 17, wherein the set voltage includes a first polarity and the reset voltage includes a second polarity opposite the first polarity.

[0090] Example 19 may include the subject matter of any of examples 14 or 15 or 16 or 17 or 18, also including setting the conductive channel by applying the set voltage across the first and second electrode.

[0091] Example 20 may include the subject matter of any of examples 14 or 15 or 16 or 17 or 18 or 19, wherein forming the wide conductive channel includes clamping the second current at a value greater than the first current.

[0092] Example 21 is a computing device that includes a processor mounted on a substrate; a communications logic unit within the processor; a memory within the processor; a graphics processing unit within the computing device; an antenna within the computing device; a display on the computing device; a battery within the computing device; a power

amplifier within the processor; a voltage regulator within the processor; and a non-volatile memory. The non-volatile memory includes a resistive random access memory (RRAM) element that includes a top electrode; a bottom electrode; a dielectric material disposed between the top electrode and the bottom electrode; a conductive filament in the dielectric material electrically connected to the top electrode, the conductive filament including a first width proximate the top electrode larger than a second width proximate the bottom electrode.

[0093] Example 22 may include the subject matter of example 21, wherein the first width includes a larger number of conductive elements than the second width.

[0094] Example 23 may include the subject matter of any of examples 21 or 22, wherein the first width is greater than 10 nanometers.

[0095] Example 24 may include the subject matter of any of examples 21 or 22 or 23, wherein the second width is less than 5 nanometers.

[0096] Example 25 may include the subject matter of any of examples 21 or 22 or 23 or 24, wherein the conductive filament electrically connects the top electrode with the bottom electrode.

[0097] Example 26 may include the subject matter of any of examples 21 or 22 or 23 or 24 or 25, wherein the conductive filament includes a plurality of conductive elements.

[0098] Example 27 may include the subject matter of any of examples 21 or 22 or 23 or 24 or 25 or 26, wherein the plurality of conductive elements includes oxygen vacancies in the dielectric material.

[0099] Example 28 may include the subject matter of any of examples 21 or 22 or 23 or 24 or 25 or 26 or 27, further including a voltage controller, the voltage controller including circuitry to provide a current at a first level for forming an operating conductive filament; provide a second current level to form a wide conductive filament; and cap the second current level at a second level for forming a wide conductive filament, the wide conductive filament including more conductive elements than the operating conductive filament.

[0100] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

CLAIMS:

1. A resistive random access memory (RRAM) element comprising:
a top electrode;
a bottom electrode;
a dielectric material disposed between the top electrode and the bottom electrode;
a conductive filament in the dielectric material electrically connected to the top electrode, the conductive filament comprising a first width proximate the top electrode larger than a second width proximate the bottom electrode.
2. The RRAM element of claim 1, wherein the first width comprises a larger number of conductive elements than the second width.
3. The RRAM element of claim 1 or 2, wherein the first width is greater than 10 nanometers.
4. The RRAM element of claim 1 or 2, wherein the second width is less than 5 nanometers.
5. The RRAM element of claim 1, wherein the conductive filament electrically connects the top electrode with the bottom electrode.
6. The RRAM element of claim 1, wherein the conductive filament comprises a plurality of conductive elements.
7. The RRAM element of claim 6, wherein the plurality of conductive elements comprises oxygen vacancies in the dielectric material.
8. The RRAM element of claim 1, wherein the dielectric comprises an oxide-based dielectric.

9. A resistive random access memory (RRAM) comprising:
a first RRAM element comprising a dielectric material between a first electrode and a second electrode; and
a second RRAM element comprising a dielectric material between a third electrode and a fourth electrode;
the first RRAM element comprising a wide conductive channel electrically connecting the first electrode and the second in a low resistive state (LRS); and
a second RRAM element in a high resistive state (HRS), wherein the third electrode and the fourth electrode are electrically unconnected.

10. The RRAM of claim 9, wherein the second RRAM element comprises a wide conduction channel formed in the dielectric between the third electrode and the fourth electrode, the third electrode and the fourth electrode electrically disconnected.

11. The RRAM of claim 9, wherein the wide conductive channel comprises a tapered shape, wherein the wide conduction channel comprises a larger number of conduction elements proximate the first electrode than a number of conduction elements proximate the second electrode.

12. The RRAM of claim 9, wherein the RRAM comprises a plurality of RRAM elements, and wherein the plurality of RRAM elements comprises the first and second RRAM elements.

13. The RRAM of claim 9, wherein the first RRAM element comprises a wide conductive channel comprising a width greater than 10 nanometers.

14. A method for forming a resistive random access memory (RRAM) element, the method comprising:
forming a first electrode;
forming a dielectric on the first electrode;
forming a second electrode on the dielectric, wherein the dielectric is disposed between the first and second electrodes;

forming a conductive channel of a first width in the dielectric by applying a first voltage across the first and second electrode;

forming a wide conductive channel of a second width in the dielectric by applying a second voltage across the first and second electrode, the second voltage larger than the first voltage, the second width is greater than the first width.

15. The method of claim 14, wherein forming the first electrode comprises depositing a metal layer on a substrate.

16. The method of claim 14 or 15, wherein the forming the dielectric comprises forming an oxide layer on the first electrode.

17. The method of claim 14, wherein the first voltage comprises a set voltage in a first direction, and the first current comprises a set current, the method further comprising:

breaking the conductive channel by applying a reset voltage across the first and second electrodes, the reset voltage comprising a direction opposite the first direction, the reset voltage greater than the second voltage.

18. The method of claim 17, wherein the set voltage comprises a first polarity and the reset voltage comprises a second polarity opposite the first polarity.

19. The method of claim 17 or 18, further comprising setting the conductive channel by applying the set voltage across the first and second electrode.

20. The method of claim 14, wherein forming the wide conductive channel comprises clamping a second current caused by the second voltage at a value greater than a first current caused by the first voltage.

21. A computing device comprising:

a processor mounted on a substrate;

a communications logic unit within the processor;

a memory within the processor;

a graphics processing unit within the computing device;
an antenna within the computing device;
a display on the computing device;
a battery within the computing device;
a power amplifier within the processor;
a voltage regulator within the processor; and
a non-volatile memory,

wherein the non-volatile memory comprises:

a resistive random access memory (RRAM) element comprising:

a top electrode;
a bottom electrode;
a dielectric material disposed between the top electrode and the bottom electrode;
a conductive filament in the dielectric material electrically connected to the top electrode, the conductive filament comprising a first width proximate the top electrode larger than a second width proximate the bottom electrode.

22. The computing device of claim 21, wherein the first width comprises a larger number of conductive elements than the second width.

23. The computing device of claim 21 or 22, wherein the first width is greater than 10 nanometers.

24. The computing device of claim 21, wherein the conductive filament electrically connects the top electrode with the bottom electrode.

25. The computing device of claim 21, further comprising a voltage controller, the voltage controller comprising circuitry to:

cap current applied to the RRAM element at a first level for forming an operating conductive filament; and

cap current applied to the RRAM element at a second level for forming a wide conductive filament, the wide conductive filament comprising more conductive elements than the operating conductive filament.

100

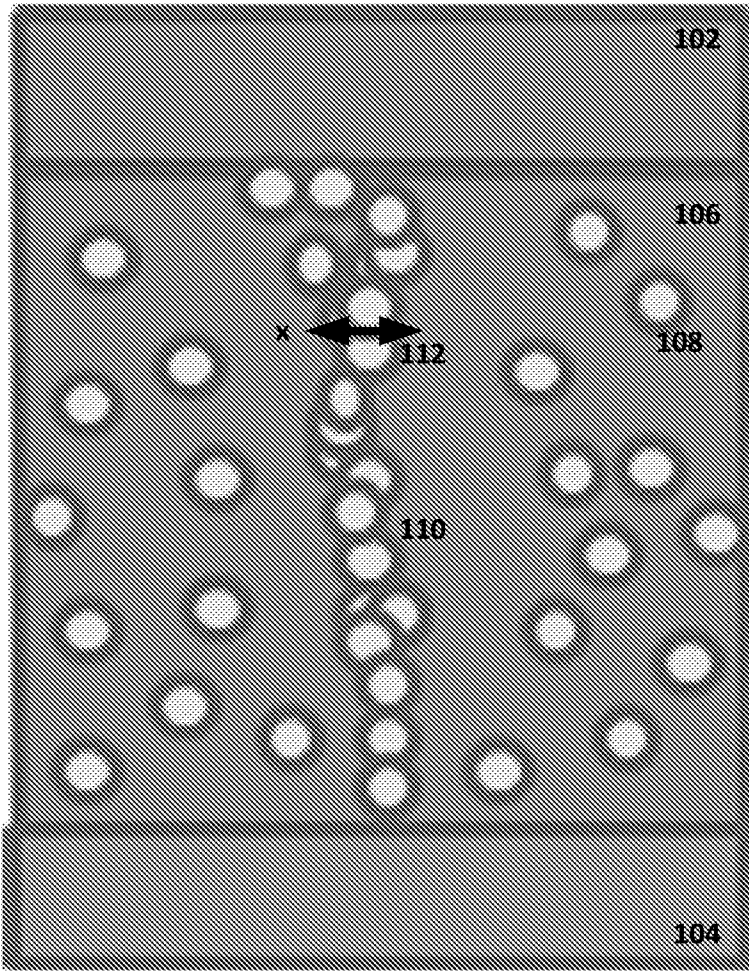


FIG. 1

2/12

100

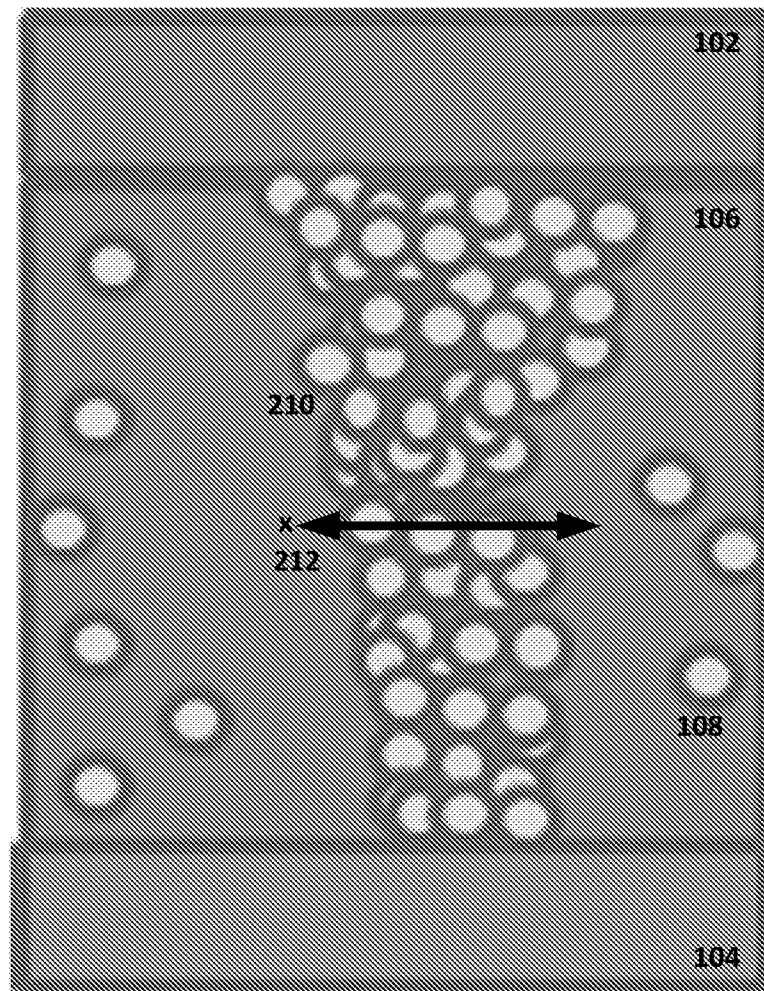


FIG. 2

300

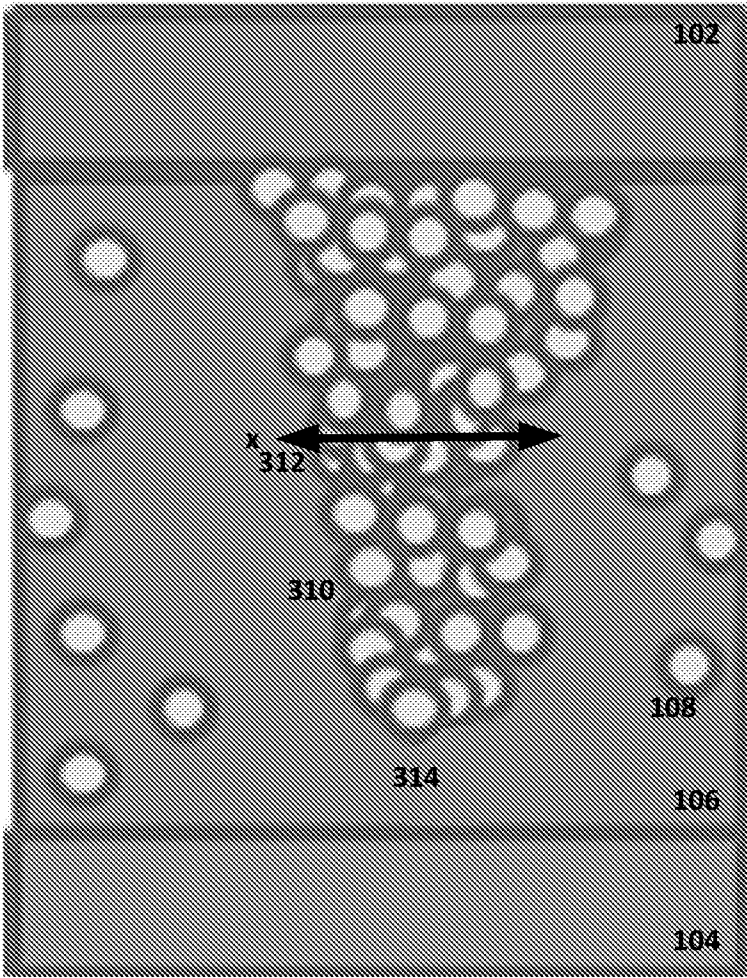


FIG. 3

4/12

400

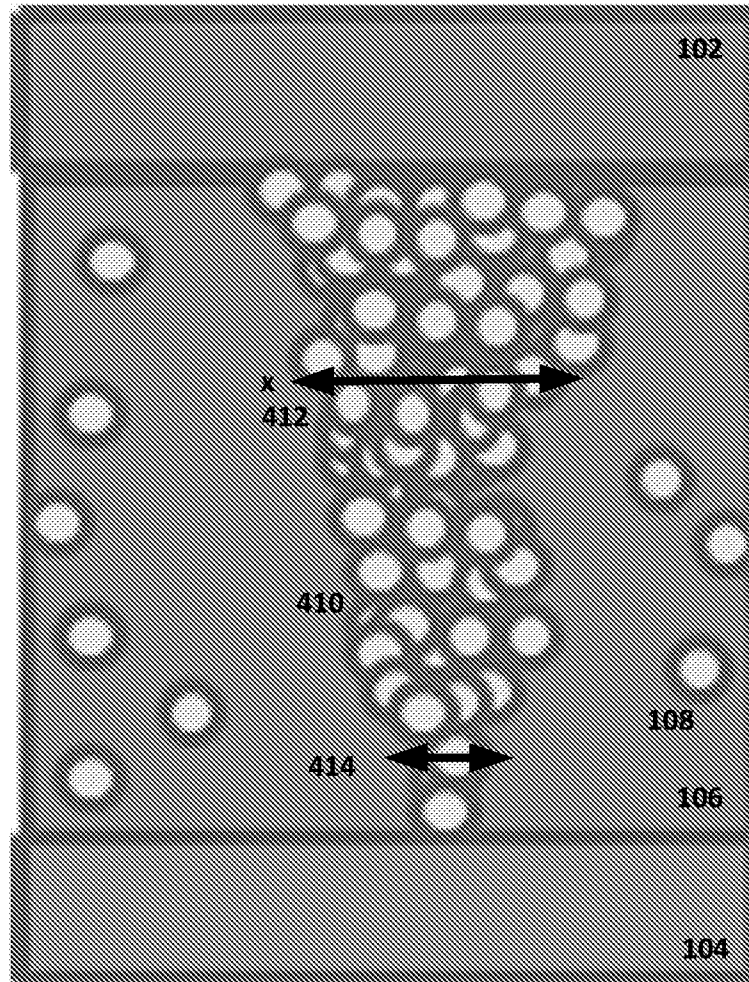


FIG. 4

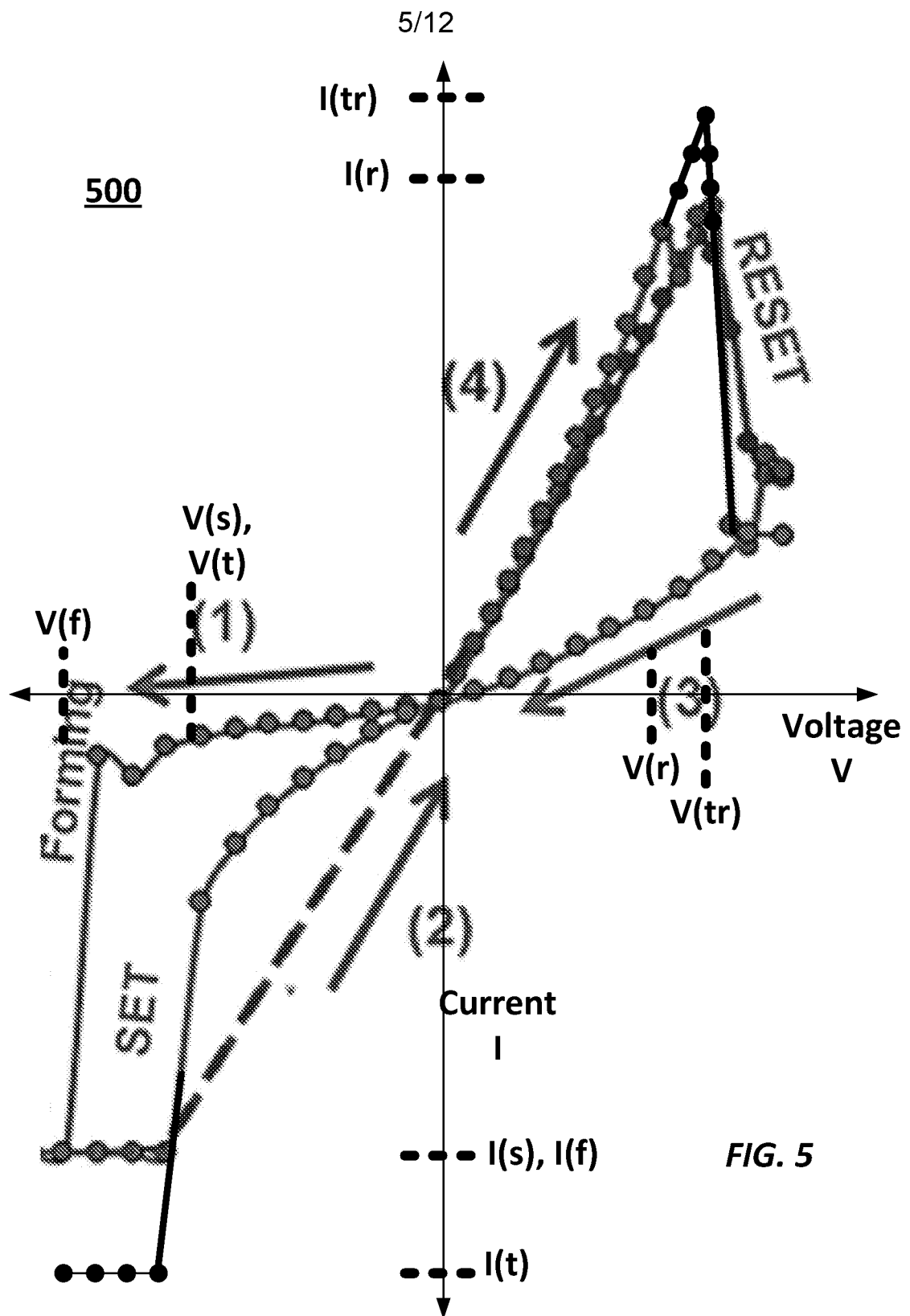
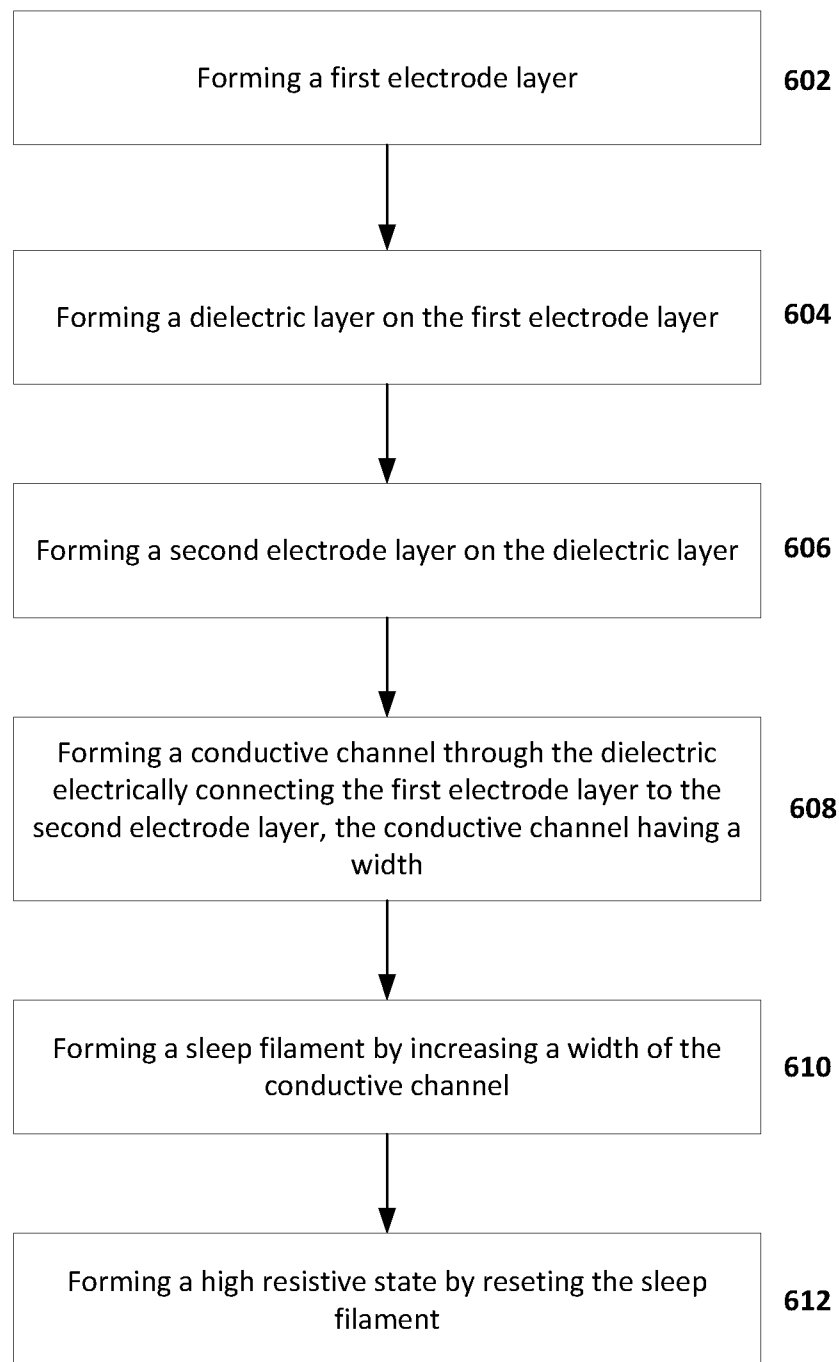
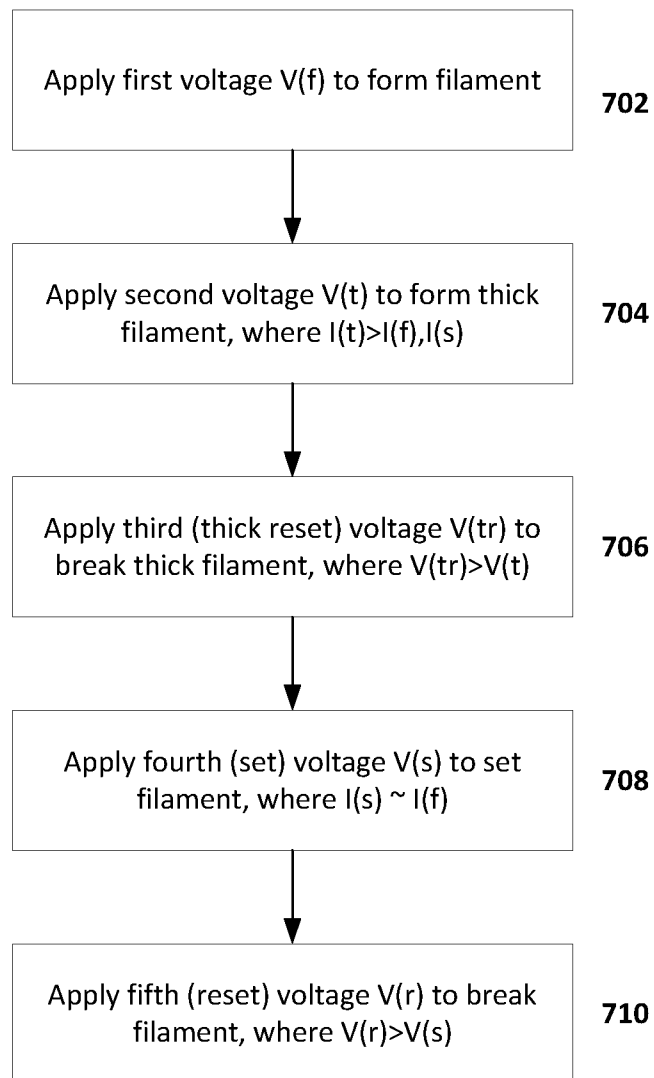


FIG. 5

6/12

600**FIG. 6**

7/12

700**FIG. 7**

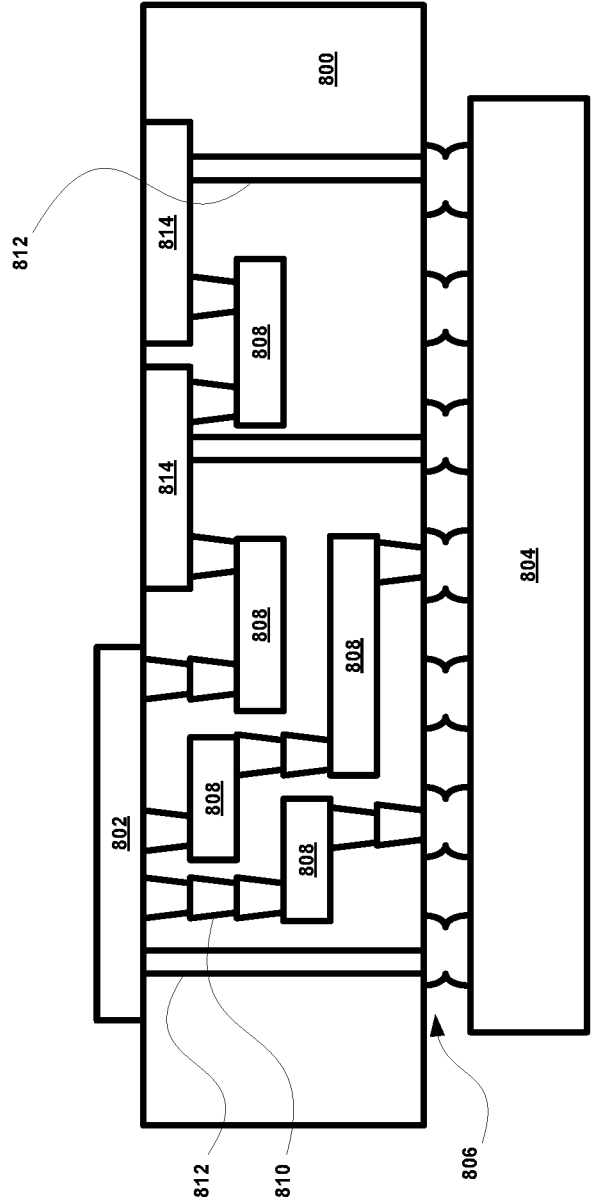
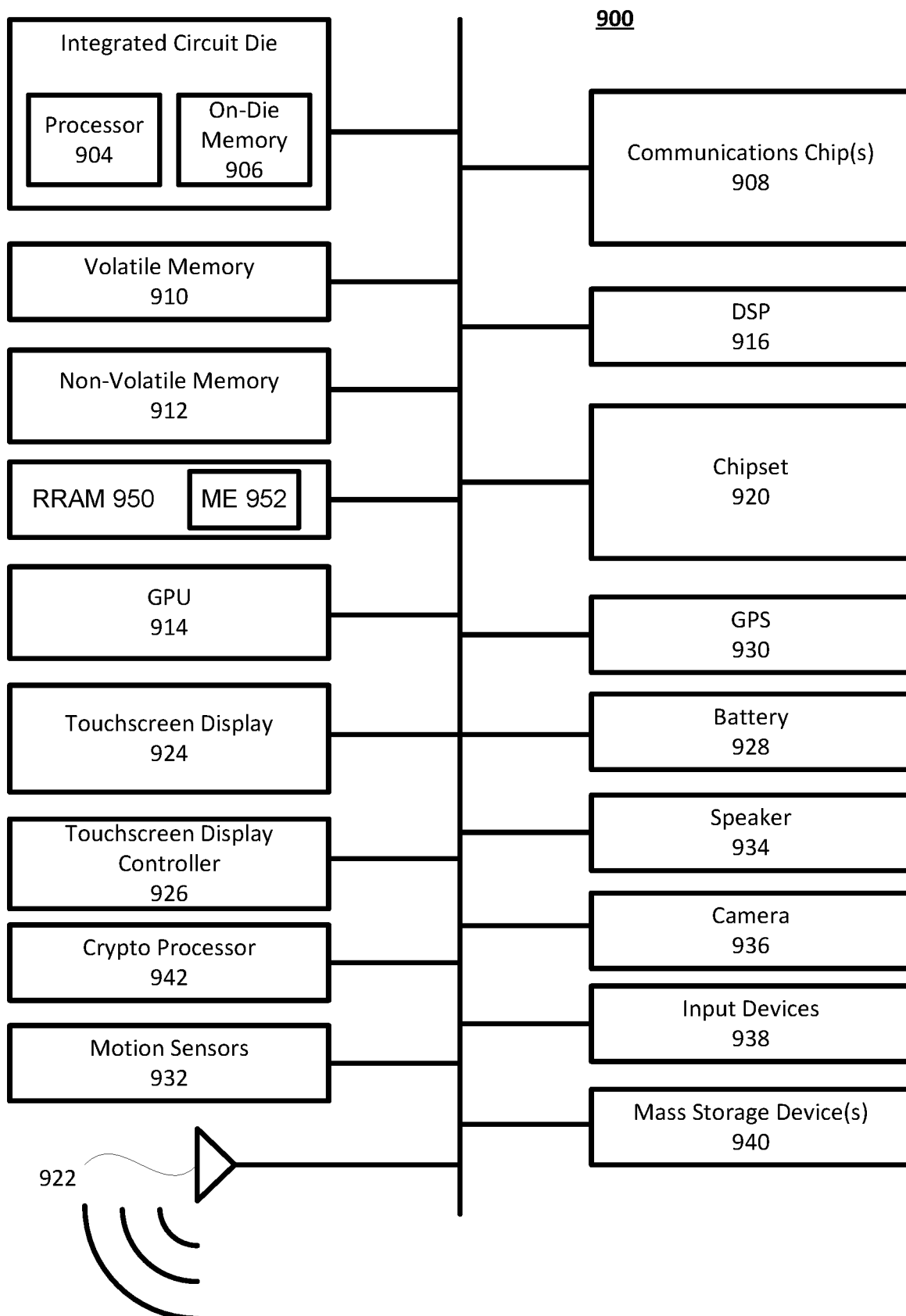


FIG. 8

9/12

**FIG. 9**

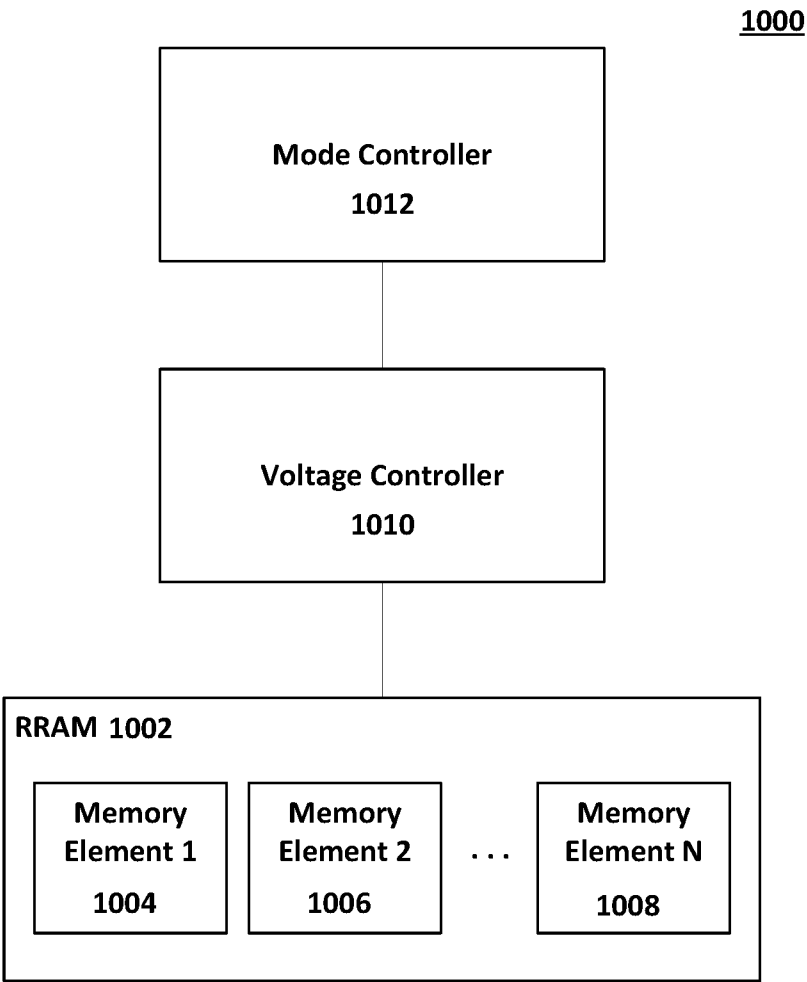


FIG. 10

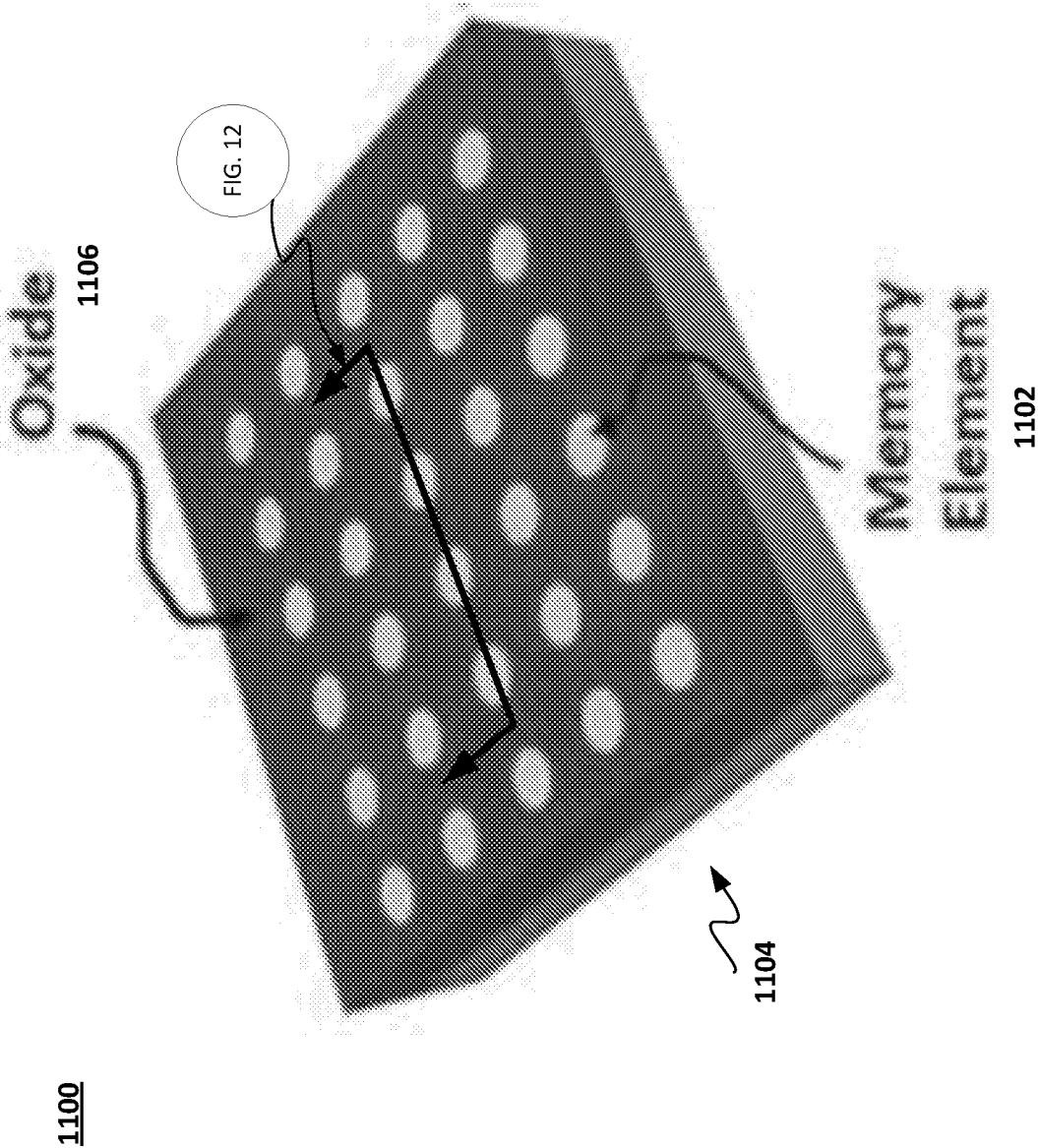


FIG. 11

1200

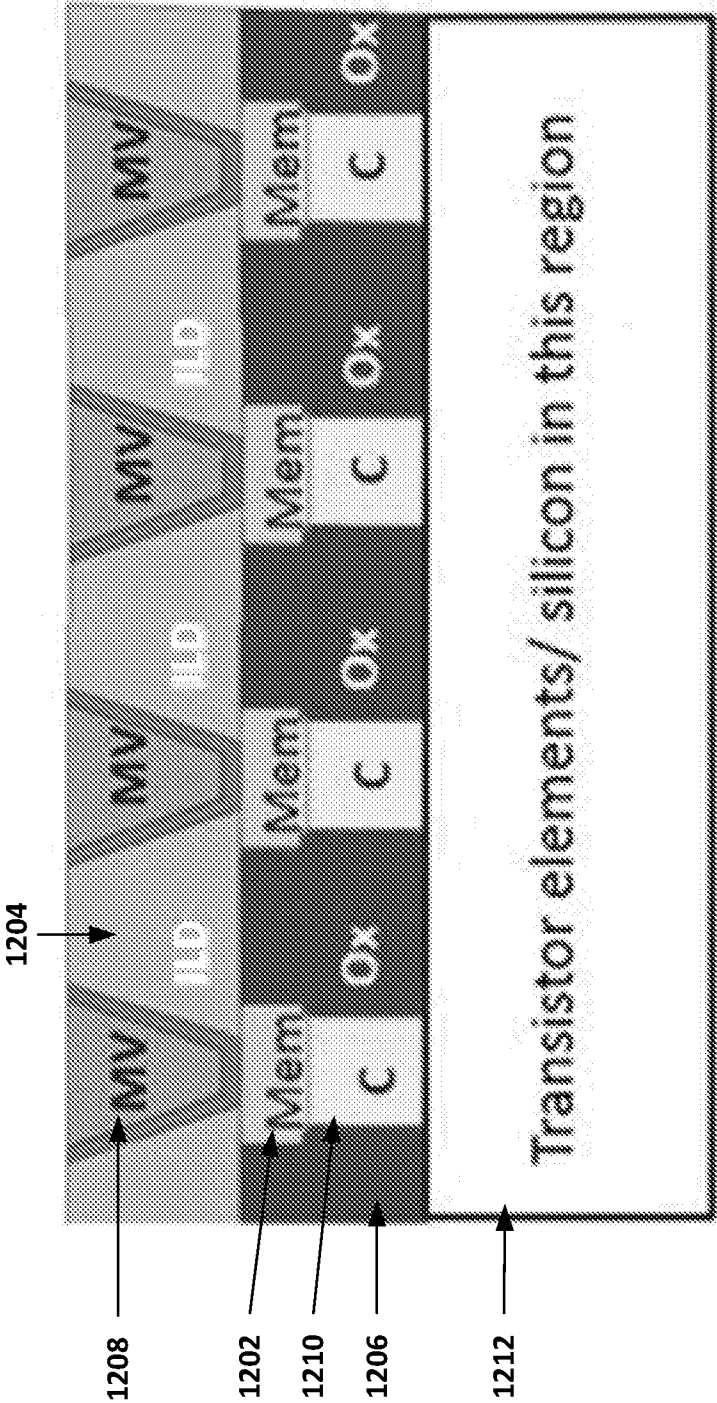


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/067241**A. CLASSIFICATION OF SUBJECT MATTER****G11C 13/00(2006.01)i, G11C 11/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 13/00; H01L 45/00; G11C 11/00; H01L 21/8239; H01L 27/24

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: top, bottom, electrode, dielectric, material, conductive, filament, resistive, memory, RRAM

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2014-0264247 A1 (SONU DARYANANI et al.) 18 September 2014 See paragraph [0006]; and figures 1-2.	1-13, 21-24
A		14-20, 25
Y	US 2014-0353566 A1 (YUN WANG et al.) 04 December 2014 See paragraphs [0006], [0015], [0017]; and figures 1B, 2C-2D.	1-13, 21-24
A	US 2015-0016178 A1 (FEDERICO NARDI et al.) 15 January 2015 See paragraphs [0056]-[0064]; and figure 2.	1-25
A	US 2014-0056053 A1 (DURAI VISHAK NIRMAL RAMASWAMY et al.) 27 February 2014 See paragraphs [0048]-[0049]; and figures 8A-8B.	1-25
A	US 2014-0077149 A1 (FREDERICK T. CHEN et al.) 20 March 2014 See paragraphs [0030]-[0032]; and figures 3A-3D.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

24 August 2016 (24.08.2016)

Date of mailing of the international search report

24 August 2016 (24.08.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/067241

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