

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
24 March 2005 (24.03.2005)

PCT

(10) International Publication Number
WO 2005/027348 A1

(51) International Patent Classification⁷: **H03K 19/082**,
19/094

(21) International Application Number:
PCT/US2004/027499

(22) International Filing Date: 24 August 2004 (24.08.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/656,051 5 September 2003 (05.09.2003) US

(71) Applicant (for all designated States except US):
FREESCALE SEMICONDUCTOR, INC. [US/US];
6501 William Cannon Drive West, Austin, TX 78735 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **CHUN, Christopher, K.** [US/US]; 8810 Grape Cove, Austin, TX 78717 (US).

(74) Agents: **KING, Robert, L.** et al.; Corporate Law Department, Intellectual Property Section, 7700 West Parmer Lane, MD: TX32/PL02, Austin, TX 78729 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

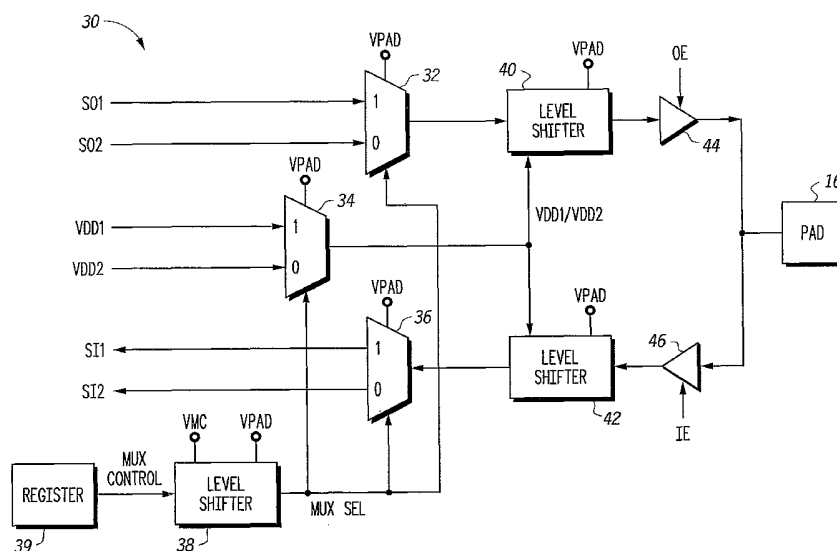
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

[Continued on next page]

(54) Title: MULTIPLEXING OF DIGITAL SIGNALS AT MULTIPLE SUPPLY VOLTAGES IN AN INTEGRATED CIRCUIT



(57) Abstract: An integrated circuit (10) includes a multiple voltage digital multiplexer circuit (30) for multiplexing digital signals provided at different supply voltage levels. In one form, the multiplexer (30) includes an analog multiplexer (32) for receiving the digital signals, a level shifter (40) coupled to the output of the analog multiplexer (32), and a supply voltage multiplexer (34) for providing one of various supply voltages used on the IC corresponding to the signals being multiplexed. A control circuit (38, 39) is used to control the input selection of the analog multiplexer (32) as well as the supply voltage multiplexer (34) for providing the correct supply voltage to the level shifter (40). This provides the ability to multiplex digital signals of differing voltage levels onto a single pad on the IC (10).



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

MULTIPLEXING OF DIGITAL SIGNALS AT MULTIPLE SUPPLY VOLTAGES IN AN INTEGRATED CIRCUIT

FIELD OF THE INVENTION

5

This invention relates to generally to integrated circuits (ICs), and more particularly, to multiplexing digital signals at multiple supply voltage levels in an integrated circuit.

10

BACKGROUND OF THE INVENTION

15

20

25

In integrated circuit (IC) manufacturing, a semiconductor die is provided with terminals, commonly referred to as pads, for communicating with a user or other circuits in an application. The die may be housed in a package having user accessible terminals for mounting on a substrate or a printed circuit board. Various methods are used to couple the die pads to the terminals of the package, such as for example, wirebonds or solder balls. Frequently, complex integrated circuit designs incorporate more functions on a single integrated circuit die than can easily be coupled to the user accessible terminals, or pins, on the integrated circuit package housing the die. In some cases, the various signals on the integrated circuit die can be multiplexed to the user accessible terminals using simple digital multiplexers. However, many ICs today include digital circuits requiring more than one supply voltage. For example, a digital signal from one part of the IC may be from a circuit operating from one supply voltage level (for example 1.0 volt), and a digital signal from another part of the IC may be from a circuit operating at another supply voltage level (for example 1.6 volts). Because of the difference in supply voltage levels, a simple digital multiplexer may not be able to reliably multiplex these signals.

Therefore, there is a need for a multiplexing circuit in an IC that can multiplex digital signals that are provided at different supply voltage levels.

BRIEF DESCRIPTION OF THE DRAWINGS

5

FIG. 1 illustrates, in block diagram form, an integrated circuit die having a multiple voltage multiplexer in accordance with the present invention.

FIG. 2 illustrates, in block diagram form, the multiplexer of FIG. 1 in more detail.

10

FIG. 3 illustrates, in schematic diagram form, a level shifter of the multiplexer of FIG. 2.

FIG. 4 illustrates, in schematic diagram form, an analog multiplexer circuit of the multiplexer of FIG. 2.

15

FIG. 5 illustrates, in block diagram form, a wireless device including the integrated circuit of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

20

Generally, the present invention provides a multiplexer circuit that can multiplex digital signals provided at different supply voltage levels. The multiplexer circuit includes an analog multiplexer for receiving the digital signals, a level shifter coupled to the output of the analog multiplexer, and a supply voltage multiplexer for providing one of various supply voltages used on the IC corresponding to the signals being multiplexed. A control circuit is used to control the input selection of the analog multiplexer as well as the supply voltage multiplexer for providing the correct supply voltage to the level shifter. This provides the ability to multiplex digital signals of differing voltage levels onto a single pad on the IC.

FIG. 1 illustrates, in block diagram form, an integrated circuit die 10 having a multiple voltage multiplexer 30 in accordance with the present invention. In the illustrated embodiment, integrated circuit die 10 includes a digital signal processor (DSP) core 12, an application processor (AP) core 14, and a plurality of pads. DSP core 12 and AP core 14 operate independently of each other. Also, DSP core 12 and AP core 14 may operate at one or more supply voltage levels (1.6, 1.4, 1.2, and 1.0 volts). The plurality of pads are arranged around a perimeter of IC 10, and are user accessible terminals for providing electrical connections for the various signals and supply voltages communicated to and from IC 10. In FIG. 1, the plurality of pads include a representative input/output (I/O) pad 16, and representative power supply pads 18, 20, 22, 24, and 26. Power supply pad 18 receives a power supply voltage labeled "VPAD", power supply pad 20 is coupled to ground and labeled "VSS1", power supply pad 22 is coupled to receive a power supply voltage labeled "VDD1", power supply pad 24 is coupled to receive a power supply voltage labeled "VDD2", and power supply pad 26 is coupled to ground and labeled "VSS2". As illustrated in FIG. 1, DSP core 12 may operate at 1.6 volts, 1.4 volts, 1.2 volts, and 1.0 volt depending on the operating mode. Likewise, AP core 14 may operate at 1.6 volts, 1.4 volts, 1.2 volts, and 1.0 volt depending on the operating mode. Furthermore, DSP core 12 and AP core 14 may operate at different supply voltage levels at the same time.

Integrated circuit 10 may include many more signals than there are external pins available on a package. For example, in one embodiment, IC 10 may include 500 or more signals to be multiplexed to only 300 pins. FIG. 1 illustrates only one simple example of multiple signals being multiplexed to one pin in accordance with the present invention. In the example illustrated in FIG. 1, DSP core 12 includes a plurality of signal lines 15 for conducting a plurality of digital signals at a supply voltage level of 1.2 volts. AP core 14

includes a plurality of signal lines 17 for conducting a plurality of digital signals at a supply voltage level of 1.4 volts. Generally, a digital signal is a “rail-to-rail” signal. That is, if the digital signal is provided from a circuit operating with a supply voltage of, for example, 1.4 volts, then a logic “one” is a 1.4 volt signal and a logic “zero” is a zero volt signal. The pluralities of signal lines 15 and 17 are coupled to input and output terminals, as the case may be, of multiple voltage multiplexer 30. Multiplexer 30 selectively controls which one of the pluralities of signals 15 and 17 communicates via I/O pad 16, and performs a voltage translation from the internal voltage, such as for example, 1.2 or 1.4 volts, to 2.5 volts. The operation of multiplexer circuit 30 will be described in more detail below.

Note that integrated circuit die 10 may include additional circuitry (not shown). In the illustrated embodiment, IC 10 is a baseband integrated circuit for wireless devices. In the case of a wireless device, the additional circuitry may include, for example, one or more memories, display control circuits, timers, debug and test circuits, analog circuits, etc. In other embodiments, IC 10 may include circuitry other than a DSP core and an AP core. Or, the IC may have only one core. Also, the IC may be, for example, an application specific integrated circuit (ASIC) having circuit portions that operate at one supply voltage level and circuit portions that operate at another supply voltage level. In addition, the IC may include different memory types that require different voltage levels.

FIG. 2 illustrates, in block diagram form, multiple voltage multiplexer 30 of FIG. 1 in more detail. Multiple voltage multiplexer 30 includes analog multiplexers 32, 34, and 36, level shifters 38, 40, and 42, register 39, output buffer 44, input buffer 46, and pad 16. Each of analog multiplexers 32, 34, and 36, input buffer 46, output buffer 44, and a portion of level shifters 38, 40, and 42 are supplied by power supply voltage VPAD. An output path includes

analog multiplexer 32, level shifter 40 and output buffer 44. Analog multiplexer 32 receives digital output signals labeled "SO1" and "SO2". Signals SO1 and SO2 may be from DSP core 12 or from AP core 14, or from another circuit (not shown) of IC 10. In the illustrated embodiment, SO1 is from a circuit operating at supply voltage VCC1, and SO2 is from a circuit operating at supply voltage VCC2. In other embodiments, digital signals SO1 and SO2 may be from circuits supplied with the same supply voltage or from circuits supplied by different supply voltages.

A control terminal of analog multiplexer 32 receives a multiplexer select signal labeled "MUX SEL". The MUX SEL signal determines which of digital signals SO1 and SO2 are coupled to the output of analog multiplexer 32. The output terminal of analog multiplexer 32 is coupled to an input of level shifter 40. In addition to controlling analog multiplexers 32 and 36, the MUX SEL signal is provided to the control terminal of multiplexer 34 for setting the voltage level of portions of level shifters 40 and 42 (see FIG. 3), where the voltage level corresponds to the supply voltage level of the selected digital signal SO1 or SO2, that is, supply voltage VCC1 or supply voltage VCC2.

A programmable register 39 is used to provide a control signal labeled "MUX CONTROL" to control the multiplexers and level shifters. Signal MUX SEL depends on signal MUX CONTROL. That is, the logic level of the MUX SEL signal is determined by the MUX CONTROL signal. Note that level shifter 38 is optionally provided because the MUX CONTROL signal may originate from a circuit having a different supply voltage than VPAD.

Programmable register 39 may include one or more bits, each bit for selecting from one or more voltage levels. In the illustrated embodiment, the voltage level of level shifters 40 and 42 is set by selecting one of VDD1 or VDD2 via analog multiplexer 34. For example, if signal SO1 is selected at multiplexer 32, then supply voltage VDD1 will be provided to level shifter 40. Likewise, if

signal SO2 is selected at multiplexer 32, then supply voltage VDD2 will be provided to level shifter 40. Level shifter 38 is similar to level shifters 40 and 42, and will be discussed below in more detail in the discussion of FIG. 3. The operation of analog multiplexer 32 will be discussed below in more detail in the discussion of FIG. 4.

Still referring to FIG. 2, the level shifted digital signal from level shifter 40 is provided to an input of buffer circuit 44, and in response, a buffered digital signal at the VPAD power supply voltage is provided to pad 16 when output enable signal OE is asserted.

Similarly, an input path of multiplexer 30 includes input buffer 46, level shifter 42, and analog multiplexer 36. Note that in the illustrated embodiment, analog multiplexer 36 performs a de-multiplexing function. A digital input signal is received at pad 16 at the pad voltage level VPAD. The digital input signal is provided to an input of input buffer circuit 46. A buffered input signal is provided at the output of buffer 46 to an input of level shifter 42 when input enable signal IE is asserted. Input enable signal IE and output enable signal OE are provided by control circuitry that is not shown. Control signal MUX SEL, which is derived from control signal MUX CONTROL, as discussed above, selects an output of multiplexer 36, either SI1 or SI2. Also, the MUX SEL signal selects the corresponding supply voltage, either VDD1 or VDD2, via multiplexer 34. A level shifted digital signal at the proper voltage level is then provided to internal circuits of IC 10 via analog de-multiplexer 36.

Note that the multiplexers 32 and 34 of FIG. 2 each have two inputs and de-multiplexer 36 had two outputs. In other embodiments, the multiplexers and de-multiplexers may have more than two inputs or outputs, respectively, depending on the number signals to be multiplexed and on the number of possible supply voltages used by the multiplexed signals.

FIG. 3 illustrates, in schematic diagram form, one embodiment of level shifter 40 of the multiplexer of FIG. 2. Note that level shifters 38 and 42 are similar to level shifter 40. Level shifter 40 includes inverter 50, P-channel transistors 52 and 54, and N-channel transistors 56 and 58. Inverter 50 receives either VDD1 or VDD2 as a supply voltage as determined by control MUX SEL. The particular supply voltage corresponds to the voltage level of a digital signal being provided from the output of multiplexer 32. Transistors 52, 54, 56, and 58 form an amplifier. The amplifier is coupled to the power supply voltage VPAD. An output of the amplifier is coupled to input buffer 44 (see FIG. 2). Using level shifter 40, a signal at voltage level VDD1 or VDD2 is translated, or level shifted to voltage level VPAD. In the illustrated embodiment, VDD1 and VDD2 are at a lower voltage potential than VPAD, however, in other embodiments, VDD1 and VDD1 may be at a higher voltage potential.

In the case where a digital signal from multiplexer 32 is a logic high voltage from a circuit being supplied by, for example, VCC1, inverter 50 provides a logic low voltage to the gate of N-channel transistor 56. N-channel transistor 56 is substantially non-conductive or "OFF". The gate of N-transistor 58 is supplied with the logic high voltage from multiplexer 32 at VCC1 and N-channel transistor 58 is conductive or "ON". The gate of P-channel transistor 52 is pulled low through transistor 58, causing P-channel transistor 52 to be ON, thus pulling the output of the amplifier up to a logic high equal to about voltage VPAD.

Conversely, if the digital signal from multiplexer 32 is a logic low, N-channel transistor 56 is "ON" and N-channel transistor 58 is "OFF". The gate of P-channel transistor 54 is pulled low through transistor 56, causing P-channel transistor 54 to be ON. The gate of P-channel transistor 52 is pulled high through P-channel transistor 54, causing P-channel transistor 52 to be

OFF. The output of the amplifier is pull to a logic low through N-channel transistor 56.

Level shifter 40, as illustrated in FIG. 3, is just one example of a level shifter that can be used with multiplexer circuit 30. In other embodiments, a different type of level shifter may be used for translating a digital signal from one voltage level to another voltage level.

FIG. 4 illustrates, in schematic diagram form, one embodiment of analog multiplexer circuit 32 of multiplexer 30 of FIG. 2. Analog multiplexers 34 and 36 are similar to analog multiplexer 32. Analog multiplexer 32 includes inverters 64, 66, and 68, and transmission gates 60 and 62. Transmission gates 60 and 62 each comprise parallel-connected N-channel and P-channel transistors. Each of the inverters is a conventional CMOS (complementary metal oxide semiconductor) inverter supplied by power supply voltage VPAD. When the MUX SEL signal is a logic high voltage, transmission gate 60 is conductive and transmission gate 62 is substantially non-conductive. Digital signal SO1 is communicated to the input of level shifter 40. Also, when the MUX SEL signal is a logic low voltage, transmission gate 60 is substantially non-conductive and transmission gate 62 is conductive. Digital signal SO2 is communicated to the input of level shifter 40. The use of transmission gates 60 and 62 allow digital signals SO1 and SO2 to be transmitted without a threshold voltage drop. Note that in some embodiments, single transistor "pass" gates may be substituted for transmission gates 60 and 62.

FIG. 5 illustrates, in block diagram form, a wireless device 72 including integrated circuit 10. Wireless device 72 includes an RF (radio frequency) IC 76, a power management IC 74 in addition to integrated circuit 10. In the illustrated embodiment, wireless device 72 is a cellular telephone. In other embodiments, wireless device 72 may be any type of 2-way radio, such as for example, a walkie-talkie, 2-way pager, PDA (personal digital assistant), or

personal computer, or any device for providing voice and/or data transmitting and/or receiving functions.

The present invention, as described herein, provides the ability to multiplex digital signals of differing voltage levels onto a single pad of an IC.

5 Various changes and modifications to the embodiments herein chosen for purposes of illustration will readily occur to those skilled in the art. For example, variations in the types of conductivities of transistors, the types of transistors, etc. may be readily made. To the extent that such modifications and variations do not depart from the scope of the invention, they are intended to be
10 included within the scope thereof, which is assessed only by a fair interpretation of the following claims.

CLAIMS

What is claimed is:

1. An integrated circuit die comprising:

a first digital signal line coupled to a first circuit receiving a first power
supply voltage;

a second digital signal line coupled to a second circuit receiving a second
power supply voltage;

a level shifter having a signal terminal and a supply voltage terminal;

means for selecting one of at least the first digital signal line and the

second digital signal line to be coupled to the signal terminal of the
level shifter; and

means for selecting one of at least a first voltage dependent upon the first
power supply voltage and a second voltage dependent upon the
second power supply voltage to supply the supply voltage terminal,
wherein the first voltage is selected when the first digital signal line
is selected to be coupled to the signal terminal of the level shifter
and the second voltage is selected when the second digital signal
line is selected to be coupled to the signal terminal of the level
shifter.

2. The integrated circuit of claim 1 wherein the first digital signal line is an
output signal line of the first circuit and the second digital signal line is an
output signal line of the second circuit.

3. The integrated circuit die of claim 1 further comprising:

a third digital signal line coupled to the first circuit;

a fourth digital signal line coupled to the second circuit;

a second level shifter having a signal terminal and a supply voltage
5 terminal; and

means for selecting one of at least the third digital signal line and the

fourth digital signal line to be coupled to the signal terminal of the

second level shifter, wherein the third digital signal line is selected

when the first voltage is selected and the fourth digital signal line is

10 selected when the second voltage is selected;

wherein the first voltage is supplied to the supply voltage terminal of the

second level shifter when the first voltage is selected and the second

voltage is supplied to the supply voltage terminal of the second

level shifter when the second voltage is selected.

- 15 4. An integrated circuit die comprising:

a multiplexer having a first terminal coupled to a first digital signal line

that when at a first state is at a voltage dependent upon a first power

supply voltage, a second terminal coupled to a second digital signal

line that when at a first state is at voltage dependent upon a second

20 power supply voltage, and a third terminal, the multiplexer

receiving a control signal, the multiplexer coupling its third

terminal to one of at least its first terminal or its second terminal

based upon the control signal;

a level shifter having a first signal terminal coupled to the third terminal

25 of the multiplexer, a second signal terminal coupled to a third

circuit, and a voltage supply terminal; and

a second multiplexer having a first terminal coupled to receive a voltage dependent upon the first power supply voltage, a second terminal coupled to receive a voltage dependent upon the second power supply voltage, and a third terminal coupled to the voltage supply terminal of the level shifter, the second multiplexer receiving a second control signal, wherein the second multiplexer provides at its third terminal a voltage of one of at least a voltage of its first terminal or a voltage of its second terminal based upon the second control signal.

- 5
- 10 5. The integrated circuit die of claim 4 wherein the level shifter includes a second supply terminal coupled to receive a third voltage that is different from a voltage provided to the supply terminal of the level shifter.
6. The integrated circuit of claim 4 wherein the first multiplexer and the second multiplexer are characterized as being analog multiplexers.
- 15 7. The integrated circuit of claim 4 further comprising:
a third multiplexer having a first terminal coupled to a third digital signal line that when at a first state is at a voltage dependent upon the first power supply voltage, a second terminal coupled to a fourth digital signal line that when at a first state is at a voltage dependent upon the second power supply voltage, and a third terminal, the third multiplexer receiving a third control signal, the third multiplexer coupling the third terminal to one of at least its first terminal or its second terminal based upon the third control signal; and
- 20

a second level shifter having a first signal terminal coupled the third terminal of the second multiplexer and a voltage supply terminal coupled to the third terminal of the second multiplexer.

8. A wireless device including the integrated circuit die of claim 4.

5 9. A method of multiplexing digital signal lines comprising:

selecting one of at least a first digital signal line and a second digital signal line to couple to a signal terminal of a level shifter for conveying a digital signal between the level shifter and the one of the at least first digital signal line and the second digital signal line;

10 powering a first circuit coupled to the first digital signal line at a first power supply voltage, wherein when the first digital signal line is at a first state, the first digital signal line is at a voltage dependent upon the first power supply voltage;

15 powering a second circuit coupled to the second digital signal line at a second power supply voltage, wherein when the second digital signal line is at a first state, the second digital signal line is at a voltage dependent upon the second power supply voltage; and

20 selecting one of at least a first voltage and a second voltage to supply to a supply voltage terminal of the level shifter, wherein the first voltage is dependent upon the first power supply voltage and the second voltage is dependent upon the second power supply voltage, wherein the first voltage is selected when the first digital signal line is selected to be coupled to the signal terminal and the second voltage is selected when the second digital signal line is selected to be coupled to a signal terminal.

25

10. The method of claim 9 wherein the selecting one of at least a first digital signal line and a second digital signal line and the selecting one of at least a first voltage and a second voltage further include writing to a control register a control value indicative of one of at least the first digital signal line and the
5 second digital signal line.

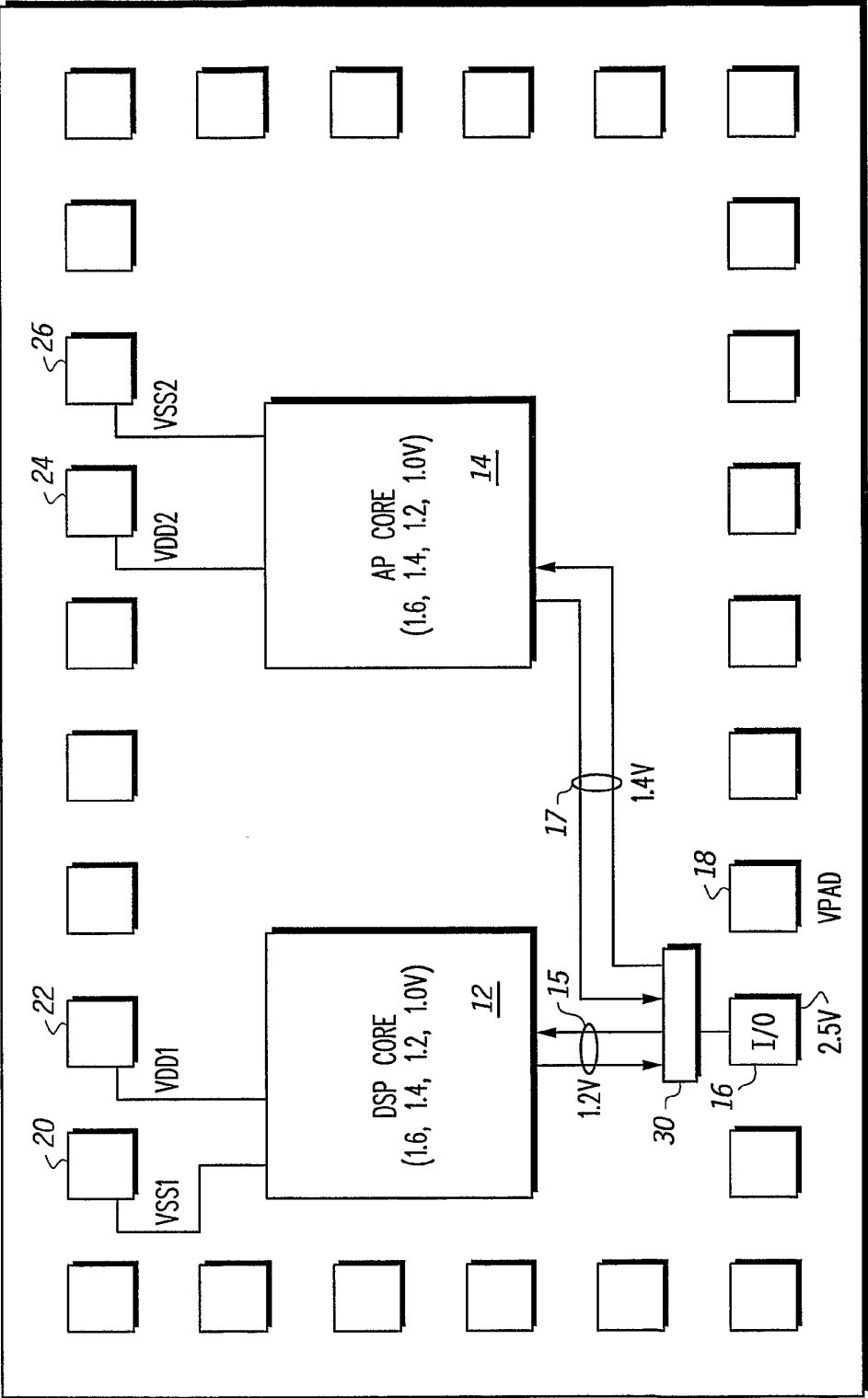


FIG. 1

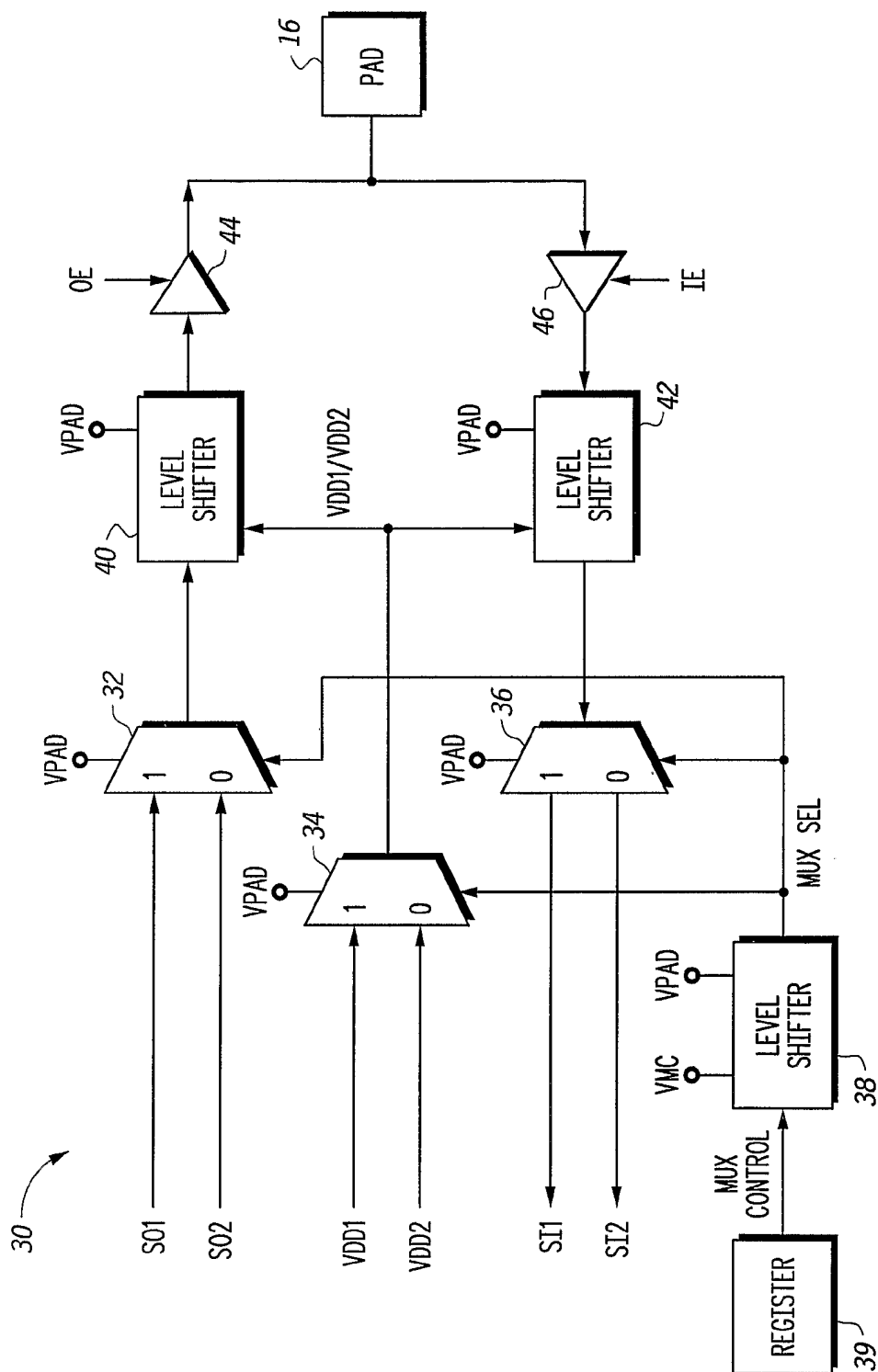


FIG. 2

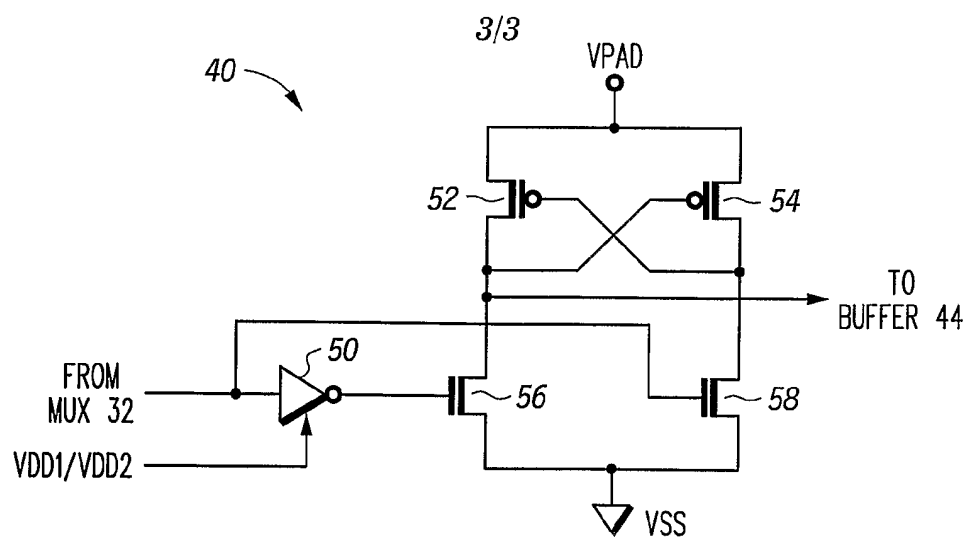


FIG. 3

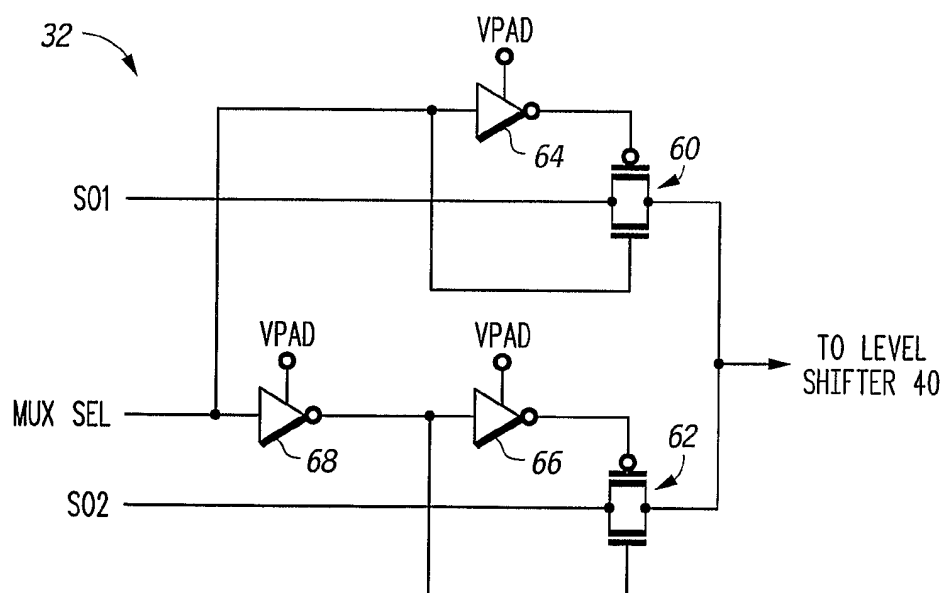


FIG. 4

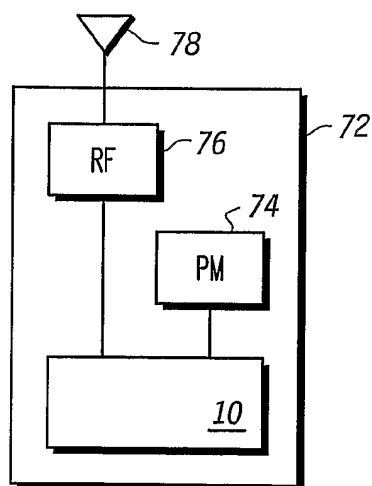


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US04/27499

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H03K 19/082, 19/094

US CL : 326/105,113,63,68,81,108; 327/333

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 326/105,113,63,68,81,108; 327/333

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST BRS: ap core, dsp core, multiple voltage supplies, multiplexer(s)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,973,955 A (NOGLE et al.) 26 October 1999, see entire document.	1-10
A	US 6,346,829 B1 (CODDINGTON) 12 February 2002, see entire document.	1-10
A	US 6,535,018 B1 (KOST) 18 March 2003, see entire document.	1-10
A	US 5,534,798 A (PHILLIPS et al.) 09 July 1996, see entire document.	1-10

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T"

later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X"

document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y"

document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"

document member of the same patent family

Date of the actual completion of the international search

05 November 2004 (05.11.2004)

Date of mailing of the international search report

15 FEB 2005

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Facsimile No. (703) 305-3230

Authorized officer

Vibol Tan

Telephone No. (703) 308-0659