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(71) Applicant *(for all designated States except US)*: **HONG KONG APPLIED SCIENCE & TECHNOLOGY RESEARCH INSTITUTE CO., LTD** [CN/CN]; 3rd Floor, Bio-Informatics Centre, 2 Science Park West Avenue, Hong Kong Science Park, Hong Kong (CN).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **MA, Wei** [CN/CN]; Flat E, 21/F, Tower 4, The Metropolis, T.K.O., NT, Hong Kong (CN). **SHI, Xunqing** [SG/CN]; Flat A, Floor 10, Block 4 Dawning Views, Fanling, N.T., Hong Kong (CN). **CHUNG, Chang Hwa** [US/CN]; 5/F, Photonics Centre, 2 Science Park, East Avenue, Hong Kong Science Park, Shatin, New Territories, Hong Kong (CN).

(74) Agent: **SHENZHEN TRUER IP**; Suite 2201, Block B, Jia Zhao Ye Centre, Shangbu Road, Futian district, Shenzhen, Guangdong, Guangdong 518031 (CN).

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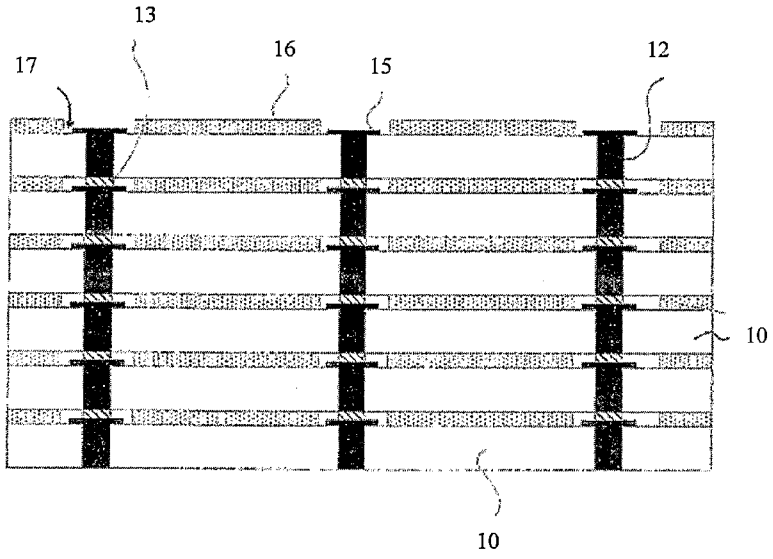
(54) **Title**: BONGDING METHOD FOR THROUGH-SILICON-VIA BASED 3D WAFER STACKING

Figure 2



(57) **Abstract**: There is described a hybrid bonding method for through-silicon-via based wafer stacking. Patterned adhesive layers are provided to join together adjacent wafers in the stack, while solder bondng is used to electrically connect the vias. The adhesive layers are patterned to enable outgassing and to provide stress relief.

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BONDING METHOD FOR THROUGH-SILICON-VIA BASED 3D WAFER STACKING

FIELD OF THE INVENTION

This invention relates to a bonding method for through-silicon-via based 3D wafer stacking, in particular the invention relates to a hybrid bonding method employing aspects of both adhesive and solder bonding. The invention also extends to the resulting wafer stack assembly.

BACKGROUND OF THE INVENTION

With electronic devices, particularly portable devices such as mobile phones, becoming smaller and yet at the same time offering a wider range of functions, there is a need to integrate multifunctional chips but without increasing the size of the devices and keeping a small form factor. Increasing the number of electronic components in a 2D structure is incompatible with these objectives, and therefore 3D packages are increasingly being adopted in order to provide greater functionality and higher component density but with a small form factor.

In a 3D structure electronic components such as semiconductor chips with different active IC devices may be provided in a multilayer stacked structure. Traditionally wire bonding (e.g., US6,933,172) is used to establish electrical interconnects between chips, but wire bonding requires greater in-plane size and out-of-plane size and is inconsistent with the objective of maximizing the component density. To connect electrically the components in different layers through-silicon-via (TSV) technology may be used to provide the electrical interconnect and to provide mechanical support. In TSV technology a via is fabricated in a silicon chip with different active IC devices or other

devices fabricated by a semiconductor process and the via is filled with metal such as Cu, Au, W, solders, or a highly-doped semiconductor material such as polysilicon. Multiple components provided with such vias are then stacked and bonded together.

PRIOR ART

The bonding method is an important aspect of the fabrication of stacked electronic components. An ideal bonding method should be reliable and cost-effective. As an alternative to wire bonding interconnection, the use of TSV interconnects has been proposed and methods including diffusion bonding, soldering, and adhesive bonding can be used to bond wafers/chips with TSV interconnects.

In diffusion bonding a thin metal bonding layer (formed for example preferably from copper but also possibly tin, indium, gold, nickel, silver, palladium, palladium-nickel alloy or titanium) is applied to the respective surface of semiconductor components that are to be bonded. When the components are brought together under the correct conditions of temperature and pressure the two metal bonding layers diffuse into each other to form an intermetallic compound (IMC) and create the bond. Diffusion bonding produces a good quality bond that is reliable, but disadvantages of this method include the requirements for very good coplanarity of the two semiconductor components and the need for a high bonding temperature. The method is therefore difficult to implement and is expensive. A typical example of a diffusion bonding method is shown in US 7,157,787.

Adhesive bonding is a low cost option in which an adhesive layer is provided on the surfaces to be bonded together. An example of adhesive bonding is shown in US

6,593,645. US 6,448,661 shows an example of the prior art in which chips are bonded using conductive adhesives such as anisotropic conductive film (ACF) or anisotropic conductive adhesive (ACA). Another example of adhesive bonding is shown in US 4,897,708 where wafers are bonded by adhesive and electrical connections are made by a conductive liquid. However, while adhesive bonding is low cost and does not present significant manufacturing problems, it provides inferior electrical connections at the vias and is not generally suitable for high current use and is unreliable.

An example of a soldering method is shown in US 6,577,013. In a soldering method solder is applied at the junctions of vias on semiconductor components to be stacked. Soldering does not require such high temperatures as diffusion bonding and can still produce a good reliable bond. However, soldering encounters problems as the number of components being stacked increases. An example of solder bonding can be found in US 7,317,256 which describes the bonding of multiple stacked wafers, another example is US 7,215,033. In such methods, however, when a new wafer is added to a stack and a soldering process is carried out to form an IMC connecting the new wafer to the stack, the previously formed IMCs between other wafers grow very fast under the high soldering temperature. Since the IMC is usually a hard and brittle material so as it grows failure issues will occur (e.g., in the drop qualification test). Furthermore, if the volume of the solder materials is not controlled well in the manufacturing process, in multiple solder bonding steps the remained solders, which are not formed IMCs, will be reflowed again, this will undermine their reliability and generate manufacturing defects, leading to potential failures in severe conditions.

SUMMARY OF THE INVENTION

According to the invention there is provided a method of forming a wafer stack comprising the steps of, forming a plurality of wafers into a stack, each said wafer being provided with at least one through-silicon-via and with solder material being provided between through-silicon-vias formed in adjacent wafers, said wafers being bonded together by means of adhesive layers provided between adjacent wafers, and subjecting said stack to a single reflow process whereby said through-silicon-vias are electrically interconnected by said solder material.

Preferably the adhesive layers are patterned to define channels that extend from at least some of said through-silicon-vias to an edge of the stack. For example the adhesive layer may comprise a photosensitive adhesive that is patterned by exposure to light.

In preferred embodiments of the invention the adhesive layer is patterned to define a space surrounding each through-silicon-via formed in a wafer. The space may be annular or any other suitable shape. In many cases at least two through-silicon-vias will be formed in a wafer and the spaces surrounding said through-silicon-vias are interconnected by channels. For example a wafer may be provided with a regular array of through-silicon-vias and the space surrounding each said through-silicon-via is connected by channels to the spaces surrounding all adjacent through-silicon-vias.

In a particularly preferred embodiment, the adhesive layers are patterned to divide a wafer into a plurality of chips and wherein the chips in a wafer are divided by main channels formed by patterning of the adhesive layer and extending to at least one edge of

the wafer, and each chip may include at least one through-silicon-via provided with a channel extending from the space surrounding the through-silicon-via to a main channel.

Preferably the stack is subject to loading compression during said soldering process.

According to another aspect of the invention there is provided a wafer stack comprising a plurality of wafers arranged in a stack, each wafer including at least one through-silicon-via, wherein adjacent wafers are bonded together by means of an intervening adhesive layer, and wherein electrical connections between the wafers are formed by solder material provided between the through-silicon-vias formed in adjacent layers.

Preferably the adhesive layers are patterned to define channels that extend from at least some of said through-silicon-vias to an edge of the stack assembly. In particular the adhesive layers may be patterned to define a space surrounding each through-silicon-via formed in a wafer. This space may be annular or any other suitable shape.

In preferred embodiments at least two through-silicon-vias are formed in a wafer and the spaces surrounding said through-silicon-vias are interconnected by channels. For example a wafer may be provided with a regular array of through-silicon-vias wherein the space surrounding each said through-silicon-via is connected by channels to the spaces surrounding all adjacent through-silicon-vias.

In a particularly preferred embodiment said adhesive layers are patterned to divide each wafer into a plurality of chips and wherein said chips in a wafer are divided by main channels formed in a said adhesive layer and extending to at least one edge of the wafer,

and wherein each said chip includes at least one through-silicon-via provided with a channel extending from the space surrounding said through-silicon-via to a said main channel.

BRIEF DESCRIPTION OF THE DRAWINGS

Some embodiments of the invention will now be described by way of example and with reference to the accompanying figures, in which;-

Fig.1 is a top view of a wafer stack according to an embodiment of the invention,

Fig.2 is a cross-sectional view along line A-A in Fig.1,

Fig.3 is a cross-sectional view of a wafer illustrating the adhesive patterning, and

Figs.4 to 12 show a manufacturing process for creating a stacked wafer assembly as shown in Figs.1 and 2.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Fig.1 shows an embodiment of the invention in the form of a circular wafer stack 100 which may be divided into four chips 110-113. Fig.2 is a cross-sectional view along line A-A showing the structure of the wafer stack with a plurality of TSVs electrically connected by solder and with individual wafers bonded together by layers of adhesive that are patterned in a manner to be described below.

In this example each chip 110-113 has a different arrangement of vias 120 (e.g., a simple square in 110, two rows of three vias in 111 and 112, and a square with a central via in chip 113), but in each case every via is formed with a surrounding space that connects to an edge of the chip through channels either directly or through another surrounding space. It will be seen that the four chips are divided by mutually perpendicular main rows 114-

119 that are channels formed by patterning the adhesive and which lead to the edge of the wafer. Each channel in one of the chips 110-113 ultimately connects to one of the main rows 114-119 and thus to the edge of the wafer. It will also be understood that the main rows 114-119 result from a patterning of the adhesive layer such that the layer does not extend as a uniform layer over the entire wafer but is broken into islands of adhesive corresponding to the four chips and the surrounding parts of the wafer. By dividing the adhesive layer in this way stress may be relieved in the manufacturing process.

Fig. 2 shows the structure of the stacked wafers in more detail. In this example the wafer stack comprises six wafers 10 electrically interconnected by means of through-silicon-vias (TSVs) 12. The TSVs are electrically connected to each other by means of solder 13 located between the lower end of a TSV 12 and a metal pad 15 provided on the upper surface of a wafer 10 and covering the upper end of a TSV 12. The wafers 10 are physically bonded together by layers of adhesive 16.

Fig.3, for clarity of understanding, shows a very simple example in which the TSVs 12 are arranged in a simple 2 x 3 array. As can be seen from Fig.3 the adhesive 16 is patterned so as to leave an annular space 17 around each metal pad. Furthermore the adhesive 16 is also patterned so as to define interconnecting channels 18 that extend between each an annular space 17 such that each annular space 17 is connected to all adjacent annular spaces 17 by means of such interconnecting channels the purpose of which will be described later. It will also be noted that in addition to providing connections between the annular spaces 17, there is also an interconnecting channel 18 that leads from each annular space 17 to the edge 19 of the stack.

It should be noted, however, that Fig.3 only shows a simple embodiment of the invention in which the TSVs are arranged in a simple regular 2 x 3 array in which each TSV has at least one interconnecting channel 18 that leads to an edge 19 (and in the case of the four corner TSVs there are two interconnecting channels 18 leading to two edges 19). In more complicated or larger structures there may be TSVs that are surrounded on all sides by other TSVs and may not connect directly to an edge but only to such other surrounding TSVs. Furthermore, while the example of Fig.3 is a simple regular array in which the interconnecting channels are at right angles to each other and each annular space 17 connects to four interconnecting channels 18, in more complex patterns different numbers of channels 18 may be provided. Preferably, each TSV is provided with interconnecting channels 18 that connect a given TSV to all its immediately adjacent neighbours and – in the case of a TSV provided at an edge of the wafer – to the edge. Even this may not be essential, however. What is important is that a network of interconnecting channels are provided such that for every TSV, whether at an edge of the wafer or not, there exists a continuous path from the annular space 17 surrounding a TSV to an edge of the wafer 19, whether directly or via other annular spaces 17. It will also be understood that while in the embodiment shown in Figs.1-3 the spaces 17 surrounding each TSV 12 by the adhesive patterning are circular this is not essential and the spaces could take other possible shapes. It will be understood however that if no further wafers 10 are to be added to the stack no further adhesive layer 16 would be provided to the upper surface.

The following description will explain how such a structure may be manufactured.

The starting point is a wafer 10 formed of a suitable material such as silicon (Fig.4). A layer of photoresist 11 is then applied to the upper surface of the wafer 10 and patterned before a deep reactive-ion etching process is used to create vias 12. After the isolation layer (e.g., SiO2), adhesion layer (e.g., Ti/W) and seed layer (e.g., Cu) are prepared for the vias 12, they are then filled with metal, usually Cu or W or other suitable material by solder plating, and then a thin layer of solder is plated sequentially after finishing the filling metal plating (Fig.5). It should be noted that at this stage the vias 12 do not extend through the complete depth of the wafer 10. The layer of photoresist 11 is then removed (Fig.6) and the wafer 10 is then mounted on a wafer holder 14 through a layer of glue 20 (Fig.7), and the wafer 10 is then subject to a thinning process (eg mechanical grinding, chemical-mechanical-polishing or chemical or plasma etching) until the inductive metal of the vias 12 extends all the way through the wafer 10 (Fig.8).

The wafer 10 – still attached to the holder 14 – is then inverted and metal pads 15 are then formed on the exposed ends of the vias 12 (Fig.9) with a layer of insulator between the pad 15 and the wafer 10. An adhesive layer 16 is then applied to the exposed surface of the wafer 10 and is patterned as shown and described above with reference to Figs.1 to 3 such that an annular space 17 is defined around each metal pad 15. The patterning of the adhesive layer 16 will also include interconnecting channels 18 as shown in Figs.1 to 3 that interconnects the annular spaces 17 surrounding the metal pads 15 and which defines conduits connecting the annular spaces 17 to the edges of the wafer 10. The adhesive layer 16 is preferably a photosensitive polymer adhesive (e.g., SU-8) that can be patterned by exposure to light. It will of course be understand that the spaces 17 need not be annular and could be other shapes.

As shown in Fig.11, the wafer holder 14 is then inverted and the wafer 10 is secured to a stiff substrate 18 through a layer of glue 19 with the patterned adhesive 16 contacting the glue layer 19. The wafer holder 14 is then removed and used again for the fabrication of the second wafer. Once the second wafer has been formed it is then secured to the first wafer 10 with the patterned adhesive layer 16 of the second wafer contacting the top surface of the first wafer. Once more the wafer holder 14 is removed and the process is repeated as often as required until the wafer stack is completed as shown in Fig.12.

Following completion of the wafer stack assembly, the assembly is then subject to a single soldering process such that all solder portions are bonded to the respective metal pads. At the same time the soldering process also serves to act as a post-cure of the adhesive layers. Optionally the wafer stack assembly may be under loading compression during the soldering/post-cure process to enhance the bonding of the wafers by means of the adhesive layers. The use of a single soldering process avoids the problems caused by multiple reflow steps in the prior art.

It will be understood that the process described above is a hybrid solder bonding/adhesive bonding process. Solder bonding is used to provide good electrical connections between vias that can operate at high currents and with good reliability. The adhesive layer provides mechanical support for the layers while the stack is being assembled and easier wafer handling, and in the final wafer stack provides additional bonding strength. By patterning the adhesive layer channels are provided that enable gases released during out-gassing to escape, and by dividing the adhesive layer into different regions stress can be relieved, while the symmetric sandwich structure (adhesive-silicon-adhesive) can balance the potential warpage caused by CTE mismatch.

Following the solder bonding process the wafer stack will be subject to a conventional singularity process and then underfill will be injected into the patterned adhesive layers and the wafer stack will be subject to a conventional molding process.

CLAIMS

1. A method of forming a wafer stack comprising the steps of: forming a plurality of wafers into a stack, each said wafer being provided with at least one through-silicon-via and with solder material being provided between through-silicon-vias formed in adjacent wafers, said wafers being bonded together by means of adhesive layers provided between adjacent wafers, and subjecting said stack to a single soldering process whereby said through-silicon-vias are electrically interconnected by said solder material.

2. A method as claimed in claim 1 wherein said adhesive layers are patterned to define channels that extend from at least some of said through-silicon-vias to an edge of the stack.

3. A method as claimed in claim 2 wherein said adhesive is a photosensitive adhesive and is patterned by exposure to light.

4. A method as claimed in claim 2 wherein said adhesive layer is patterned to define a space surrounding each through-silicon-via formed in a wafer.

5. A method as claimed in claim 4 wherein said space is annular or any other suitable shape.

6. A method as claimed in claim 4 wherein at least two through-silicon-vias are formed in a wafer and the spaces surrounding said through-silicon-vias are interconnected by channels.

7. A method as claimed in claim 4 wherein a said wafer is provided with a regular array of through-silicon-vias and wherein the space surrounding each said through-silicon-via is connected by channels to the spaces surrounding all adjacent through-silicon-vias.

8. A method as claimed in claim 4 wherein said adhesive layers are patterned to divide a wafer into a plurality of chips and wherein said chips in a wafer are divided by main channels formed in said adhesive layer and extending to at least one edge of the wafer, and wherein each said chip includes at least one through-silicon-via provided with a channel extending from the space surrounding said through-silicon-via to a said main channel.

9. A method as claimed in claim 1 wherein said stack is subject to compression loading during said soldering process.

10. A method as claimed in claim 1 wherein after the single soldering process the wafer is divided into individual chips which are then subject to an underfill and molding process.

11. A wafer stack comprising a plurality of wafers arranged in a stack, each said wafer including at least one through-silicon-via, wherein adjacent wafers are bonded together by means of an intervening adhesive layer, and wherein electrical connections between said wafers are formed by solder material provided between the through-silicon-vias formed in adjacent layers.

12. A wafer stack assembly as claimed in claim 11 wherein said adhesive layer is patterned to define channels that extend from at least some of said through-silicon-vias to an edge of the stack assembly.

13. A wafer stack assembly as claimed in claim 12 wherein said adhesive layer is patterned to define a space surrounding each through-silicon-via formed in a wafer.

14. A wafer stack assembly as claimed in claim 13 wherein said space is annular or any other suitable shape.

15. A wafer stack assembly as claimed in claim 14 wherein at least two through-silicon-vias are formed in a wafer and the spaces surrounding said through-silicon-vias are interconnected by channels.

16. A wafer stack assembly as claimed in claim 15 wherein a said wafer is provided with a regular array of through-silicon-vias and wherein the space surrounding each said through-silicon-via is connected by channels to the spaces surrounding all adjacent through-silicon-vias.

17. A wafer stack assembly as claimed in claim 11 wherein said adhesive layers are patterned to divide each wafer into a plurality of chips and wherein said chips in a wafer are divided by main channels formed in a said adhesive layer and extending to at least one edge of the wafer, and wherein each said chip

includes at least one through-silicon-via provided with a channel extending from the space surrounding said through-silicon-via to a said main channel.

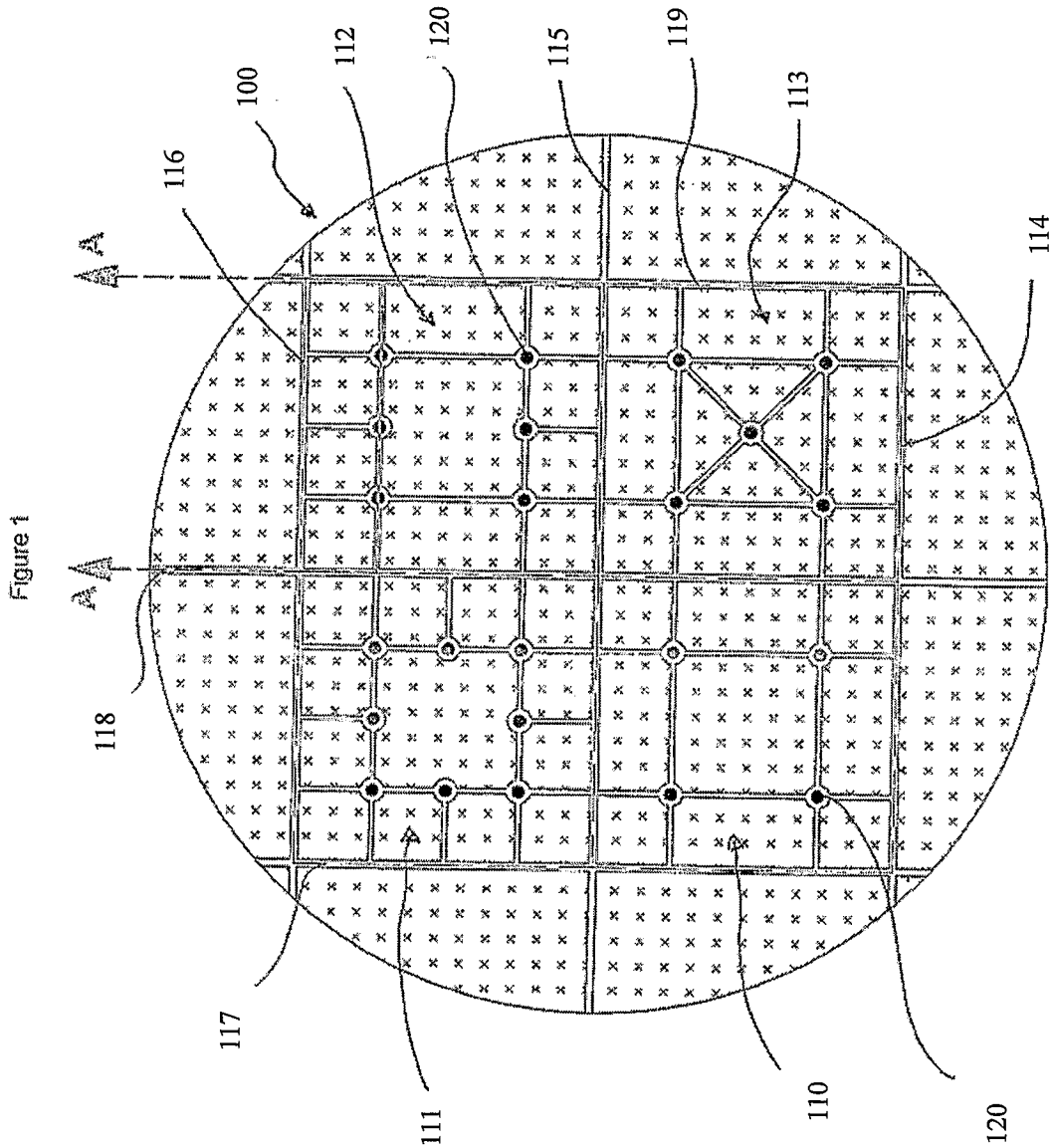


Figure 1

Figure 2

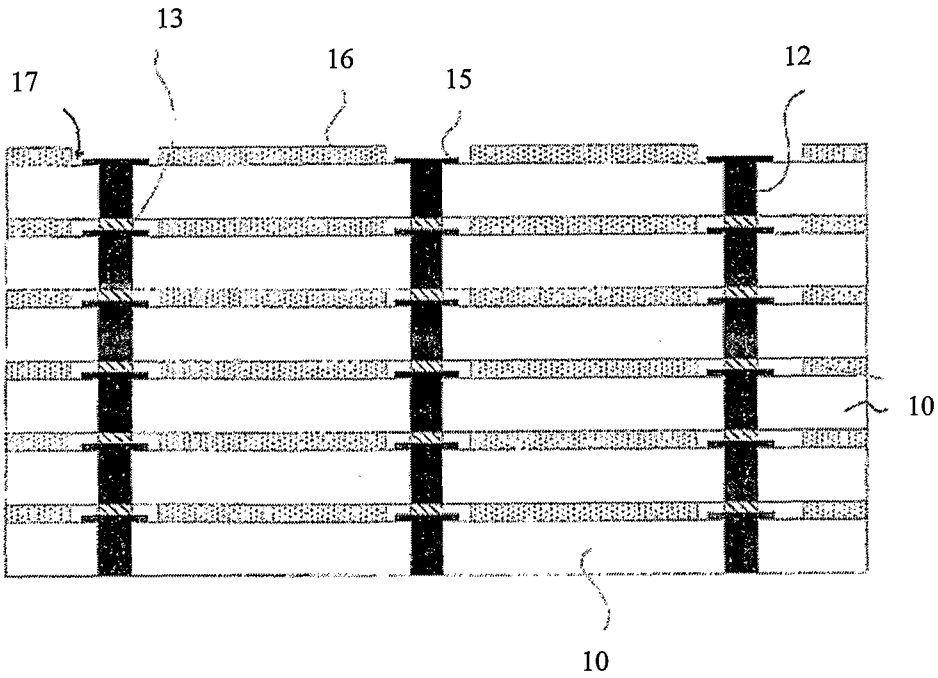


Figure 3

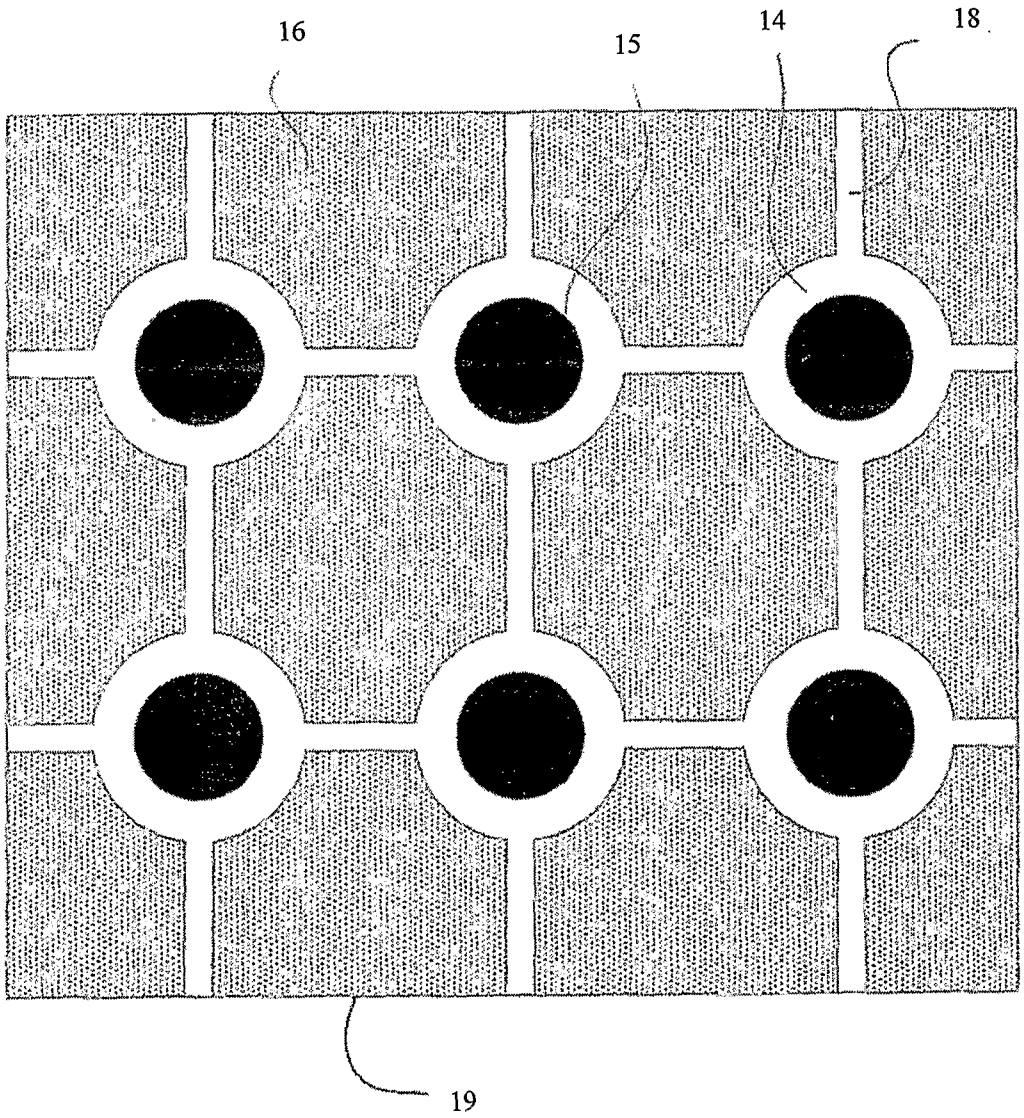


Figure 4

Figure 5

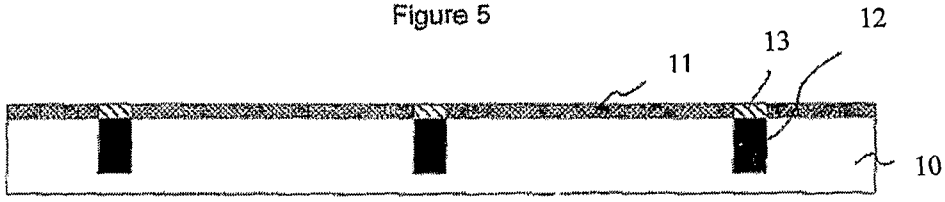


Figure 6

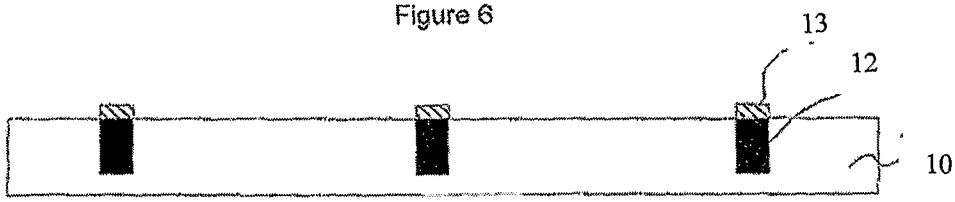


Figure 7

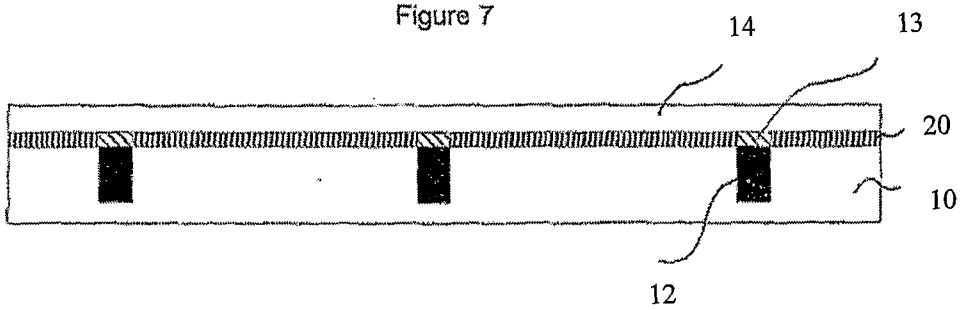


Figure 8

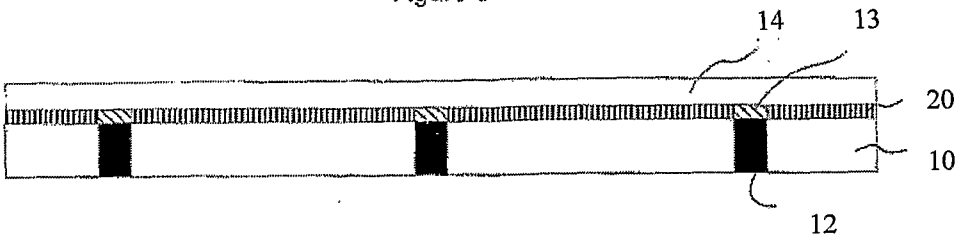


Figure 9

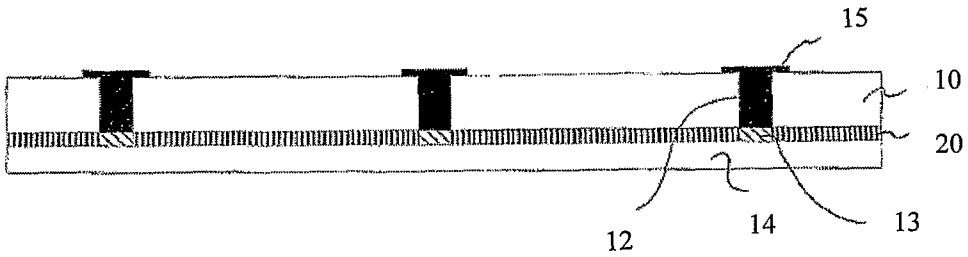


Figure 10

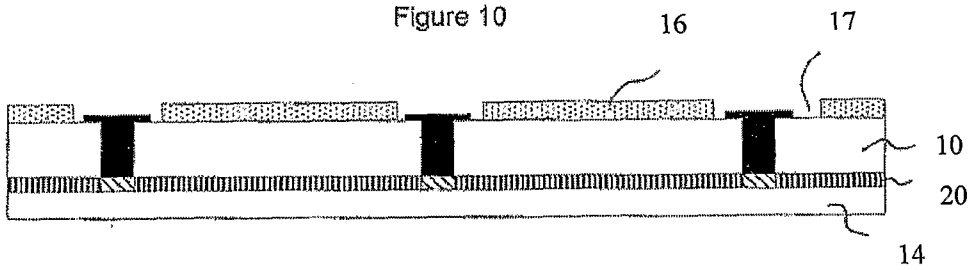


Figure 11

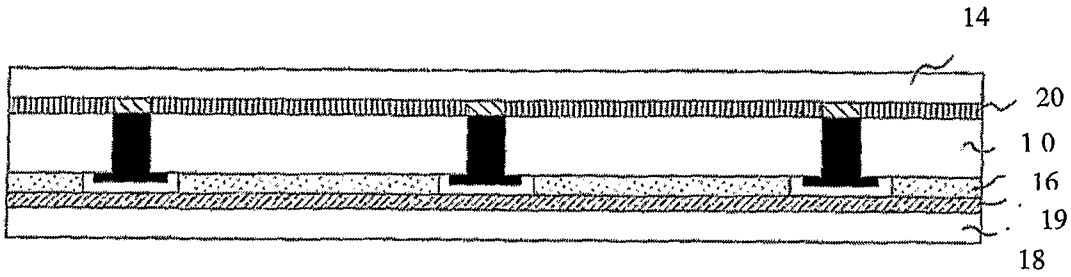
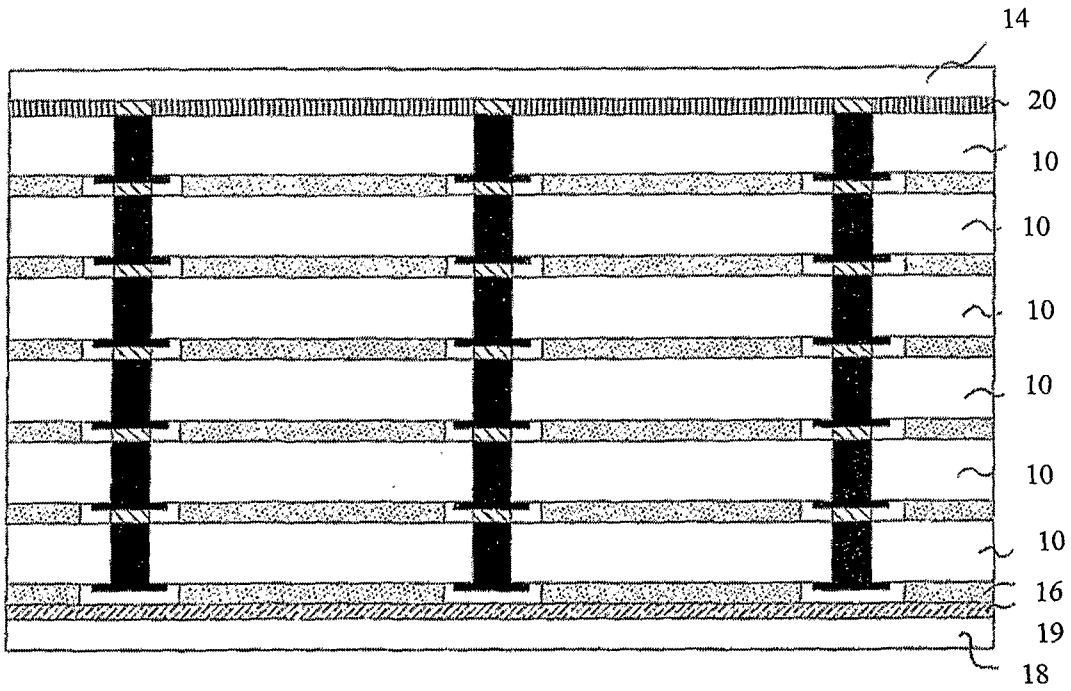


Figure 12



INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2008/071193

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L 23/02, H01L 23/48, H01L 23/488, H01L 23/52, H01L 25/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC,WPI, PAJ, CNPAT, CNKI: wafer, chip, die, device, stack, assembly, array, via, hole, through silicon via, bond???, solder???, adhesive, adhere, stick, pattern??, outgas???, stress, single solder???, reflow, once

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 7317256B2 (Williams et al.) 08 Jan. 2008 (08.01.2008), line 1-line 67 of column 5, Figs1,4-6	1,9,10,11
Y	US 4897708 A (Clements) 30 Jan. 1990 (30.01.1990), line36-line40 of column 4, Figs 1-8	1,9,10,11
Y	US 2006/0049501 A1(Lee et al.) 09 Mar. 2006 (09.03.2006), paragraph 59 of page 4, Fig. 3H	1,9,10
A	US 6593645 B2 (Shih et al.) 15 Jul. 2003 (15.07.2003), the whole document	1-17
A	US 6448661 B1 (Kim et al.) 10 Sep. 2002 (10.09.2002), the whole document	1-17
A	US 2008/0079121 A1 (Han) 03 Apr. 2008 (03.04.2008), the whole document	1-17
A	CN 101038908 A(HYNIX SEMICONDUCTOR INC) 19 Sep. 2007 (19.09.2007), the whole document	1-17

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5. Nov. 2008(05.11.2008)	**20 Nov. 2008 (20.11.2008)**
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CLASSIFICATION OF SUBJECT MATTER

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