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(71) Applicant: **CARL ZEISS AG** [DE/DE]; Carl-Zeiss-Strasse 22, 73447 Oberkochen (DE).

(72) Inventor; and
(71) Applicant: **MCGARVEY, James, E.** [US/US]; 139 Clarkson Hamlin Town Line Rd, Hamlin, NY 14464 (US).

(72) Inventor: **VALERA, Harshesh**; #111-15152 62A Ave, Syrrey, BC, V3S 8A6 (CA).

(74) Agent: **EWERS, Falk**; Ewers & Hasselmann PLLC, 1101 Connecticut Ave., NW, Suite 450, Washington, DC 20036 (US).

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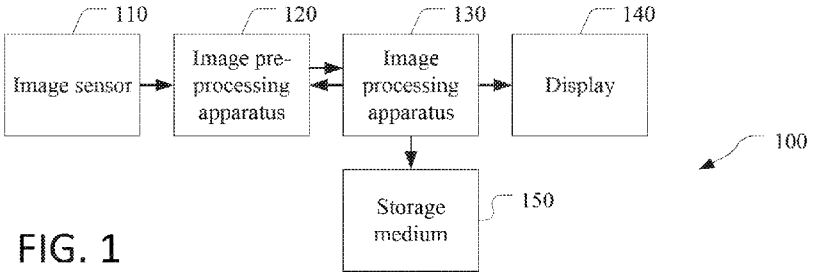


FIG. 1

(57) Abstract: A method, an image pre-processing apparatus, and a camera system for processing large images are provided. The method includes receiving from an image sensor an image frame at an image pre-processing apparatus, the image frame having a frame pixel resolution substantially equal to a sensor pixel resolution of the image sensor, dividing the image frame into first and second image subframes to be sequentially processed by an image signal processor, each of the first and the second image subframes having a subframe pixel resolution smaller than the sensor pixel resolution and a region in which the first and second image subframes overlap with each other. The subframe pixel resolution is predetermined by a processing capacity of the image signal processor, and the first and the second image subframes are consecutively processed by the image signal processor.

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METHOD, APPARATUS, AND SYSTEM FOR PROCESSING DIGITAL IMAGES

CROSS-REFERENCE TO RELATED PATENT APPLICATION

[0001] This application claims priority to U.S. Patent Application No. 16/006,637 filed on June 12, 2018, the disclosure of which is incorporated herein in its entirety by reference.

TECHNICAL FIELD

[0002] The invention relates to processing of digital images, and, in particular, to processing large digital images with a high pixel resolution in a still image mode. Further, the invention relates to an apparatus and a system performing processing of digital images.

BACKGROUND

[0003] Digital cameras include image sensors to capture digital images and are generally operated in still image mode or live view mode. Different techniques may be used to produce still images and live view images. While it is important to produce still images with a high quality, images for live view or preview may be generated with less but still acceptable image quality.

[0004] Image sensors typically detect a light intensity per pixel. To allow color information

to be recorded, color filters may be bonded to the substrate of the image sensor which allocate a certain color to a certain pixel, and each pixel detects the light intensity for the specific color. A typical pattern for a color filter used in digital cameras is a Bayer filter. A Bayer filter contains alternating rows of red and green filters and blue and green filters, wherein each row contains alternating red and green filters and blue and green filters, respectively. Green filters preferentially allow green light photons to pass to the detector (e.g., a photodiode) of the respective pixel of the image sensor. At the same time, red and blue light photons that arrive at the green filter are not transmitted by the filter and, therefore, not detected by the respective detector. Similarly, red filters preferentially allow red light photons and blue filters allow only blue light photons to pass to the respective detector.

[0005] Each image frame has an image pixel resolution that depends on a pixel resolution of the image sensor and generally describes the detail of information that a digital image contains. In other words, by increasing the image pixel resolution, the level of detail in the image can be increased. The pixel resolution of an image frame is typically described by a number of pixel columns (image width) and a number of pixel rows (image height) which result in a number of total pixels that need to be processed by the specialized image processor.

[0006] When a Bayer filter is applied in front of an image sensor, the resulting image frame produced by the image sensor needs to be interpolated or demosaiced to generate all three colors for each pixel so that the digital image can be displayed, printed or stored.

[0007] In digital cameras, interpolating or demosaicing may be performed by specialized

image signal processors (ISPs) but also by general purpose processors (CPUs) which execute image processing software programs.

[0008] The process of interpolating or demosaicing can be very complex depending on the effectiveness of the mathematical algorithms used in particular because of the much higher number of pixels that need to be processed in still image mode. United States Patent No. 6,292,218 B1 describes an electronic camera in which the more complex digital techniques for generating a high quality still image are implemented in software and executed on a CPU, whereas the less complex techniques for producing preview images of acceptable quality are implemented in an application specific integrated circuit (ASIC).

[0009] However, utilizing a CPU for still image processing may significantly increase the cost of manufacturing high resolution digital cameras. In particular, still image processing is significantly slower than still image processing with ISP's because all the steps have to be performed sequentially on the CPU, whereas they are performed concurrently in a pipeline in the ISP. On the other hand, processing still images with ISPs that have correspondingly high processing capabilities may also result in significantly higher manufacturing costs for the digital camera. Therefore, new approaches are needed which allow the use of ISPs with relatively low processing capabilities to also process full resolution high quality still image frames without the need of a CPU for image processing, such as interpolating and demosaicing.

SUMMARY

[0010] It is therefore an object of the invention to provide a method, an image processing apparatus, and a system for processing large digital images with a high pixel resolution in a still image mode by an image signal processor with a limited processing capacity.

[0011] According to a first aspect of the invention, a method for processing digital images is provided in which an image frame is received from an image sensor at an image pre-processing apparatus. The image frame has a frame pixel resolution substantially equal to a sensor pixel resolution of the image sensor. A frame pixel resolution that is substantially equal to the sensor pixel resolution in this disclosure may include frame pixel resolutions that are equal to the sensor pixel resolution and frame pixel resolutions that slightly deviate from the sensor pixel resolution. In particular, substantially equal means that the frame pixel resolution can be slightly smaller than the sensor pixel resolution because some image frame rows and/or image frame columns are omitted from the full sensor pixel resolution. The image frame is divided into at least two image subframes to be sequentially processed by an image signal processor. Thereafter, the at least two image subframes are consecutively processed by the image signal processor.

[0012] According to a second aspect of the invention, an image pre-processing apparatus is provided which includes an image data receiver configured to receive an image frame from an image sensor, the image frame having a frame pixel resolution substantially equal to a sensor pixel resolution of the image sensor. The image pre-processing apparatus further includes a data interface, an imager data interface, and a direct memory access (DMA) controller in

communication with the image data receiver, the data interface, and the imager data interface. The DMA controller is configured to store the image frame to a buffer memory via the data interface, to receive first and second image subframes being generated from the image frame by dividing the image frame into the first and second image subframes to be processed by an image signal processor, and to consecutively transmit the first and second subframes to the image signal processor via the imager data interface.

[0013] Each of the first and the second image subframes have a subframe pixel area that is smaller than the sensor pixel resolution and a region in which the first and second image subframes overlap with each other. The subframe pixel resolution is predetermined by a processing capacity of the image signal processor.

[0014] According to a third aspect of the invention, a camera system for processing digital images is provided. The camera system includes an image sensor, an image pre-processing apparatus in communication with the image sensor, an image processing apparatus in communication with the pre-processing apparatus and including a buffer memory and an image signal processor; and a display connected to the image processing apparatus. The image pre-processing apparatus includes an image data receiver configured to receive an image frame from the image sensor, the image frame having a frame pixel resolution substantially equal to a sensor pixel resolution of the image sensor, a data interface and an imager data interface, and a direct memory access (DMA) controller in communication with the image data receiver, the data interface, and the imager data interface. The DMA controller is configured to store the image frame to the buffer memory via the data interface, to receive first and second subframes being generated from the image frame, and to

consecutively transmit the first and second subframes to the image signal processor via the imager data interface.

[0015] As a result, the use of an image pre-processing apparatus according to an aspect of the invention allows the use of pre-manufactured image processing apparatuses that have ISPs thereon with processing capabilities that would, without the operations performed by the image pre-processing apparatus, only be capable of processing downsized preview image frames, but not high resolution still image frames.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The invention will now be described with reference to the drawings, wherein:

[0017] FIG. 1 shows a schematic illustration of a camera system for processing digital images according to an exemplary embodiment of the invention;

[0018] FIG. 2 shows a schematic illustration of an image pre-processing apparatus according to an exemplary embodiment of the invention;

[0019] FIG. 3 shows another detailed schematic illustration of the camera system for processing digital images according to an exemplary embodiment of the invention;

[0020] FIG. 4A shows an illustration of an image frame generated by an image sensor;

[0021] FIG. 4B shows an illustration of a first image subframe generated from the image frame of FIG. 4A;

[0022] FIG. 4C shows an illustration of a second image subframe generated from the image frame of FIG. 4A;

[0023] FIG. 5 is a flow chart depicting operations performed by the camera system to process an image frame according to an exemplary embodiment of the invention;

[0024] FIG. 6 is a flow chart depicting operations performed by the camera system to generate a still image frame according to an exemplary embodiment of the invention;

[0025] FIG. 7 shows a schematic illustration of an image pre-processing apparatus according to a second exemplary embodiment of the invention;

[0026] FIG. 8 shows a schematic illustration of a camera system for processing digital images according to a third exemplary embodiment of the invention;

[0027] FIG. 9 shows a detailed schematic illustration of the camera system for processing digital images according to the second exemplary embodiment of the invention;

[0028] FIG. 10 shows a detailed schematic illustration of the camera system for processing digital images according to the third exemplary embodiment of the invention; and

[0029] FIG. 11 shows a detailed schematic illustration of the camera system for processing digital images according to a fourth exemplary embodiment of the invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0030] FIG. 1 shows a camera system 100 for processing digital images according to an exemplary embodiment of the invention. The camera system 100 includes an image sensor 110, an image pre-processing apparatus 120, and an image processing apparatus 130 to which a display 140 and a storage medium 150 are connected.

[0031] The image sensor 110 can be operated in a live view mode and in a still capture mode. In both modes, the full active area of the image sensor 110 is utilized, and an image frame is generated and outputted by the image sensor 110 to the image pre-processing apparatus 120. As described in more detail below, for previewing live view or still capture preview, the image frame is downsized by the image pre-processing apparatus 120 to enable a high frame rate. For still image capture, however, all lines and columns of the image frame are processed without downsizing.

[0032] Live view images and capture view images are displayed in display 140. The display 140 may include an electronic view finder (EVF) that is connected to the image processing apparatus 130 via an MIPI display serial interface (MIPI DSI) (not shown) specified by the Mobile Industry Processor Interface (MIPI) Alliance, but is not limited thereto. The display 140 may also include a back display of the digital camera (not shown) that is also connected to the image processing apparatus 130 via an MIPI.

[0033] The storage medium 150 is a non-transitory computer readable storage medium, for example, a solid-state drive (SSD), but is not limited thereto. Any other non-transitory computer readable storage medium can be also utilized as the storage medium 150.

[0034] FIG. 2 shows a schematic illustration of an image pre-processing apparatus 120. The image pre-processing apparatus 120 includes an image data receiver 210, a direct memory access (DMA) controller 220, a data interface 230 and an imager data interface 240 required for still image processing. The image data receiver 210 is configured to receive an image frame from the image sensor 110. The image frame has a frame pixel resolution that is substantially equal to the sensor pixel resolution of the image sensor. In other words, the image frame includes image information of all sensor pixels of the active area of the image sensor.

[0035] The data interface 230 connects the image pre-processing apparatus 120 to a buffer memory 250 in the image processing apparatus 130. The imager data interface 240 connects the pre-processing apparatus 120 to an ISP 260. The DMA controller 220 is in communication with the image data receiver 210, the data interface 230, and the imager data interface 240, and is configured to store the image frame to the buffer memory 250 via the data interface 230, to receive first and second image subframes from the buffer memory 250 via the data interface 230, and to consecutively transmit the first and second subframes to the ISP 260 via the imager data interface 240.

[0036] Reference is now made to FIG. 3, which shows another more detailed schematic illustration of a camera system 300 for processing digital images according to an exemplary embodiment of

the present invention. As shown in FIG. 3, the camera system 300 includes an image pre-processing apparatus 310 to which image sensor 110 is connected, and an image processing apparatus 330. The image processing apparatus 330 is in communication with image pre-processing apparatus 310, display 140, and storage medium 150.

[0037] The image processing apparatus 330 in the exemplary embodiment of the camera system 300 shown in FIG. 3 has a system on chip (SoC) architecture and integrates all components necessary to process an image frame received from an image sensor to generate digital images that can be displayed, printed or stored. Thus, image processing apparatus 330 includes image processor 342 which may be implemented, for example, as a digital signal processor (DSP) or a graphics processing unit (GPU). Image processing apparatus 330 further includes a first ISP 338 and data transceiver 332 configured to receive and transmit image frames to be stored in still image pre-buffer 334. In addition, an image data receiver 336 is provided which is configured to receive image subframes to be processed by the ISP 338. The image subframes processed by the ISP 338 are stored in still image post-buffer 340. A display controller 352 is provided which performs operations to allow the image frame captured by the image sensor 110 to be visible on the entire display 140. The display controller 352 is connected to the display 140 via display data transmitter 354. To store still image frames in a graphics image format or image frames in a raw image format in the storage medium 150, a storage controller 356 and a storage interface 358 are provided.

[0038] The image pre-processing apparatus 310 includes a data transceiver 312 and a first imager data transmitter 314. Data transceiver 312 and data transceiver 332 form a data interface between the image pre-processing apparatus 310 and the image processing apparatus 330. The data

interface 312, 332 may be a high-speed serial computer expansion bus standard interface, such as a Peripheral Component Interconnect Express (PCIe) standard interface, but is not limited thereto.

[0039] Like the data interface 312, 332, the imager data transmitter 314 together with the imager data receiver 336 form another interface (i.e., an imager data interface) between the image pre-processing apparatus 310 and the image processing apparatus 330. Data transceiver 312 and imager data transmitter 314 are controlled by receive DMA (RX-DMA) controller 316 and transmit DMA (TX-DMA) controller 318. RX-DMA controller 316 is in communication with imager data transmitter 314 via first in first out (FIFO) buffer 320. Image pre-processing apparatus 310 also includes image data receiver 322 and pixel processor 324 which is in communication with TX-DMA controller 318 via FIFO buffer 326.

[0040] The first and second imager data interfaces 314, 336 and 346, 348 according to the exemplary embodiment shown in FIG. 3 are Mobile Industry Processor Interface (MIPI) Camera Serial Interface (CSI) image data interfaces. The imager data interfaces, however, are not limited to MIPI CSI and any other serial interfaces can also be utilized instead.

[0041] In the exemplary embodiment shown in FIG. 3, the image pre-processing apparatus 310 is implemented as a field-programmable gate array (FPGA). However, the image pre-processing apparatus 310 may also be implemented as an application-specific integrated circuit (ASIC).

[0042] Image pre-processing apparatus 310 further includes image downsizer 328 that is connected via FIFO buffer 344 to a second imager data transmitter 346 that forms together with a second

imager data receiver 348 a second imager data interface. The imager data receiver 348 is connected to a second ISP 350.

[0043] Both imager data interfaces 314, 336 and 346, 348 can be utilized in still capture mode. The ISPs 338 and 350 are configured upon entering the still capture mode and do not change between live view states and capture states. Still image processing is performed by image pre-processing apparatus 310, ISP 338, and image processor 342.

[0044] As discussed above, image sensor 110 is operated in different modes, i.e., in live view mode and in a still capture mode. The first imager data interface 314, 336 together with ISP 338 are only used when still image frames are captured. The second imager data interface 346, 348 together with ISP 348 are only utilized for live view and capture preview.

[0045] In both modes, the full active area of the image sensor is used. When an image frame is received from the image sensor 110 by the image data receiver 322 of the image pre-processing apparatus 310, the sensor pixels are corrected by pixel processor 324 in both modes. However, while in still capture mode, all lines and columns are read out from the image sensor 110, in live view mode, lines may be skipped to enable a high frame rate. For example, in live view, the image sensor 110 may output only one quarter of the lines, but all columns. Since the imager data interface 346, 348 may support only a limited data rate, after pixel corrections, the frames may be horizontally resized 4:1 by the image downsizer 328 to accommodate the limited data rate. The image frames in live view are processed by ISP 350 and then asymmetrically scaled to the correct resolution for the display 140.

[0046] A typical aspect ratio of the image sensor 110 is 3:2, whereas a typical aspect ratio of the display 140 is 16:9. If, for example, the aspect ratio of the image sensor 110 is 3:2 and the aspect ratio of the display 140 is 16:9, black bars may be added at the display controller 352 so that the entire image frame received from the image sensor 110 is visible on the display 140.

[0047] In still capture mode, all lines and columns of the image sensor 110 are read out. For still capture view, pixel correction is performed by pixel processor 324 the same way as for live view mode. However, row skipping is also done by image downsizer 328. As a result, the format of the image data transmitted via imager data interface 346, 348 in still capture mode is the same as in live view mode and no reconfiguration of ISP 350 is required. Still image capture frames are displayed as they are captured by the image sensor 110 at a much lower frame rate than the live view image frames.

[0048] Since the live view image frames and still image capture frames usually have different integration times, and captures may be flash illuminated, there may be exposure and white balance changes between the image path flowing through ISP 350 and the image path flowing through ISP 338. Image statistics are collected in ISP 350 and the statistical data is used to determine exposure, white balance, and focus corrections for both live view by ISP 350 and subsequent processing of still image frames by ISP 336.

[0049] Imager data interface 314, 336 and ISP 338 are only used when still image frames are captured. During still image capture, full resolution frames are output from the image pre-processing apparatus via data transceivers 312 and 332 to the image processing apparatus 330 and

stored in a memory area of still-image pre-buffer 334. When a complete full resolution image frame captured from the image sensor 110 is stored in the still image pre-buffer, pre-ISP processing is performed by the image processor 342. After the pre-ISP processing is complete, pre-ISP processed image frame may be stored in storage medium 150 by storage controller 356 in a raw image format, for example in a digital negative (DNG) format.

[0050] Since the ISP 338 has a processing capacity that cannot accommodate the full sensor width, the ISP 338 is not capable of processing the entire image frame generated by the image sensor 110 during still capture mode, the image frame needs to be processed in image subframes, i.e., in tiles or portions of half the image width. For this purpose, the image frame is divided by the image processor 342 into first and second image subframes to be sequentially processed by the ISP 338. Each of the first and the second image subframes has a subframe pixel resolution that is smaller than the sensor pixel resolution and a region in which the first and second image subframes overlap with each other. The subframe pixel resolution is predetermined by a processing capacity of the ISP 338. Thereafter, the first and the second image subframes are consecutively processed by the ISP 338.

[0051] In other words, the image data is transferred back over the data interface 312, 332 to the image pre-processing apparatus 310 where it is streamed over the imager data interface 314, 336 to the front end of ISP 338. As each image subframe is processed, it is stored in the still image post-buffer 340 and reassembled into a complete image with a high image quality.

[0052] In recent years, the development of image sensors resulted in a fast increase of available

pixel resolution of image sensors. At the same time, the development of cost effective ISPs with a corresponding processing power has fallen behind and created a potential bottleneck. The above-described approach significantly improves the quality of the complete image, and it also improves the overall performance of systems performing processing of digital images which include ISPs that are not capable of processing the entire image frame generated by the image sensor 110 during still capture mode, for example. Accordingly, hardware costs can be reduced and the impact of the bottleneck in processing power of ISPs can be minimized.

[0053] The image processor 342 performs post-ISP processing on the image subframes in the still-image post-buffer. At this point, a finished image frame in a graphics image format, for example, in the YCbCr tagged image file format (TIFF) or in the joint photographic experts group (JPEG) format may be stored to storage medium 150. It is also possible to compress the finished image frame by a JPEG encoder (not shown) before storing it to the storage medium 150.

[0054] The processing of image subframes is asynchronous with the capture of image frames, is somewhat slower than the capture of the image frames and may continue as a background process after the image sensor 110 returns to live view mode. In the case of a burst capture, it takes considerably more time to save up to three files per frame, so the still image pre-buffer 334 empties relatively slowly compared to the fill rate during a burst. When the still image pre-buffer is full, captures will be blocked, even if the user holds the shutter button of the camera. As the buffer is emptied, additional burst frames can be captured.

[0055] FIG. 4A shows an illustration of an image frame 410 generated by image sensor 110.

Although FIG. 4A shows a frame which has a number of pixel columns (representing the pixel width) of the image frame that is larger than the number of pixel rows (representation the pixel height) of the image frame, any other ratio between width and height is possible. In the exemplary embodiment shown in FIGS. 4A to 4C, the image frame 410 is vertically divided, by way of example, at the dotted line shown in FIG. 4A into first and second image subframes. However, any other division of the image frame 410 is also possible. For example, the image frame 410 may be horizontally divided into three subframes, the image frame 410 may also be further divided vertically, or otherwise, as long as the resulting subframes have an image subframe resolution that can be processed by ISP 338.

[0056] FIG. 4B shows an illustration of a first image subframe 420 generated from the image frame 410 by image processor 342, and FIG. 4C shows an illustration of a second image subframe 440 generated from the image frame 410 by image processor 342. As shown in FIGS. 4B and 4C, each of the first and second image subframes have a region 430, 450 in which the first and second subframes 420 and 440 overlap with each other.

[0057] Referring now to FIG. 5 (with reference to FIGS. 3 and 4A to 4C), in which a flow chart is shown illustrating method 500 including operations performed by the camera system 100 to process an image frame 410 according to an exemplary embodiment of the invention. Method 500 begins at step 510 where an image frame 410 is received from image sensor 110, which is operated in still image mode. At 520, the image frame 410 is divided into first and second image subframes 420 and 440, and at 530, the first and second image subframes 420 and 440 are consecutively processed by ISP 338.

[0058] Reference is now made to FIG. 6 (with continued reference to FIGS. 3 and 4A to 4C). FIG. 6 is a flow chart showing a method 600 for operating the camera system 100 to generate a still image frame according to an exemplary embodiment of the invention. The method begins at step 605 in which defects in the image frame 410 are corrected by pixel processor 324. The method continues to 610 at which the corrected image frame is transmitted to still image pre-puffer 334 shown in FIG. 3 by TX-DMA controller 318 of image pre-processing apparatus 310. At 615, the image frame 410 is stored in still image pre-buffer 334 and at 620, first image subframe 420 is received by RX-DMA controller 316 of image pre-processing apparatus 310 via data interface 312, 332. The first image subframe 420 is generated by image processor 342 in still image pre-buffer before being transmitted to the image pre-processing apparatus.

[0059] The method continues to 625 at which the first image subframe 420 is transmitted via imager data interface 314, 336 by RX-DMA controller 316 to ISP 338 where it is processed at 630 by the ISP 338. At 635, a second image subframe 440 is received from still image pre-buffer 334 by RX-DMA controller 316 of image pre-processing apparatus 310, and at 640, the second image subframe 440 is transmitted to the ISP 338 via imager data interface 314, 336 where it is processed by ISP 338 at 645. The method concludes with 650 at which the processed first and second image subframes 420 and 440, that are stored after being processed by ISP 338 in still image post-buffer 340, are reassembled in Still Image post-buffer 340 to a still image frame. The reassembling or subframe merging in the Still Image post-buffer 340 is configurable and overlapping regions are determined by the image quality parameters and spatial components determined in the ISP 338.

[0060] The processing engines of the ISP 338 are configured in such a way that the spatial

components in pre-processing and post-processing of the image may minimize the image quality which may affect the subframe processing and the final still image frame.

[0061] Noise filtering and other fixed pattern noise removal are performed by the Image Processor 342 on the entire image. The pre-processing block is tuned in such a way that minimal sensor specifics like ADC, pedestal corrections, black offset removal processing, etc., is performed outside the ISP 338 to avoid any spatial artefacts which depend on the full frame capture.

[0062] FIG. 7 shows a schematic illustration of an image pre-processing apparatus 720 of a camera system 700. The image pre-processing apparatus 720 includes an image data receiver 210 and an imager data interface 240 for still image processing. The configuration of the image data receiver 210 and of the data interface 240 has already been discussed with regard to FIG. 2.

[0063] As shown in FIG. 7, image pre-processing apparatus 720 does not require a DMA controller and a data interface to store image frame 410 to the buffer memory 250, to receive first and second image subframes 420 and 440 from the buffer memory 250 and to consecutively transmit first and second subframes to the ISP 260. Instead, in the second exemplary embodiment, image frame 410 generated by image sensor 110 is transmitted from image sensor 110 through image pre-processing apparatus 720 via image data receiver 210 and imager data interface 240 to pre-processor 730. Pre-processor 730 stores image frame 410 in buffer memory 250, receives first and second image subframes 420 and 430 from the buffer memory 250 and consecutively transmits the first and second subframes to the ISP 260.

[0064] FIG. 8 shows a schematic illustration of a camera system 800 for processing digital images according to a third exemplary embodiment of the invention. In this exemplary embodiment, image sensor 110 is directly connected to pre-processor 730 without an intermediate image pre-processing apparatus. As a result, in the camera system 800 shown in FIG. 8, image processor 110 directly transmits image frame 410 to pre-processor 730 which stores image frame 410 in buffer memory 250, receives first and second image subframes 420 and 430 from the buffer memory 250 and consecutively transmits the first and second subframes to the ISP 260.

[0065] Reference is now made to FIG. 9, which shows a detailed schematic illustration of camera system 700 for processing digital images according to the second exemplary embodiment of the invention. As shown in FIG. 9, the camera system includes an image pre-processing apparatus 910 to which image sensor 110 is connected, and an image processing apparatus 930. The image processing apparatus 930 is in communication with image pre-processing apparatus 910, display 140, and storage medium 150. For better clarity, the description of elements that are the same as in the FIG 3 is omitted.

[0066] The image processing apparatus 930 in the second exemplary embodiment of the camera system shown in FIG. 9 has a SoC architecture and integrates all components necessary to process an image frame received from an image sensor to generate digital images that can be displayed, printed or stored. In particular, image processing apparatus 930 includes pre-processor 932. Pre-processor 932 performs operations to allow image frame 410 received by image data receiver 336 to be stored in still-image pre-buffer 334. In addition, pre-processor 932 is configured to receive first and second image subframes 420 and 430 generated by image processor 342 from still-image

pre-buffer 334 and to consecutively transmit the first and second image subframes 420 and 430 to ISP 338. Thus, pre-processor 932 provides a data path for the first and second image subframes 420 and 430 from the still image pre-buffer 334 back into the front end of ISP 1 without modifying the data.

[0067] ISPs such as ISP 338 are typically complex structures and permit a plurality of operating parameters to be set. Therefore, the data path is needed to permit a test image to be processed by the ISP a plurality of times with different parameters. This allows the same image to be replayed multiple times until the correct parameters are set. Thereby, the ISP and the configuration of the ISP can be tested. Such a test within the SoC would not be possible if the configuration of the image processing apparatus would only allow the ISP to receive live data from an image sensor.

[0068] The image processing apparatus 310 shown in FIG. 3 does not include the data path between still image pre-buffer 334 and ISP 338. Therefore, the data path in the exemplary embodiment shown in FIG. 3 is created by pre-processing apparatus 310 via data interfaces 332 and 312, receive DMA controller 316, FIFO 320, image data transmitter 314, and image data receiver 336.

[0069] Since the data path for the first and second image subframes 420 and 430 from the still image pre-buffer 334 to the ISP 338 in the exemplary embodiment shown in FIG. 9 is provided via pre-processor 932, in the image pre-processing apparatus 910, the image frame 410 after being processed by pixel processor 324 is transmitted to FIFO 320 and subsequently via image data transmitter 314 to pre-processor 932. FIFO 326, DMA controllers 318 and 316, and data interfaces 312 and 332 in the exemplary embodiment shown in FIG. 3 are omitted in FIG. 9.

[0070] FIG. 10 shows a detailed schematic illustration of camera system 800 for processing digital images according to the third exemplary embodiment of the invention. In FIG. 10, the image processing apparatus is entirely omitted and the image sensor 110 is directly connected to image data receiver 336 of the image processing apparatus 1030. In this exemplary embodiment, the image sensor 110 outputs image frame 410 in accordance with the communication standards of the image data receiver 336 and the corrections of the image data performed by the pixel processor 324 in the exemplary embodiments shown in FIGS. 3 and 9 are either performed by ISP 338 or are dispensed with.

[0071] As shown in FIG. 10, image processing apparatus 1030 does not include a second data path for live view via a separate ISP, such as ISP 350 in FIGS. 3 and 9. Therefore, in the exemplary embodiment shown in FIG. 10, view data is generated from still image post-buffer 340 and transmitted from still image post-buffer 340 to display controller 352.

[0072] According to yet another exemplary embodiment, the pre-processor 932 in FIGS. 9 and 10 can also be omitted and direct data paths (not shown) can be established between image data receiver 336 and still image pre-buffer 334, and between still image pre buffer 334 and ISP 338.

[0073] FIG. 11 shows a detailed schematic illustration of a camera system for processing digital images according to a fourth exemplary embodiment of the invention. As shown in FIG. 11, image processing apparatus 1130 includes a second data path for live view via ISP 350. That is, the image processing apparatus 1130 includes data paths from the imager data receiver 336 that allow one image sensor input to be routed to either of two or more ISPs.

[0074] In the exemplary embodiment shown in FIG. 11, the pre-image processor 932 may not be capable of downsizing the image frames in live view, or, as discussed above, the pre-processor 932 may be omitted entirely. However, many image sensors allow skipping or binning in both horizontal and vertical dimensions to reduce output resolution which allows directly connecting the image sensor 110 to the image processing apparatus 1130 and to perform live view via ISP 350, for example. Such image sensors can also be connected to the image processing apparatus 1030 or to any other image processing apparatus of the other exemplary embodiments discussed above to provide additional capabilities to reduce output resolution.

[0075] It is understood that the foregoing description is that of the exemplary embodiments of the invention and that various changes and modifications may be made thereto without departing from the spirit and scope of the invention as defined in the appended claims.

WHAT IS CLAIMED IS:

1. A method for processing digital images, the method comprising:

receiving from an image sensor an image frame, the image frame having a frame pixel resolution substantially equal to a sensor pixel resolution of the image sensor;

dividing the image frame into first and second image subframes to be sequentially processed by an image signal processor, each of the first and the second image subframes having a subframe pixel resolution smaller than the sensor pixel resolution and a region in which the first and second image subframes overlap with each other, the subframe pixel resolution being predetermined by a processing capacity of the image signal processor; and

consecutively processing the first and the second image subframes by the image signal processor.

2. The method of claim 1, wherein the dividing comprises horizontally dividing the image frame into the first and second image subframes.

3. The method of claim 1, wherein the dividing comprises vertically dividing the image frame into the first and second image subframes.

4. The method of claim 1, wherein the dividing comprises dividing the image frame into the first image subframe, the second image subframe, and at least one third image subframe.

5. The method of claim 1, wherein:

a first number of pixel rows of the image frame is substantially equal to a second

number of pixel rows of the first and second subframes; and

a first number of pixel columns of the image frame is larger than a second number of pixel columns of the first and second subframes.

6. The method of claim 1, further comprising:

correcting defects in the image frame;

transmitting the corrected image frame to a buffer memory;

storing the image frame in the buffer memory;

receiving the first image subframe from the buffer memory;

transmitting the first image subframe to the image signal processor;

processing the first image subframe by the image signal processor;

receiving the second image subframe from the buffer memory;

transmitting the second image subframe to the image signal processor upon completion of the processing of the first image subframe by the image signal processor; and

processing the second image subframe by the image signal processor.

7. The method of claim 1, wherein:

the buffer memory is a first buffer memory, and

the method further comprises:

storing the first and second image subframes in a second buffer memory after being processed by the image signal processor;

reassembling the first and second image subframes stored in the second buffer memory to a still image frame by a digital signal processor;

post-processing the still image frame by the digital signal processor; and

storing the post-processed still image frame in a non-transitory computer-readable storage medium in a graphics image format.

8. The method of claim 7, further comprising:

processing the image frame stored in the first buffer memory by the digital signal processor to remove a noise from the image frame; and

storing the image frame processed by the digital signal processor in the non-transitory computer-readable storage medium in a raw image format.

9. The method of claim 8, wherein the non-transitory computer-readable storage medium is a solid-state drive (SSD).

10. The method of claim 7, wherein the graphics image format is selected from the group consisting of a tagged image file format (TIFF) and a joint photographic experts group (JPEG) format.

11. The method of claim 8, wherein the raw image format is a digital negative (DNG) format.

12. The method of claim 8, wherein the digital signal processor is a graphics processing unit (GPU).

13. The method of claim 1, further comprising:

receiving the image frame from the image sensor at an image pre-processing apparatus, the pre-processing apparatus including a pixel processor, a data interface, and an image data transmitter;

correcting defects in the image frame by the pixel processor;

transmitting the image frame to a buffer memory via the data interface;

storing the image frame in the buffer memory;

receiving the first image subframe via the data interface from the buffer memory;

transmitting the first image subframe via the imager data interface to the image signal processor;

processing the first image subframe by the image signal processor;

receiving the second image subframe via the data interface from the buffer memory;

transmitting the second image subframe via the imager data interface to the image signal processor upon completion of the processing of the first image subframe by the image signal processor; and

processing the second image subframe by the image signal processor.

14. The method of claim 13, wherein the pre-processing apparatus is a field-programmable gate array (FPGA).

15. The method of claim 1, wherein:

the image signal processor is a first image signal processor,

the imager data interface is a first imager data interface, and

the method further comprises:

resizing the image frame to a capture view image frame by removing at least one of a column and a row of pixels from the image frame;

transmitting the capture view image frame via a second imager data interface to a second image signal processor;

processing the capture view image frame by the second image signal processor; and

displaying the capture view image frame on a display.

16. An image pre-processing apparatus comprising:

an image data receiver configured to receive an image frame from an image sensor, the image frame having a frame pixel resolution substantially equal to a sensor pixel resolution of the image sensor;

a data interface and an imager data interface;

a direct memory access (DMA) controller in communication with the image data receiver, the data interface and the imager data interface, the DMA controller being configured to:

store the image frame to a buffer memory via the data interface;

receive first and second image subframes being generated from the image frame by dividing the image frame into the first and second image subframes to be processed by an image signal processor, each of the first and the second image subframes having a subframe pixel resolution smaller than the sensor pixel resolution and a region in which the first and second image subframes overlap with each other, the subframe pixel resolution being predetermined by a processing capacity of the image signal processor; and

consecutively transmit the first and second subframes to the image signal processor via the imager data interface.

17. The image pre-processing apparatus of claim 16, wherein the image frame is horizontally divided into the first and second image subframes.

18. The image pre-processing apparatus of claim 16, wherein the image frame is vertically divided into the first and second image subframes.

19. The image pre-processing apparatus of claim 16, wherein the image frame is divided into the first image subframe, the second image subframe, and at least one third image subframe.

20. The image pre-processing apparatus of claim 16, further comprising:

a pixel processor configured to correct defects in the image frame received from the image sensor via the image data receiver.

21. The image pre-processing apparatus of claim 16, wherein:

the image signal processor is a first image signal processor,

the imager data interface is a first imager data interface,

the image pre-processing apparatus further comprises an image downsizer in communication with the pixel processor and configured to:

receive the corrected image frame from the pixel processor;

resize the corrected image frame to a capture view image frame by removing at least one of a column and a row of pixels from the corrected image frame; and

transmit the capture view image frame via a second imager data interface to a second image signal processor to be processed and displayed on a display.

22. The image pre-processing apparatus of claim 16, wherein the image pre-processing apparatus is a field-programmable gate array (FPGA).

23. A camera system for processing digital images, the system comprising:

an image sensor;

an image processing apparatus in communication with the image sensor and including a buffer memory and an image signal processor; and

a display connected to the image processing apparatus.

24. The camera system of claim 23, wherein the image processing apparatus further comprises a digital signal processor configured to divide the image frame stored in the buffer memory into the first and second image subframes to be processed by the image signal processor, each of the first and the second image subframes having a subframe pixel resolution smaller than the sensor pixel resolution and a region in which the first and second image subframes overlap with each other, the subframe pixel resolution being predetermined by a processing capacity of the image signal processor.

25. The camera system of claim 24, further comprising:

a non-transitory computer-readable storage medium connected to the image processing apparatus;

wherein:

the buffer memory is a first buffer memory;

the image processing apparatus further comprises a second buffer memory in which the first and second image subframes are stored after being processed by the image signal processor;

the digital signal processor is configured to:

reassemble the first and second image subframes stored in the second buffer memory to a still image frame;

post-process the still image frame; and

store the post-processed still image frame in the non-transitory computer-readable storage medium in a graphics image format.

26. The camera system of claim 25, wherein the digital signal processor is further configured to:

process the image frame stored in the first buffer memory by the digital signal processor to remove noise from the image frame, and

store the image frame processed by the digital signal processor in the non-transitory computer-readable storage medium in a raw image format.

27. The camera system of claim 25, wherein the non-transitory computer-readable storage medium is a solid-state drive (SSD).

28. The camera system of claim 25, wherein the graphics image format is selected from the group consisting of a tagged image file format (TIFF) and a joint photographic experts group (JPEG) format.

29. The camera system of claim 26, wherein the raw image format is a digital negative (DNG) format.

30. The camera system of claim 25, wherein the digital signal processor is a graphics processing unit (GPU).

31. The camera system of claim 23, further comprising:

an image pre-processing apparatus in communication with the image sensor;

the image pre-processing apparatus comprising:

an image data receiver configured to receive an image frame from the image sensor, the image frame having a frame pixel resolution substantially equal to a sensor pixel resolution of the image sensor;

a data interface and an imager data interface;

a direct memory access (DMA) controller in communication with the image data receiver, the data interface and the imager data interface, the DMA controller being configured to:

store the image frame to the buffer memory via the data interface;

receive first and second subframes being generated from the image frame; and

consecutively transmit the first and second subframes to the image signal processor via the imager data interface.

32. The camera system of claim 31, wherein the image pre-processing apparatus is a field-programmable gate array (FPGA).

33. The camera system of claim 23, further comprising:

an image pre-processing apparatus in communication with the image sensor and comprising:

an image data receiver to receive an image frame from the image sensor, the image frame having a frame pixel resolution substantially equal to a sensor pixel resolution of the image sensor;

an imager data transmitter to transmit the image frame to the buffer memory, and

wherein the image processing apparatus includes a pre-processor configured to:

store the image frame to the buffer memory;

receive first and second subframes being generated from the image frame; and

consecutively transmit the first and second subframes to the image signal processor.

34. The camera system of claim 31, wherein:

the image signal processor is a first image signal processor,

the image processing apparatus further comprises a second image signal processor;

the imager data interface is a first imager data interface; and

the image pre-processing apparatus further comprises a second imager data interface and an image downsizer, the image downsizer being in communication with the second imager data interface and configured to:

resize the image frame to a capture view image frame by removing at least one of a column and a row of pixels from the image frame; and

transmit the capture view image frame via the second imager data interface to the second image signal processor, the second image signal processor being configured to process the capture view image frame and to forward the processed capture view image frame to the display.

35. The camera system of claim 23, wherein:

the images sensor is at least one of a charge-coupled device (CCD) sensor, a complementary metal-oxide-semiconductor (CMOS) sensor, and an N-type metal-oxide-semiconductor (NMOS) sensor; and

the image sensor has a pixel resolution that is larger than the processing capacity of the image signal processor.

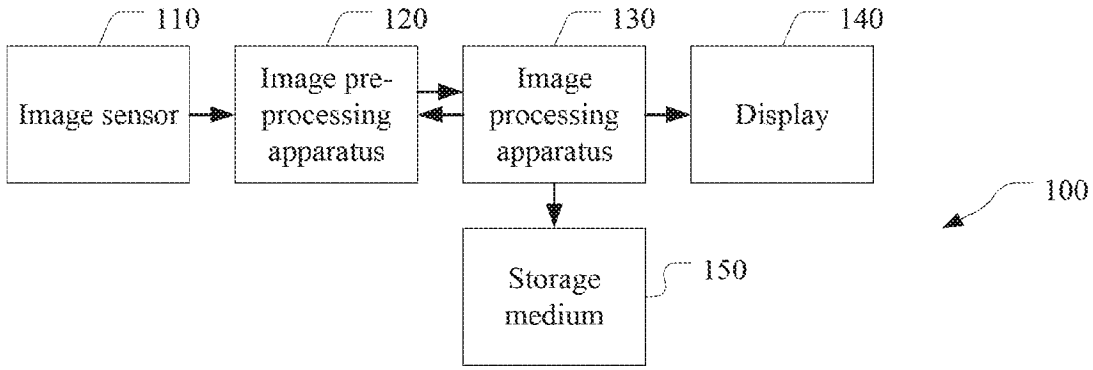

110
120
130
140
Image sensor
Image pre-processing apparatus
Image processing apparatus
Display
100
Storage medium
150

FIG. 1

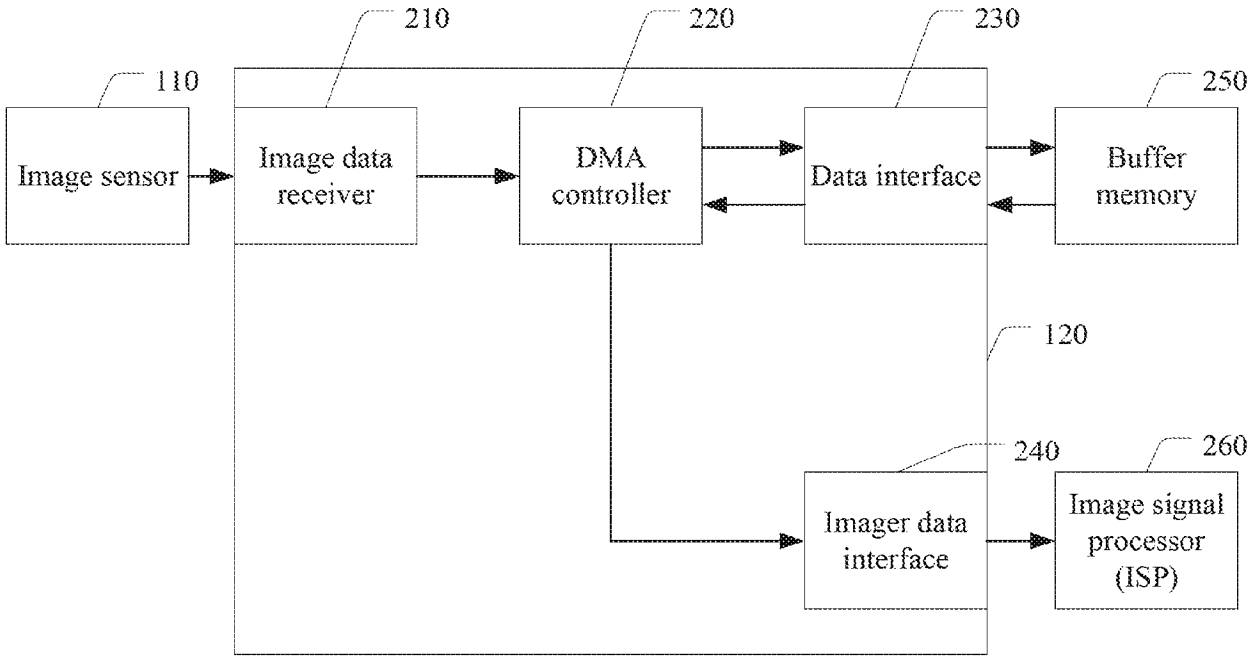

210
220
230
110
250
Image sensor
Image data receiver
DMA controller
Data interface
Buffer memory
120
240
260
Imager data interface
Image signal processor (ISP)

FIG. 2

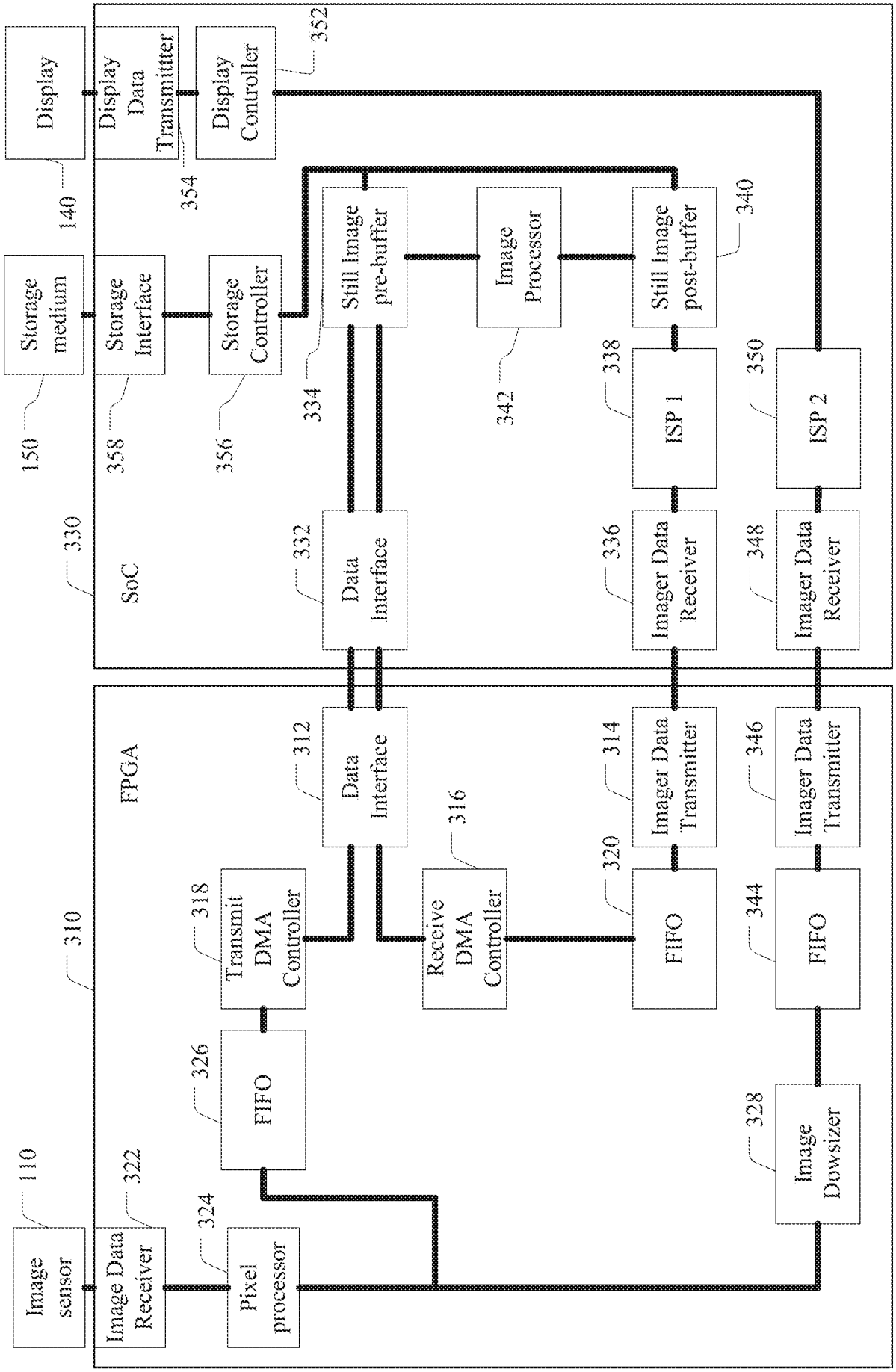

Display
Display Data Transmitter
Display Controller
352
354
140
Storage medium
Storage Interface
Storage Controller
Still Image pre-buffer
Image Processor
Still Image post-buffer
340
150
358
356
334
342
338
ISP 1
350
ISP 2
330
SoC
332
Data Interface
336
Imager Data Receiver
348
Imager Data Receiver
FPGA
312
Data Interface
314
Imager Data Transmitter
346
Imager Data Transmitter
316
310
318
Transmit DMA Controller
Receive DMA Controller
320
FIFO
344
FIFO
326
FIFO
328
Image Dowsizer
110
322
324
Image sensor
Image Data Receiver
Pixel processor

FIG. 3

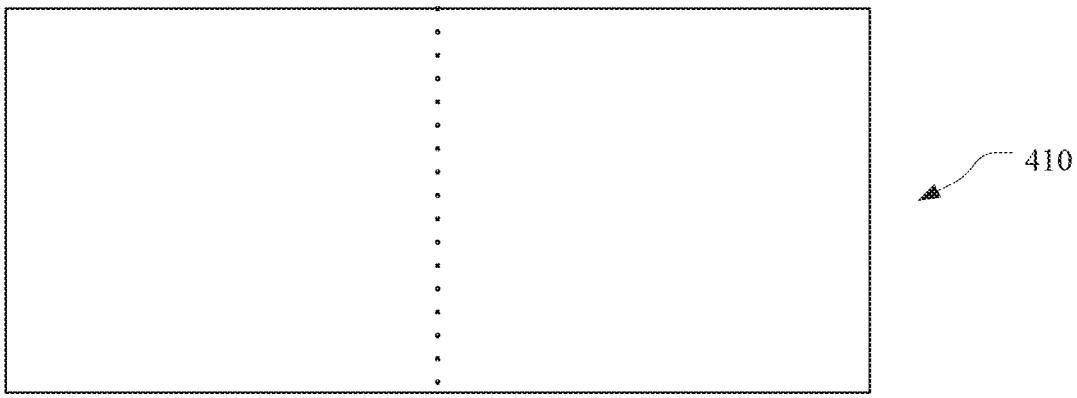


FIG. 4A

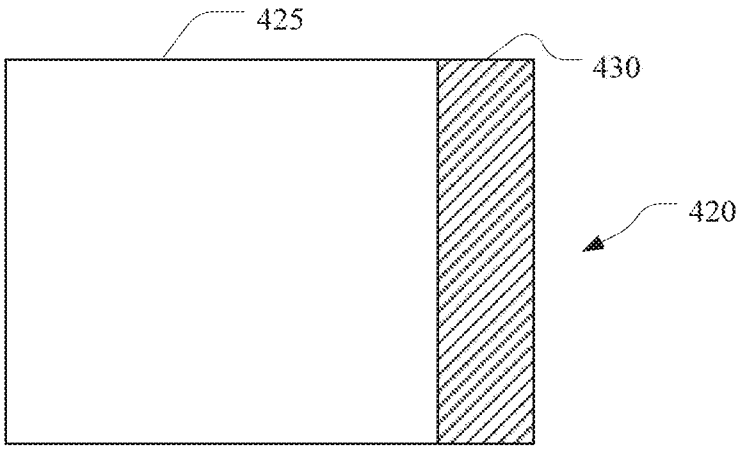


FIG. 4B

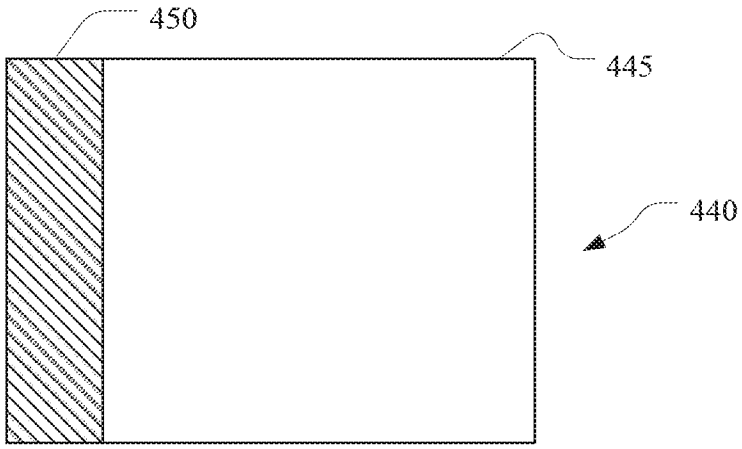


FIG. 4C

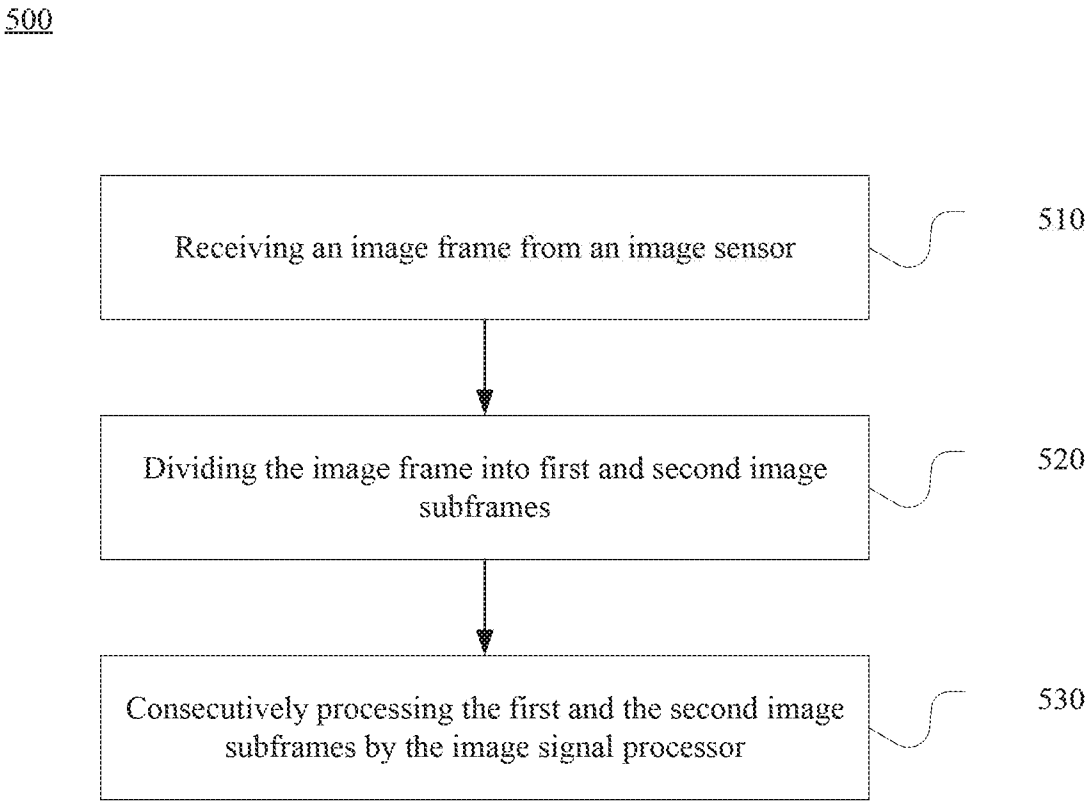

500
Receiving an image frame from an image sensor
510
Dividing the image frame into first and second image subframes
520
Consecutively processing the first and the second image subframes by the image signal processor
530

FIG. 5

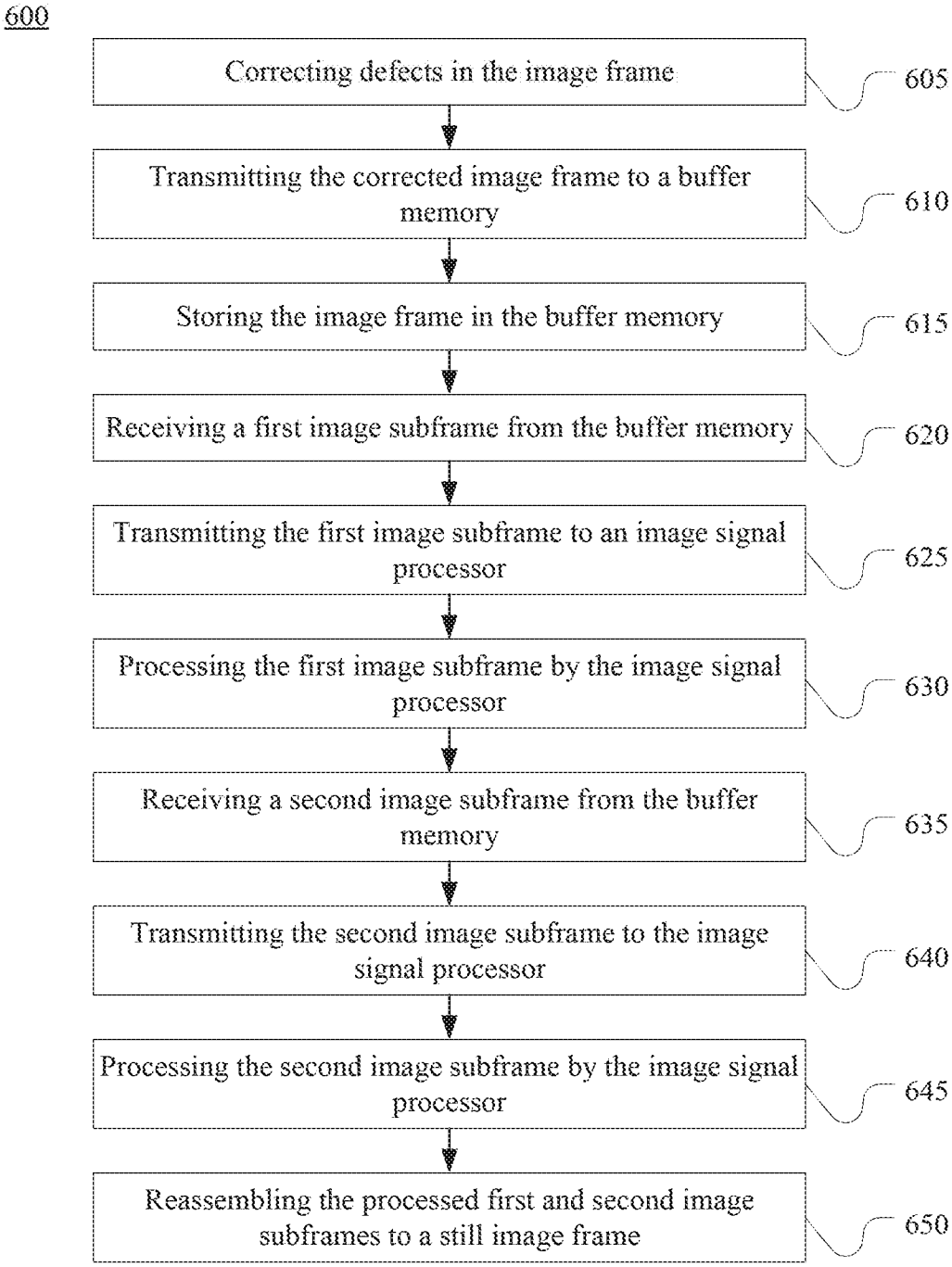

600
Correcting defects in the image frame
605
Transmitting the corrected image frame to a buffer memory
610
Storing the image frame in the buffer memory
615
Receiving a first image subframe from the buffer memory
620
Transmitting the first image subframe to an image signal processor
625
Processing the first image subframe by the image signal processor
630
Receiving a second image subframe from the buffer memory
635
Transmitting the second image subframe to the image signal processor
640
Processing the second image subframe by the image signal processor
645
Reassembling the processed first and second image subframes to a still image frame
650

FIG. 6

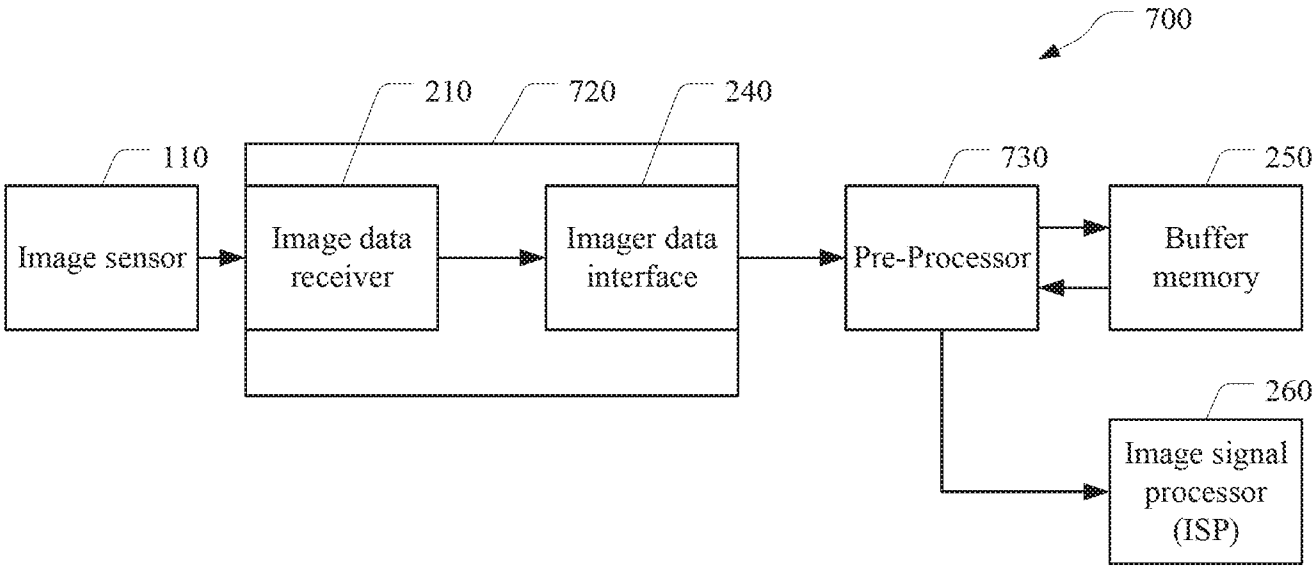

700
210
720
240
110
730
250
Image sensor
Image data receiver
Imager data interface
Pre-Processor
Buffer memory
260
Image signal processor (ISP)

FIG. 7

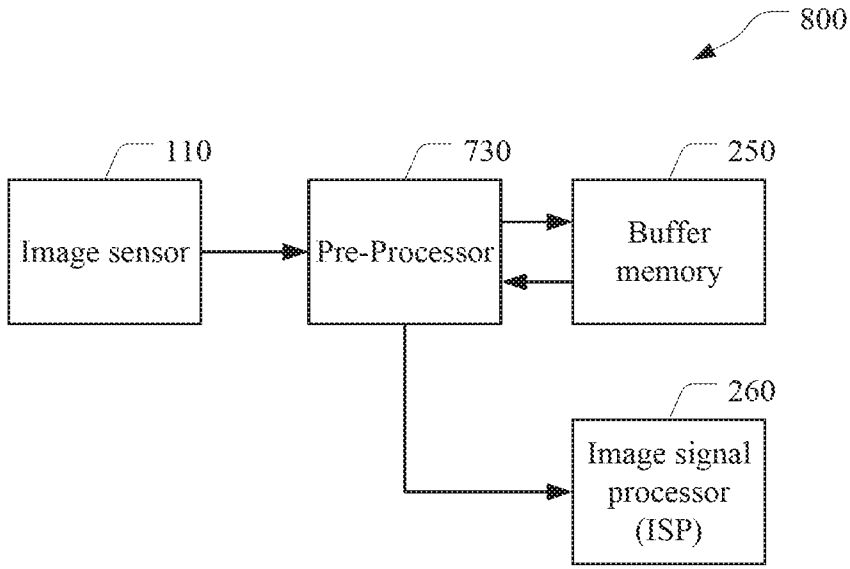

800
110
730
250
Image sensor
Pre-Processor
Buffer memory
260
Image signal processor (ISP)

FIG. 8

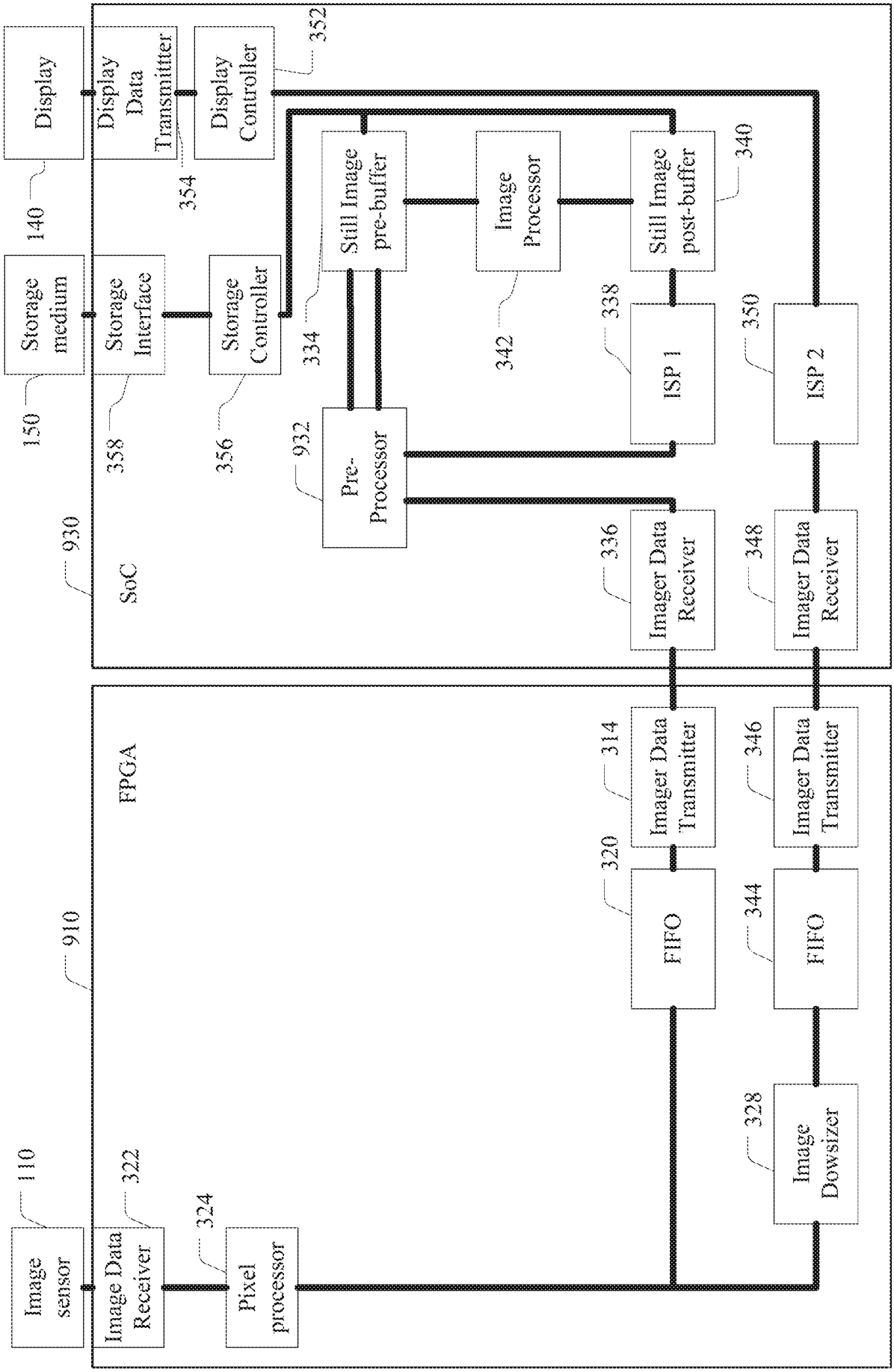

Image sensor
110
Image Data Receiver
322
Pixel processor
324
FPGA
910
Image Dowsizer
328
FIFO
344
FIFO
320
Imager Data Transmitter
346
Imager Data Transmitter
314
Imager Data Receiver
348
Imager Data Receiver
336
ISP 2
350
ISP 1
338
Image Processor
342
Still Image post-buffer
340
Still Image pre-buffer
334
Pre-Processor
932
SoC
930
Storage Controller
356
Storage Interface
358
Storage medium
150
Display Controller
352
Display Data Transmitter
354
Display
140

FIG. 9

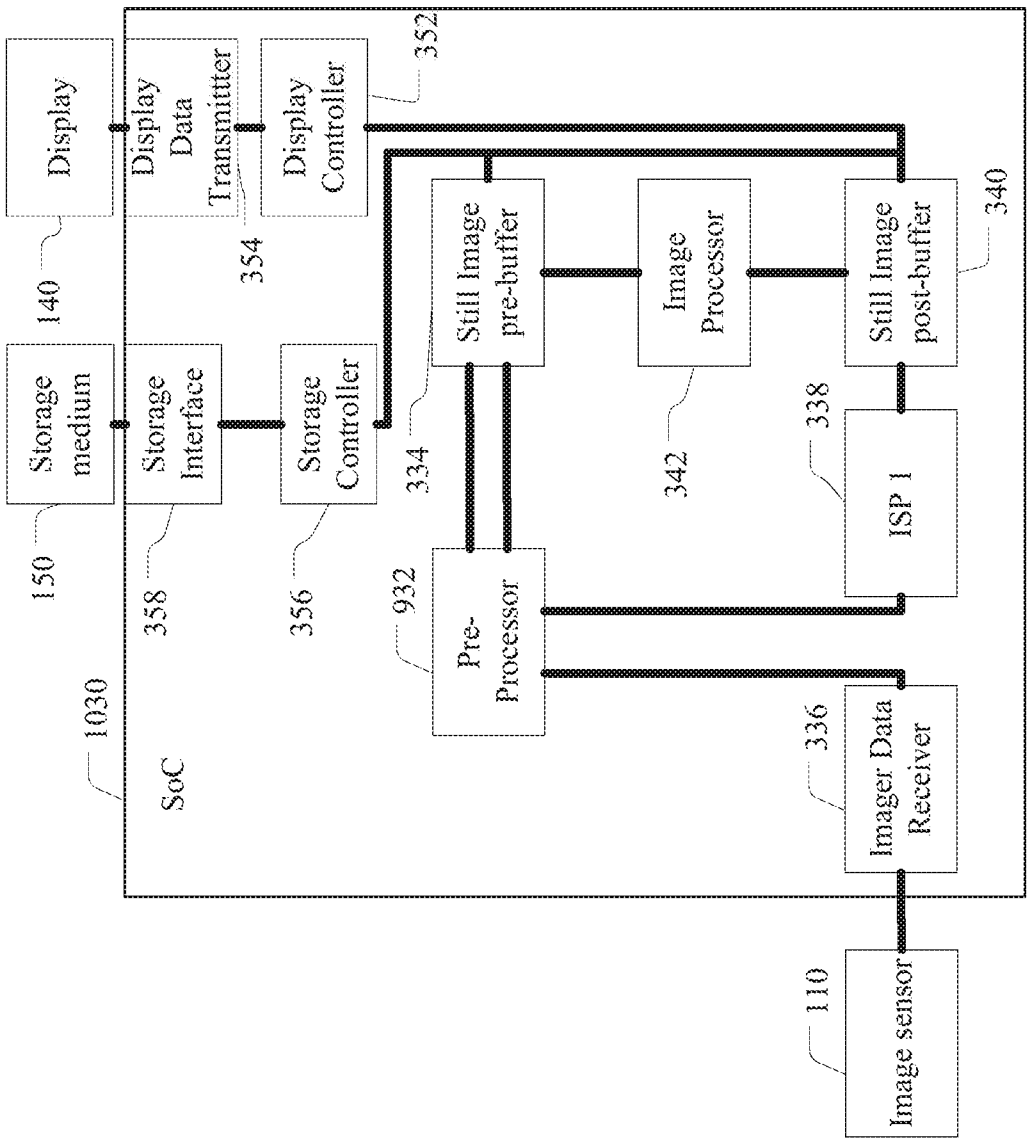

Display
140
Display Data Transmitter
354
Display Controller
352
Storage medium
150
Storage Interface
358
Storage Controller
356
Still Image pre-buffer
334
Image Processor
342
Still Image post-buffer
340
ISP 1
338
Pre-Processor
932
Imager Data Receiver
336
SoC
1030
Image sensor
110

FIG. 10

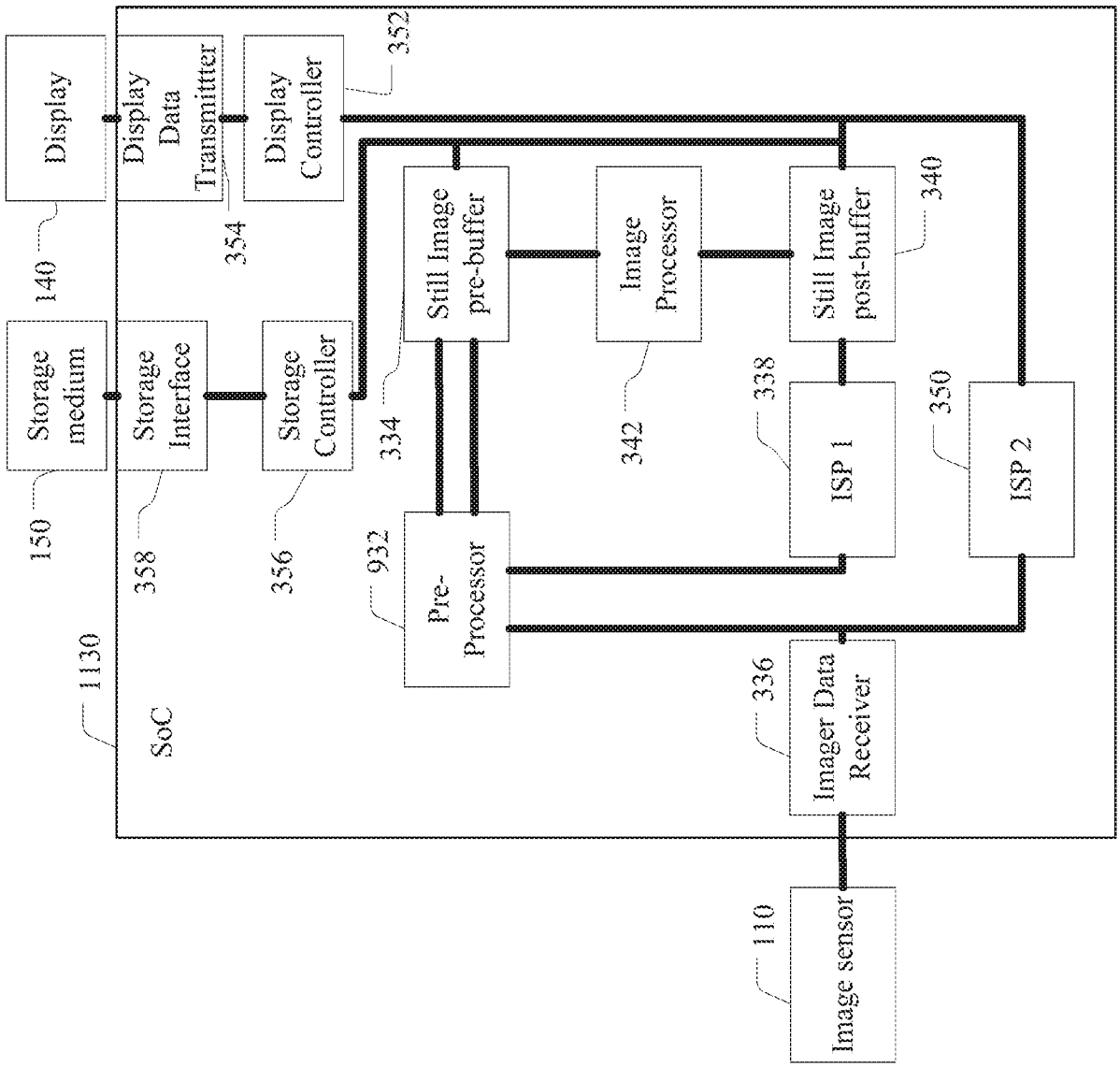

Display
Display Data Transmitter
Display Controller
352
140
354
Storage medium
Storage Interface
Storage Controller
Still Image pre-buffer
Image Processor
Still Image post-buffer
340
150
358
356
334
342
338
ISP 1
350
ISP 2
932
Pre-Processor
1130
SoC
336
Imager Data Receiver
110
Image sensor

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/036687

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H04N 3/15; H04N 9/04; H04N 1/21; H04N 5/222; H04N 5/225 (2019.01)
CPC - H04N 5/3454; H04N 9/045; H04N 1/0044; H04N 1/2112; H04N 1/2158 (2019.08)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 348/E3.02; 348/E9.01; 348/234; 348/558; 348/564 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/0177021 A1 (SHAN et al) 02 August 2007 (02.08.2007) entire document	23
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A		1-22
A	US 2014/0043435 A1 (BLAYVAS) 13 February 2014 (13.02.2014) entire document	1-22
A	US 2008/0002160 A1 (CHANG et al) 03 January 2008 (03.01.2008) entire document	1-22
A	US 5,047,858 A (AIMONOYA) 10 September 1991 (10.09.1991) entire document	1-35
A	CHAN. "Digital Imaging- Pixels and Sensors." In: Seawood Photo. 27 January 2018 (27.01.2018) Retrieved on 11 August 2019 (11.08.2019) from <https://www.seawood.com/seawoodblog/2018/1/27/digital-imaging-pixels-and-sensors> entire document	1-35
A	US 6,788,338 B1 (DINEV et al) 07 September 2004 (07.09.2004) entire document	1-35
A	US 6,292,218 B1 (PARULSKI et al) 18 September 2001 (18.09.2001) entire document	1-35

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 August 2019	22 AUG 2019

Name and mailing address of the ISA/US	Authorized officer
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-8300	Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774