(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) **World Intellectual Property Organization**
International Bureau

(43) **International Publication Date**
16 January 2020 (16.01.2020)

(10) **International Publication Number**
WO 2020/014352 A1

(51) **International Patent Classification:**
H01L 21/768 (2006.01) *H01L 21/027* (2006.01)

(21) **International Application Number:** PCT/US2019/041193

(22) **International Filing Date:** 10 July 2019 (10.07.2019)

(25) **Filing Language:** English

(26) **Publication Language:** English

(30) **Priority Data:**
62/696,692 11 July 2018 (11.07.2018) US
62/729,145 10 September 2018 (10.09.2018) US

(71) **Applicant: TOKYO ELECTRON LIMITED** [JP/JP]; Akasaka Biz Tower, 3-1 Akasaka 5-chome, Minato-ku, Tokyo 107-6325 (JP).

(71) **Applicant** *(for JP only)*: **TOKYO ELECTRON U.S. HOLDINGS, INC.** [US/US]; 2400 Grove Boulevard, Austin, Texas 78741 (US).

(72) **Inventors: KIKUCHI, Yuki**; Suite 214, NanoFab 300 South 255 Fuller Rd., Albany, New York 12203 (US). **WADA, Toshiharu**; Suite 214, NanoFab 300 South 255 Fuller Rd., Albany, New York 12203 (US). **MAEKAWA, Kaoru**; Suite 214, NanoFab 300 South 255 Fuller Rd., Albany, New York 12203 (US). **KO, Akiteru**; Suite 214, NanoFab 300 South 255 Fuller Rd., Albany, New York 12203 (US).

(74) **Agent: MADRIAGA, Manuel B.**; Tokyo Electron U.S. Holdings, Inc., 2400 Grove Boulevard, Austin, Texas 78741 (US).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,

(54) **Title:** METHODS TO REDUCE GOUGING FOR CORE REMOVAL PROCESSES USING THERMAL DECOMPOSITION MATERIALS

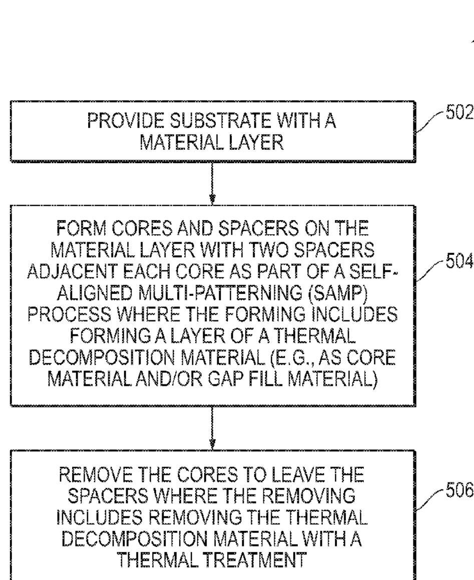
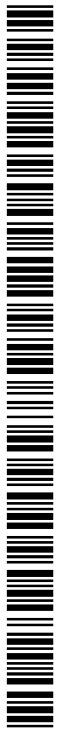


FIG. 5

(57) **Abstract:** Embodiments are disclosed that reduce gouging during multi-patterning processes using thermal decomposition materials. For one embodiment, gouging is reduced or suppressed by using thermal decomposition materials as cores during multiple patterning processes. For one embodiment, gouging is reduced or suppressed by using thermal decomposition materials as a gap fill material during multiple patterning processes. By using thermal decomposition material, gouging of an underlying layer, such as a hard mask layer, can be reduced or suppressed for patterned structures being formed using the self-aligned multi-patterning processes because more destructive etch processes, such as plasma etch processes, are not required to remove the thermal decomposition materials.



WO 2020/014352 A1

[Continued on next page]

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

METHODS TO REDUCE GOUGING FOR CORE REMOVAL PROCESSES USING THERMAL DECOMPOSITION MATERIALS

RELATED APPLICATIONS

5 **[0001]** This application claims priority to the following co-pending provisional applications: U.S. Provisional Patent Application Serial Number 62/696,692, filed July 11, 2018, and entitled "METHODS TO REDUCE GOUGING FOR MANDREL PULL PROCESSES," and U.S. Provisional Patent Application Serial Number 62/729,145, filed September 10, 2018, and entitled "METHODS TO REDUCE GOUGING FOR CORE 10 REMOVAL PROCESSES USING THERMAL DECOMPOSITION MATERIALS," which are hereby incorporated by reference in their entirety.

BACKGROUND

[0002] The present disclosure relates to methods for the manufacture of microelectronic workpieces including the formation of patterned structures on microelectronic workpieces.

15 **[0003]** Device formation within microelectronic workpieces typically involves a series of manufacturing techniques related to the formation, patterning, and removal of a number of layers of material on a substrate. To meet the physical and electrical specifications of current and next generation semiconductor devices, processing flows are being requested to reduce feature size while maintaining structure integrity for various patterning processes.

20 **[0004]** Self-aligned multiple patterning (SAMP) processes, such as self-aligned double patterning (SADP) processes and self-aligned quadruple patterning (SAQP), have been developed to reduce feature sizes beyond what is directly achievable by lithography processes.

[0005] For some SAMP processes and particularly for SADP processes, spacers are typically formed as side wall structures adjacent cores on a substrate being processed, and the 25 core material is later removed. For example, an organic film such as an organic planarizing layer (OPL) or an organic dielectric layer (ODL) is often used as a material for the cores, and oxide (SiO_2) is often used as a material to form spacers adjacent the ODL/OPL cores. The ODL/OPL core material is then removed after an etch back of the spacer material is used to form the spacers as side wall structures adjacent the cores. This core removal process is

typically called a mandrel pull and is often performed by a plasma etch process such as a reactive ion etch (RIE) process. These etch processes, however, can cause undesired gouging when exposed portions of an underlying layer, such as a hard mask layer, are not evenly etched during the etch process (*e.g.*, RIE process). As one example, the gouging amount for a hard
5 mask layer under the cores can differ from the gouging for the hard mask layer that is exposed within gaps between the cores and spacers. These differences in gouging can cause problems in later process steps. For example, these gouging differences can cause pitch-walking during subsequent wiring formation process and/or cause other subsequent processing defects for the microelectronic workpieces being manufactured.

10 **[0006]** For other SAMP processes and particularly for SAQP processes, amorphous silicon (a-Si) is used as the core material that is later removed in a mandrel pull process. A spacer material is deposited on this core material and an etch back of spacer material is then performed to form spacers adjacent the cores. The cores are then removed in the mandrel pull process. However, when an underlying layer such as a hard mask layer is exposed during the mandrel
15 pull process, differences in gouging can occur. For example, gouging of exposed portions of a hard mask layer during the etch process for the mandrel pull can differ from gouging associated with portions of the hard mask layer under the core material (*e.g.*, a-Si). As indicated above, these differences in gouging can cause problems in later process steps. For example, these gouging differences can cause pitch-walking during subsequent wiring formation process
20 and/or cause other subsequent processing defects for the microelectronic workpieces being manufactured.

[0007] FIGS. 1A-1E (Prior Art) and FIGS. 2A-D (Prior Art) provide background information for prior solutions where undesired gouging occurs during SAMP processes such as during mandrel pull processes and/or during subsequent etch processes.

25 **[0008]** Looking first to FIGS. 1A-E (Prior Art), cross-section views are shown for an example where gouging occurs for prior solutions during an etch process (*e.g.*, dry etch) applied for a mandrel pull process where an organic dielectric layer (ODL) is used for the SAMP core material.

[0009] FIG. 1A (Prior Art) provides cross-section views of an example embodiment 100
30 where stacked layers have been formed on a substrate (not shown) including an anti-reflective layer 110, an ODL planarization layer 120, and a hard mask layer 130 (*e.g.*, SiN). In addition,

a photoresist layer 140 has been deposited and patterned, for example, using lithography and etch processes.

[0010] FIG. 1B (Prior Art) provides a cross-section view of an example embodiment 101 after the photoresist (PR) pattern is transferred to underlying layers above the hard mask layer 130. For example, one or more etch processes can be used to transfer the pattern formed in the PR layer 140 to underlying layers 110/120 and to form cores 150.

[0011] FIG. 1C (Prior Art) provides a cross-section view of an example embodiment 102 after a spacer material layer 155 has been deposited. As shown, the spacer material layer 155, such as an oxide layer, is deposited over the cores 150. The cores 150 still include the anti-reflective layer 110 and the ODL layer 120.

[0012] FIG. 1D (Prior Art) provides a cross-section view of an example embodiment 103 after an etch back process has been performed. For example, an etch back process is performed to etch back the spacer layer 155 and form spacers 160 along the side walls of the cores 150. This etch back process can also remove the anti-reflective layer 110 shown in FIG. 1C thereby leaving only the ODL layer 120 for the cores 150.

[0013] FIG. 1E (Prior Art) provides a cross-section view of an example embodiment 104 after a mandrel pull process has been performed. As shown, the mandrel pull process, such as an ash process, is used to remove the cores 150 shown in FIG. 1D. This mandrel pull process, however, introduces gouging 170 in the hard mask layer 130 where it is exposed in the gaps between the cores 150 and spacers 160 shown in FIG. 1D. This gouging 170 causes deterioration of etching uniformity in the etching process of subsequent patterns formed through the SAMP process.

[0014] FIGS. 2A-2C (Prior Art) provide cross-section views for an example where gouging occurs for prior solutions during an etch process (*e.g.*, dry etch) applied for a mandrel pull process where another material, such as amorphous silicon (a-Si), is used for the core material.

[0015] Looking first to FIG. 2A (Prior Art), an example embodiment 200 is shown where a spacer material layer 255, such as an oxide spacer layer, is deposited over cores 250 made from amorphous silicon. The cores 250 have been previously formed over a substrate (not shown), for example, using one or more patterning, etch, and deposition processes. The spacer material layer 255 and the cores 250 have been formed on a hard mask layer 230.

[0016] FIG. 2B (Prior Art) provides a cross-section view of an example embodiment 201 after an etch back process has been performed. For example, an etch back process is performed to etch back the spacer material layer 255 and form spacers 260 along the side walls of the cores 250. For example, an oxide etch back can be used where an oxide spacer material is
5 used.

[0017] FIG. 2C (Prior Art) provides a cross-section view of an example embodiment 202 after a mandrel pull process has been performed. As shown, the mandrel pull process, such as silicon etch process, is used to remove the a-Si cores 250 shown in FIG. 2B. This mandrel pull process, however, introduces gouging 270 in the hard mask layer 230 where it is exposed in
10 the gaps between the cores 250 and spacers 260 shown in FIG. 2B. This gouging 270 causes deterioration of etching uniformity in the etching process of subsequent patterns formed through the SAMP process.

SUMMARY

[0018] Embodiments are described herein to reduce gouging during multi-patterning
15 processes using thermal decomposition materials. For one embodiment, gouging is reduced or suppressed by using thermal decomposition materials as cores during multiple patterning processes. For one embodiment, gouging is reduced or suppressed by using thermal decomposition materials as a gap fill material during multiple patterning processes. By using thermal decomposition material as described herein, gouging of an underlying layer, such as a
20 hard mask layer, can be reduced or suppressed for patterned structures being formed using the self-aligned multi-patterning processes because more destructive etch processes, such as plasma etch processes, are not required to remove the thermal decomposition materials. Different or additional features, variations, and embodiments can also be implemented, and related systems and methods can be utilized as well.

25 **[0019]** For one embodiment, a method to improve etch uniformity for processing of microelectronic workpieces is disclosed including providing a substrate with a material layer, forming cores and spacers on the material layer with two spacers adjacent each core as part of a self-aligned multi-patterning (SAMP) process where the forming includes forming a layer of a thermal decomposition material, and removing the cores to leave the spacers where the
30 removing includes removing the thermal decomposition material with a thermal treatment.

[0020] In additional embodiments, the thermal treatment has a temperature range from 100 to 450 degrees Celsius. In further embodiments, the thermal treatment comprises an anneal process.

[0021] In additional embodiments, the thermal decomposition material has a depolymerizability characteristic such that it can be removed by thermal treatment of 100 to 450 degrees Celsius. In additional embodiments, the thermal decomposition material has a depolymerizability characteristic such that it can be removed by thermal treatment of 250 to 450 degrees Celsius and such that it is stable from 150 to 215 degrees Celsius.

[0022] In additional embodiments, a rate for the removing is controlled by adjusting at least one of temperature or pressure for a processing chamber within which substrate is being processed. In additional embodiments, the thermal decomposition material includes at least one of urethane, polymethyl methacrylate (PMMA), or a monomer.

[0023] In additional embodiments, the thermal decomposition material includes an ashing-less coating (ALC) material. In further embodiments, the ALC material includes a urea binding resin. In further embodiments, the urea binding resin includes polyurea having depolymerizability characteristics such that it can be removed by thermal treatment of less than 450 °C.

[0024] In additional embodiments, the layer of thermal decomposition material is used to form the cores. In further embodiments, the forming includes forming the layer of thermal decomposition material over the material layer, patterning the layer of thermal decomposition material to form the cores, depositing a spacer layer over the cores, and performing an etch back of the spacer layer to leave spacers as side wall structures adjacent the cores. In still further embodiments, the removing includes applying the thermal treatment to remove the cores of thermal decomposition material. Still further, the material layer can be a hard mask layer. In addition, a gouging target for the hard mask layer can be achieved.

[0025] In additional embodiments, the layer of thermal decomposition material is used as gap fill material for the removing. In further embodiments, the forming includes forming a core material layer over the material layer, patterning the core material layer to form cores on the material layer, depositing a spacer layer over the cores, and performing an etch back of the spacer layer to leave spacers as side wall structures adjacent the cores. In still further embodiments, the remove includes forming a layer of thermal decomposition material over the

cores and spacers, performing an etch back of the layer of thermal decomposition material using a thermal treatment to expose the cores and to leave the thermal decomposition material as the gap fill material between the cores and spacers, performing a mandrel pull process to remove the cores, and applying the thermal treatment to remove the cores of thermal decomposition material. Still further, the material layer can be a hard mask layer. In addition, a gouging target for the hard mask layer can be achieved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] A more complete understanding of the present inventions and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features. It is to be noted, however, that the accompanying drawings illustrate only exemplary embodiments of the disclosed concepts and are therefore not to be considered limiting of the scope, for the disclosed concepts may admit to other equally effective embodiments.

[0027] FIGS. 1A-1E (Prior Art) provides cross-section views for an example where gouging occurs for prior solutions during an etch process applied for a mandrel pull process where an organic dielectric layer is used for the SAMP core material.

[0028] FIGS. 2A-2C (Prior Art) provide cross-section views for an example where gouging occurs for prior solutions during an etch process applied for a mandrel pull process where another material, such as amorphous silicon, is used for the core material

[0029] FIGS. 3A-3E provide example cross-section views where a thermal decomposition material is used as the core material during multiple patterning processes according to reduce or eliminate the undesired gouging experienced in prior solutions.

[0030] FIGS. 4A-4E provide example cross-section views where a thermal decomposition material is used as a gap fill material during a multiple patterning process, such as a SAMP processes, to reduce or eliminate the undesired gouging experienced in prior solutions.

[0031] FIG. 5 provides a process diagram of an example embodiment where thermal decomposition materials are used in multiple patterning processes to reduce or suppress gouging in underlying layers.

[0032] FIGS. 6A-B provide diagrams for example thermal behaviors for representative thermal decomposition materials that can be used for the disclosed embodiments.

[0033] FIGS. 7 provides a diagram for thermal removal temperatures and heat resistance for example thermal decomposition materials that can be used for the disclosed embodiments.

DETAILED DESCRIPTION

[0034] Embodiments are disclosed that reduce gouging during multi-patterning processes for the manufacture of microelectronic workpieces. This reduction in gouging is achieved using thermal decomposition materials that can be removed through thermal treatment processes without requiring etch processes. Other advantages and implementations can also be achieved while still taking advantage of the process techniques described herein.

[0035] As described herein, thermal decomposition materials are used in multiple patterning processes so that gouging of underlying layers is reduced during the manufacture of microelectronic workpieces. The thermal decomposition materials are preferably materials that can be removed with a thermal treatment having a temperature range from 100 to 450 degrees Celsius (°C). For one embodiment, an ashing-less coating (ALC) material can be used as the thermal decomposition material, and this ALC material can be removed by thermal treatment using a de-polymerization temperature from 300°C to 400°C. Other thermal decomposition materials, such a urea binding resin, can also be used that have depolymerizability characteristics such that they can be removed by thermal treatment from 200°C to 240°C. Other thermal decomposition materials can also be used that can be removed using thermal treatments from 100°C to 450°C. More generally, thermal decomposition materials having depolymerizability characteristics such that they can be removed by thermal treatment from 100°C to 450°C are preferable for the embodiments described herein. These low temperature processes reduce gouging of underlying material layers in SAMP processes such as SADP and SAQP processes.

[0036] For one example, by using thermal decomposition material as a core material for a SAMP process, it is possible to remove the cores during a mandrel pull process by thermal treatment without using an etch process such as a plasma etch process (*e.g.*, RIE process) for the mandrel pull process. As such, exposed underlying layers (*e.g.*, hard mask layer) within gaps between cores are not gouged or otherwise affected by the plasma etch process. Gouging

is thereby suppressed in these exposed underlying layers, and the influence of defects caused by gouging, such as pitch walking, can be reduced or minimized.

[0037] As another example, by using thermal decomposition material to fill gaps between cores/spacers and thereby protect exposed underlying layers during a mandrel pull process, the
5 underlying layer within the gaps is protected during the etch process for the mandrel pull. As such, gouging is not introduced in these gap regions during the removal of cores made of other materials (*e.g.* a-Si). Further, because this thermal decomposition material can be removed by thermal treatment, an etch process is not necessary to remove the thermal decomposition material and gouging is further suppressed.

10 **[0038]** The disclosed embodiments provide one or more of the following features or advantages: (1) suppressing gouging by not using an ash process to remove organic layers, (2) replacing ODL/OPL with thermal decomposition materials, (3) using thermal decomposition materials for gap fill methods during mandrel pull processes, (4) reshaping spacers with no spacer profile change to suppress gouging, and/or (5) providing other features or advantages
15 based upon the use of thermal decomposition materials during SAMP processes.

[0039] Looking now to FIGS. 3A-E and FIGS. 4A-D, example embodiments are shown where thermal decomposition materials are used to reduce gouging experienced with prior solutions.

[0040] FIGS. 3A-E provide example cross-section views where a thermal decomposition
20 material is used as the core material during SAMP processes to reduce or eliminate the undesired gouging experienced in prior solutions such as shown in FIGS. 1A-E (Prior Art). For example, instead of an ODL or OPL layer as in prior solutions, a thermal composition material is formed as a material layer above a hard mask layer and patterned to form cores.

[0041] FIG. 3A provides cross-section view of an embodiment 300 where a thermal
25 decomposition material layer has been formed instead of the ODL or OPL layer to provide cores for a multiple patterning process such as a SAMP process. As shown, stacked layers have been formed on a substrate (not shown) including an anti-reflective layer 310, a thermal decomposition layer 320, and a hard mask layer 330 (*e.g.*, SiN). In addition, a photoresist layer 340 is deposited and patterned using lithography.

[0042] FIG. 3B provides a cross-section view of an example embodiment 301 after the pattern within the photoresist (PR) pattern is transferred to underlying layers including the thermal decomposition layer 320. For example, one or more etch processes can be used to transfer the pattern in the PR layer 340 to underlying layers and to form cores 350 within the underlying layers including the anti-reflective layer 310 and the thermal decomposition material 320.

[0043] FIG. 3C provides a cross-section view of an example embodiment 302 after a spacer material layer 355 has been deposited. As shown, the spacer material layer 355, such as an oxide layer, is deposited over the cores 350 that still include the anti-reflective layer 310 and the thermal decomposition material 320.

[0044] FIG. 3D provides a cross-section view of an example embodiment 303 after an etch back process has been performed. For example, an etch back process is performed to etch back the spacer material layer 355 shown in FIG. 3C and form spacers 360 along the side walls of the cores 350. Thus, after the spacer material layer 355 is formed and etched, the spacers 360 are left on side walls of cores 350. This etch back process can also remove the anti-reflective layer 310 shown in FIG. 3C thereby leaving only the thermal decomposition material 320 for the cores 350.

[0045] FIG. 3E provides a cross-section view of an example embodiment 304 after a mandrel pull process has been performed to remove the cores 350. Because the cores 350 are formed of the thermal decomposition material 320 as shown in FIG. 3D, the cores 350 can then be pulled by a thermal treatment such as a low temperature anneal (*e.g.*, from 100 to 450 degrees Celsius). As one example, the low temperature anneal can be performed using a heated plate. By carrying out thermal treatment after etch back to leave only the oxide spacers 360, the depolymerizable thermal decomposition material is removed without requiring an etch process which can lead to gouging. Because there is no need to perform subsequent etch processes for the mandrel pull, such as plasma etch processes (*e.g.*, RIE process), gouging in underlying layers within gap portions are reduced or suppressed. By using the thermal decomposition material 320 for the cores 350, a gouging target for the hard mask layer 330 is achieved.

[0046] FIGS. 4A-E provide example cross-section views where a thermal decomposition material is used as a gap fill material during a multiple patterning process, such as a SAMP

processes, to reduce or eliminate the undesired gouging experienced in prior solutions such as shown in FIGS. 2A-D (Prior Art).

[0047] FIG. 4A provides a cross-section view of an example embodiment 400 where a spacer material layer 455, such as a spacer material layer made from oxide (SiO_2), is deposited over cores 450 made from another material such as amorphous silicon. The cores 450 have been previously formed over a substrate (not shown), for example, using one or more patterning, etch, and deposition processes. As such, the spacer material layer 455 is formed over a core made of another material, such as a-Si, which has in turned been formed over a hard mask layer 430.

[0048] FIG. 4B provides a cross-section view of an example embodiment 401 after an etch back process has been performed on the spacer material layer 455 deposited on the cores 450. For example, an etch back process is performed to etch back the spacer material layer 455 and leave spacers 460 along the side walls of the cores 450. For example, an oxide etch back can be used where an oxide spacer material is used.

[0049] FIG. 4C provides a cross-section view of an example embodiment 402 after a thermal decomposition material 420 has been deposited over the cores 450 and spacers 460. For example, after spacer formation, a thermal decomposition material 420 is deposited to protect the gap portions between the cores 450 and spacers 460.

[0050] FIG. 4D provides a cross-section view of an example embodiment 403 after a mandrel pull process has been performed to remove the cores 450 shown in FIG. 4C. Gouging is not introduced in this process because the gap portions between the cores/spacers 450/460 are protected by the thermal decomposition material 420 during the mandrel pull process. For one embodiment, it is further noted that an etch back process can be performed prior to the mandrel pull process to remove a portion of the thermal decomposition material 420 and thereby expose the top surfaces of the cores 450. This etch back of the thermal decomposition material 420 can be achieved using a thermal treatment as described herein. A planarization process could also be used instead of and/or in addition to an etch back to expose the top surfaces of the cores 450.

[0051] FIG. 4E provides a cross-section view of an example embodiment 404 after the thermal decomposition material 420 has been removed using a thermal treatment as described herein. Because the thermal decomposition material 420 can be removed by a thermal

treatment, such as a low temperature anneal (*e.g.*, from 100 to 450 degrees Celsius), etch processes such as plasma etch processes (*e.g.* RIE process) are not needed. As such, gouging due to such plasma etch processes is further reduced or suppressed. Further, by using the thermal decomposition material 420 as the gap fill material, a gouging target for the hard mask
5 layer 430 is achieved.

[0052] FIG. 5 provides a process flow diagram for an example embodiment 500 where thermal decomposition materials are used in multiple patterning processes to reduce or suppress gouging in underlying layers and improve etch uniformity for processing of microelectronic workpieces. In block 502, a substrate is provided with a material layer. In
10 block 504, cores and spacers are formed on the material layer with two spacers adjacent each core as part of a self-aligned multi-patterning (SAMP) process. Further, the core/spacer formation includes forming a layer of a thermal decomposition material, for example, as a core material and/or as a gap fill material. In block 506, the cores are removed to leave the spacers. Further, the core removal includes removing the thermal decomposition material with a thermal
15 treatment. For example, the thermal treatment can be used to remove the cores where the thermal decomposition material is used as core material, and the thermal treatment can be used to remove gap fill material where the thermal decomposition material is used to fill gaps between cores/spacers. Additional and/or different process steps can also be used while still taking advantage of the techniques described herein.

20 **[0053]** FIGS. 6A and 6B provide diagrams for example thermal behaviors for a representative thermal decomposition material (*e.g.*, ALC material). In FIGS. 6A and 6B, thermal behavior is tested using a 400 nanometer (nm) layer of thermal decomposition material (*e.g.*, a 400 nm ALC layer) formed on silicon. This thermal decomposition layer on silicon is then annealed using a hot plater under a nitrogen gas. This thermal annealing is performed at
25 different temperature levels. After annealing, the removal of the thermal decomposition material layer is tested using FT-IR (Fourier transform infrared spectroscopy) to determine magnitudes (N) for different electromagnetic emissions based upon wavenumber (K) as shown in FIG. 6A. The removal rate is also tested under different pressures as shown in FIG. 6B.

[0054] Looking in more detail to FIG. 6A, a diagram 600 is provided that shows the
30 effectiveness of thermal treatments in removing the thermal decomposition material. In particular, thermal decomposition material (*e.g.*, ALC) formed on a substrate (*e.g.*, silicon substrate) is annealed at different temperature levels 606, 608, 610, 612, 614, and 616 (initial,

200°C, 250°C, 275°C , 300°C, 325°C), for example, using a hot plate anneal under a nitrogen (N_2) gas. The spectral peaks 602 and 604 indicate the presence of the thermal decomposition material, and the reduced magnitude levels for the progressively higher temperatures show that more of the thermal decomposition material is removed as the temperature of the anneal is
5 increased. The lack of peaks 602/604 in the FT-IR analysis for the temperature level 616 reveals that the ALC thermal decomposition material is effectively removed in this example for the 325°C thermal anneal.

[0055] FIG. 6B provides a diagram 650 that shows removal rates for thermal treatments of the thermal decomposition material under different pressures. For one thermal treatment test,
10 a pressure of 700 Torr was used. The line 652 represents a linear fit to measured removal rates at different temperatures for thermal anneals performed under this 700 Torr pressure. The removal rate is represented by percent change in thickness per min (Thickness Δ% / min). For another thermal treatment test, a pressure of 10 Torr or near vacuum was used. The line 654 represents a linear fit to measured removal rates at different temperatures for thermal anneals
15 performed under this 10 Torr pressure. As shown by the removing rate diagram 650, the temperature for the thermal treatment to remove the thermal decomposition material can be lowered by reducing the pressure as indicated by arrow 656. As also shown in the removing rate diagram 650, adjusting the temperature of the anneal process also adjusts the relative removal rate of percent change in thickness per minute of thermal treatment. More generally,
20 it is noted that these examples show that the rate for the removal of the thermal decomposition can be controlled by adjusting at least one of temperature or pressure for a processing chamber within which the substrate for a microelectronic workpiece is being processed.

[0056] FIG. 7 provides a diagram 700 of thermal removal temperatures and heat resistance for example thermal decomposition materials. The thermal removal temperature represents the
25 temperature at which a thermal treatment removes the thermal decomposition material, for example, by a degas process. The heat resistance represents the temperature level below which the thermal decomposition material remains stable and above which the decomposition material becomes unstable.

[0057] With respect to thermal removal, temperatures at which different thermal
30 decomposition materials are removed (*e.g.*, degas) are shown for ALC materials (*e.g.*, ALC, ALC-2) 702/704, urethane 706, polymethyl methacrylate (PMMA) 708, and monomers 710. As shown, these materials have thermal removal temperatures for thermal treatments from

100°C to 450°C. Other materials could also be used that have similar thermal removal characteristics while still taking advantage of the techniques described herein. For example, materials having depolymerizability characteristics such that they can be removed by thermal treatment of 100°C to 450°C can be used as a thermal decomposition material for the
5 techniques described herein.

[0058] With respect to thermal stability, temperatures at which the different thermal decomposition materials become unstable are also shown for ALC materials (*e.g.*, ALC, ALC-2) 702/704, urethane 706, polymethyl methacrylate (PMMA) 708, and monomers 710. It is noted for certain processes, such as where lithography anneal processes are used, it is desirable
10 for the thermal decomposition material to have thermal stability from 100°C to 215°C. For example, this thermal stability will allow the thermal decomposition material to resist depolymerization or removal through an etch back process for a silicon anti-reflective coating (SiARC). For such an embodiment where thermal stability is desired for lower temperatures, it is preferred to use materials having depolymerizability characteristics such that they can be
15 removed by thermal treatments from 250°C to 450°C and have thermal stability below this temperature range, for example, from 150°C to 215°C. As shown with respect to element 714, for example, the ALC material 702 meets these parameters as it has a thermal removal temperature of 350°C yet remains stable up to 250°C. Other variations could also be used for particular SAMP processes.

20 **[0059]** It is noted that the ALC and ALC-2 material can be materials such as urea binding resins (*e.g.*, polyurea) that have depolymerizability characteristics such that they can be removed by thermal treatment of less than 450 °C, and in another embodiment by thermal treatment of less than 300 °C. Through the application of thermal energy during the thermal treatment, the thermal decomposition material depolymerizes and is removed from the
25 substrate. As described herein, by using such thermal decomposition materials, as opposed to standard organic planarization or dielectric layers, gouging of underlying material layers during SAMP processes is reduced or eliminated.

[0060] The techniques described herein are not limited to a particular thermal decomposition material, as a variety of materials may be utilized while still obtaining the
30 benefits described herein. However, for one embodiment a urea binding resin, such as polyuria, is used that can be formed via a thin film deposition. An exemplary technique for the formation

of a polyurea and the removal of such a polyurea by a depolymerization process to decompose thermally the polyurea are described in more detail in U.S. Patent Application No. 15/654,307 filed July 19, 2017, entitled "Method of Fabricating Semiconductor Device, Vacuum Processing Apparatus and Substrate Processing Apparatus," to Yatsuda et al., the disclosure of which is expressly incorporated herein by reference in its entirety. The techniques described in U.S. Patent Application No. 15/654,307 include, but are not limited to, copolymerizing isocyanate and amine as raw material monomers to form a urea bond, for example, using a vapor deposition polymerization process. As described in U.S. Patent Application No. 15/654,307, a liquid process may also be used to form the polyurea. Further, as described, the polyurea may be subsequently depolymerized to an amine and vaporized by the application of a thermal treatment. It will be recognized, however, that other formation processes and other removal processes may be utilized while still gaining the benefits of the use of a thermal decomposition layer and thermal removal of such layer as described herein. Further, it will be recognized that the techniques described herein are not limited to polyurea and other materials and/or combinations or variants of polyurea and other materials may be utilized as the thermal decomposition material.

[0061] It is noted that one or more deposition processes can be used to form the material layers described herein. For example, one or more depositions can be implemented using chemical vapor deposition (CVD), plasma enhanced CVD (PECVD), physical vapor deposition (PVD), atomic layer deposition (ALD), and/or other deposition processes. For a plasma deposition process, a precursor gas mixture can be used including but not limited to hydrocarbons, fluorocarbons, or nitrogen containing hydrocarbons in combination with one or more dilution gases (*e.g.*, argon, nitrogen, *etc.*) at a variety of pressure, power, flow and temperature conditions. Lithography processes with respect to PR layers can be implemented using optical lithography, extreme ultra-violet (EUV) lithography, and/or other lithography processes. The etch processes can be implemented using plasma etch processes, discharge etch processes, and/or other desired etch processes. For example, plasma etch processes can be implemented using plasma containing fluorocarbons, oxygen, nitrogen, hydrogen, argon, and/or other gases. In addition, operating variables for process steps can be controlled to ensure that CD target parameters for vias are achieved during via formation. The operating variables may include, for example, the chamber temperature, chamber pressure, flowrates of gases, frequency and/or power applied to electrode assembly in the generation of plasma, and/or other

operating variables for the processing steps. Variations can also be implemented while still taking advantage of the techniques described herein.

[0062] It is noted that reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention, but do not denote that they are present in every embodiment. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, materials, or characteristics may be combined in any suitable manner in one or more embodiments. Various additional layers and/or structures may be included and/or described features may be omitted in other embodiments.

[0063] "Microelectronic workpiece" as used herein generically refers to the object being processed in accordance with the invention. The microelectronic workpiece may include any material portion or structure of a device, particularly a semiconductor or other electronics device, and may, for example, be a base substrate structure, such as a semiconductor substrate or a layer on or overlying a base substrate structure such as a thin film. Thus, workpiece is not intended to be limited to any particular base structure, underlying layer or overlying layer, patterned or unpatterned, but rather, is contemplated to include any such layer or base structure, and any combination of layers and/or base structures. The description below may reference particular types of substrates, but this is for illustrative purposes only and not limitation.

[0064] The term "substrate" as used herein means and includes a base material or construction upon which materials are formed. It will be appreciated that the substrate may include a single material, a plurality of layers of different materials, a layer or layers having regions of different materials or different structures in them, etc. These materials may include semiconductors, insulators, conductors, or combinations thereof. For example, the substrate may be a semiconductor substrate, a base semiconductor layer on a supporting structure, a metal electrode or a semiconductor substrate having one or more layers, structures or regions formed thereon. The substrate may be a conventional silicon substrate or other bulk substrate comprising a layer of semi-conductive material. As used herein, the term "bulk substrate" means and includes not only silicon wafers, but also silicon-on-insulator ("SOI") substrates, such as silicon-on-sapphire ("SOS") substrates and silicon-on-glass ("SOG") substrates, epitaxial layers of silicon on a base semiconductor foundation, and other semiconductor or

optoelectronic materials, such as silicon-germanium, germanium, gallium arsenide, gallium nitride, and indium phosphide. The substrate may be doped or undoped.

[0065] Systems and methods for processing a microelectronic workpiece are described in various embodiments. One skilled in the relevant art will recognize that the various embodiments may be practiced without one or more of the specific details, or with other replacement and/or additional methods, materials, or components. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of various embodiments of the invention. Similarly, for purposes of explanation, specific numbers, materials, and configurations are set forth in order to provide a thorough understanding of the invention. Nevertheless, the invention may be practiced without specific details. Furthermore, it is understood that the various embodiments shown in the figures are illustrative representations and are not necessarily drawn to scale.

[0066] Further modifications and alternative embodiments of the described systems and methods will be apparent to those skilled in the art in view of this description. It will be recognized, therefore, that the described systems and methods are not limited by these example arrangements. It is to be understood that the forms of the systems and methods herein shown and described are to be taken as example embodiments. Various changes may be made in the implementations. Thus, although the inventions are described herein with reference to specific embodiments, various modifications and changes can be made without departing from the scope of the present inventions. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and such modifications are intended to be included within the scope of the present inventions. Further, any benefits, advantages, or solutions to problems that are described herein with regard to specific embodiments are not intended to be construed as a critical, required, or essential feature or element of any or all the claims.

CLAIMS

What is claimed is:

1. A method to improve etch uniformity for processing of microelectronic workpieces, comprising:

providing a substrate with a material layer;

forming cores and spacers on the material layer with two spacers adjacent each core as part of a self-aligned multi-patterning (SAMP) process, the forming comprising forming a layer of a thermal decomposition material; and

removing the cores to leave the spacers, the removing including removing the thermal decomposition material with a thermal treatment.

2. The method of claim 1, wherein the thermal treatment has a temperature range from 100 to 450 degrees Celsius.

3. The method of claim 2, wherein the thermal treatment comprises an anneal process.

4. The method of claim 1, wherein the thermal decomposition material has a depolymerizability characteristic such that it can be removed by thermal treatment of 100 to 450 degrees Celsius.

5. The method of claim 1, wherein the thermal decomposition material has a depolymerizability characteristic such that it can be removed by thermal treatment of 250 to 450 degrees Celsius and such that it is stable from 150 to 215 degrees Celsius.

6. The method of claim 1, wherein a rate for the removing is controlled by adjusting at least one of temperature or pressure for a processing chamber within which substrate is being processed.

7. The method of claim 1, wherein the thermal decomposition material comprises at least one of urethane, polymethyl methacrylate (PMMA), or a monomer.

8. The method of claim 1, wherein the thermal decomposition material comprises an ashing-less coating (ALC) material.

9. The method of claim 8, wherein the ALC material comprises a urea binding resin.

10. The method of claim 9, wherein the urea binding resin comprises polyurea having depolymerizability characteristics such that it can be removed by thermal treatment of less than 450 °C.

11. The method of claim 1, wherein the layer of thermal decomposition material is used to form the cores.

12. The method of claim 11, the forming comprises:
forming the layer of thermal decomposition material over the material layer;
patterning the layer of thermal decomposition material to form the cores;
depositing a spacer layer over the cores; and
performing an etch back of the spacer layer to leave spacers as side wall structures adjacent the cores.

13. The method of claim 12, wherein the removing comprises applying the thermal treatment to remove the cores of thermal decomposition material.

14. The method of claim 13, wherein the material layer is a hard mask layer.

15. The method of claim 14, wherein a gouging target for the hard mask layer is achieved.

16. The method of claim 1, wherein the layer of thermal decomposition material is used as gap fill material for the removing.

17. The method of claim 16, wherein the forming comprises:
forming a core material layer over the material layer;
patterning the core material layer to form cores on the material layer;
depositing a spacer layer over the cores; and
performing an etch back of the spacer layer to leave spacers as side wall structures adjacent the cores.

18. The method of claim 17, wherein the removing comprises:
forming a layer of thermal decomposition material over the cores and spacers;
performing an etch back of the layer of thermal decomposition material using a thermal treatment to expose the cores and to leave the thermal decomposition material as the gap fill material between the cores and spacers;
performing a mandrel pull process to remove the cores; and
applying the thermal treatment to remove the cores of thermal decomposition material.

19. The method of claim 18, wherein the material layer is a hard mask layer.

20. The method of claim 19, wherein a gouging target for the hard mask layer is achieved.

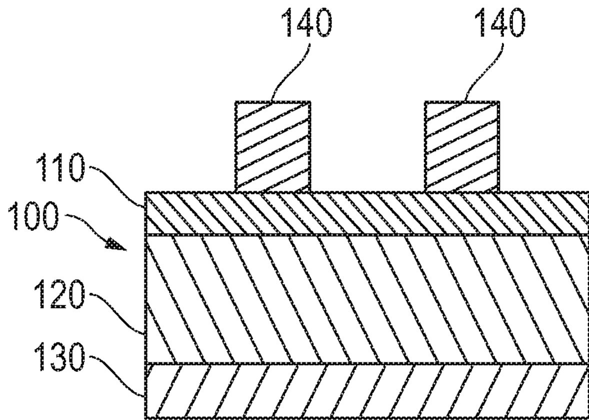


FIG. 1A
(Prior Art)

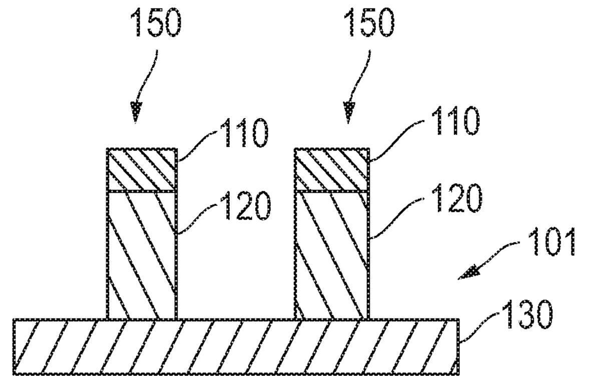


FIG. 1B
(Prior Art)

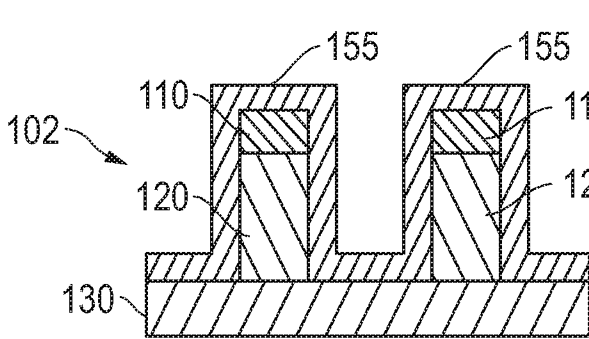


FIG. 1C
(Prior Art)

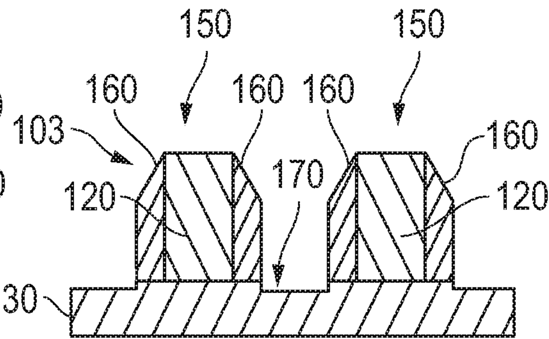


FIG. 1D
(Prior Art)

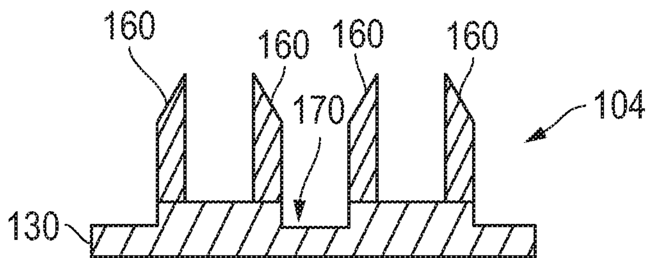


FIG. 1E
(Prior Art)

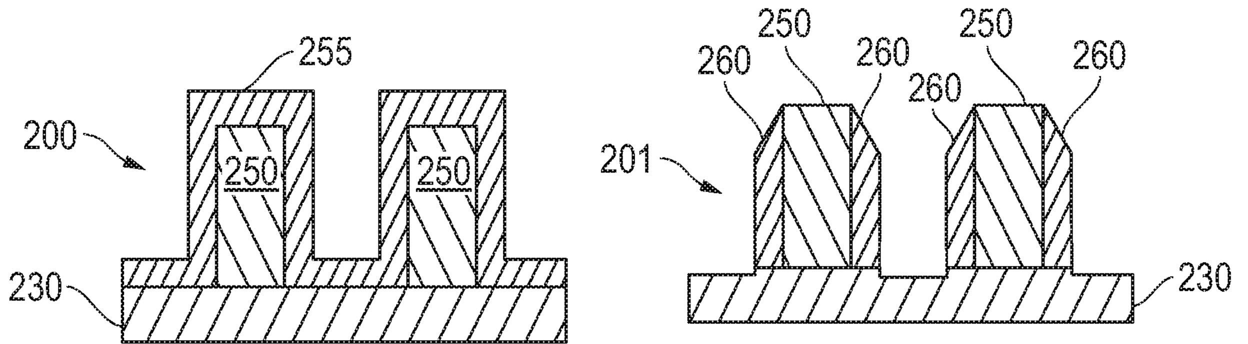


FIG. 2A
(Prior Art)

FIG. 2B
(Prior Art)

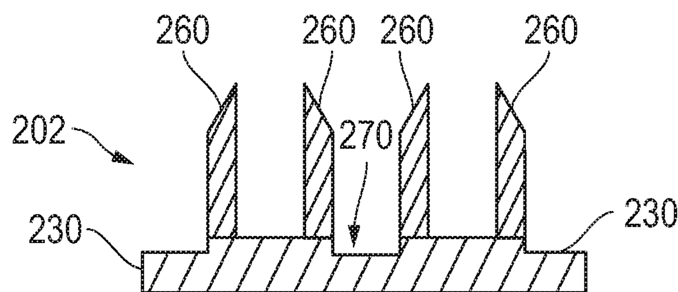


FIG. 2C
(Prior Art)

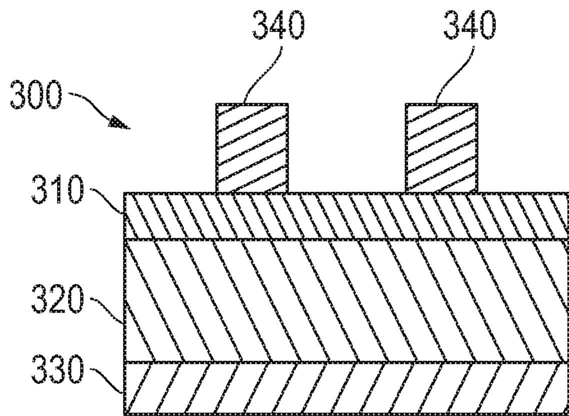


FIG. 3A

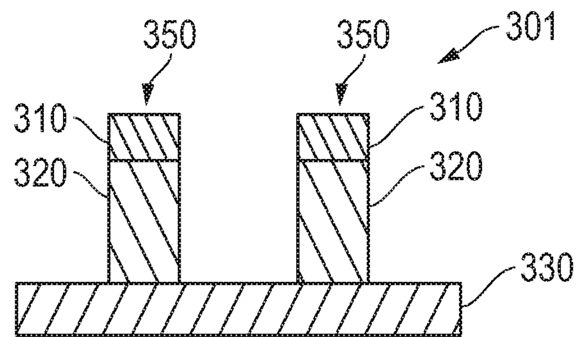


FIG. 3B

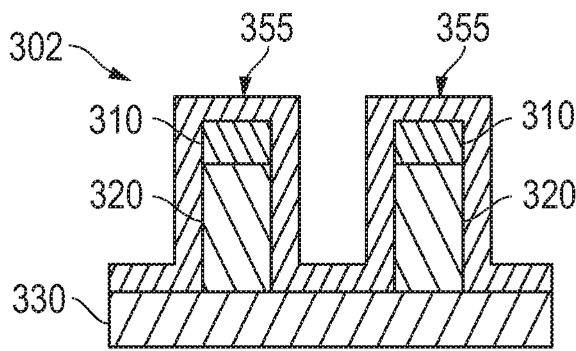


FIG. 3C

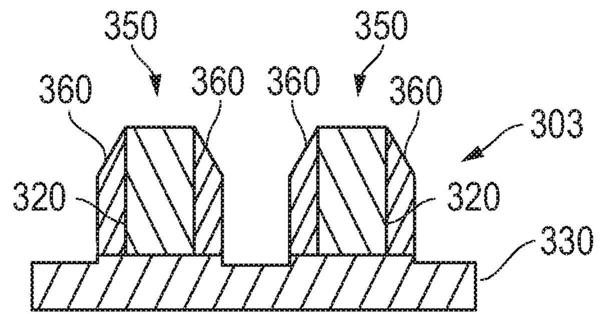


FIG. 3D

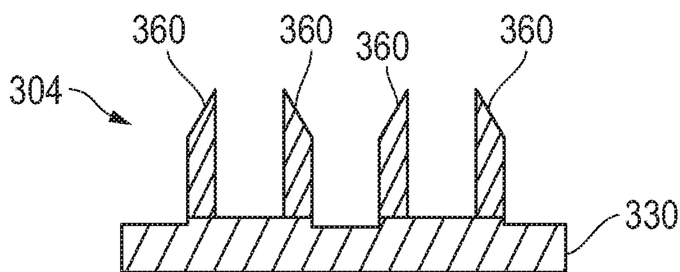


FIG. 3E

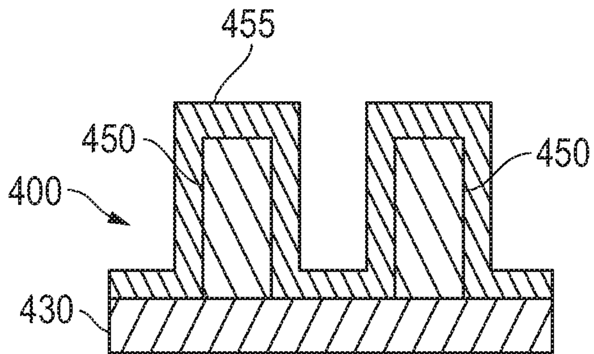


FIG. 4A

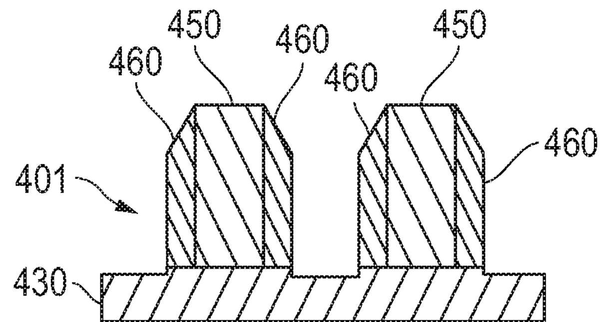


FIG. 4B

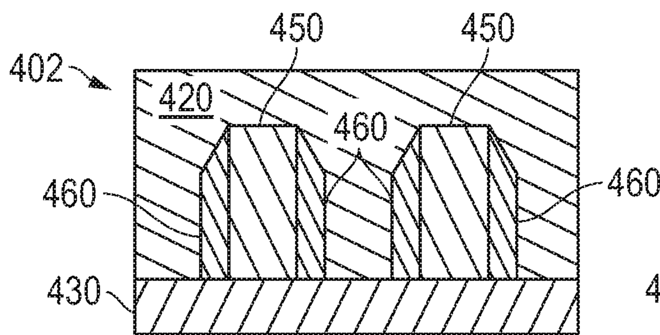


FIG. 4C

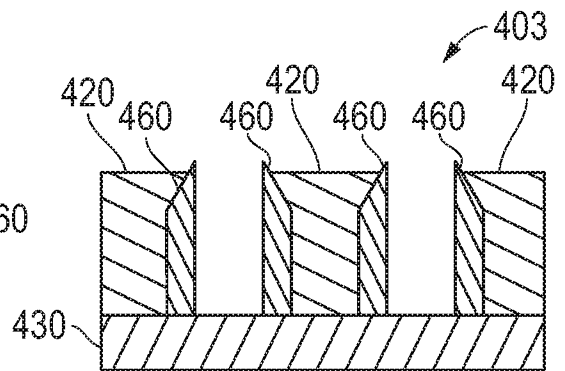


FIG. 4D

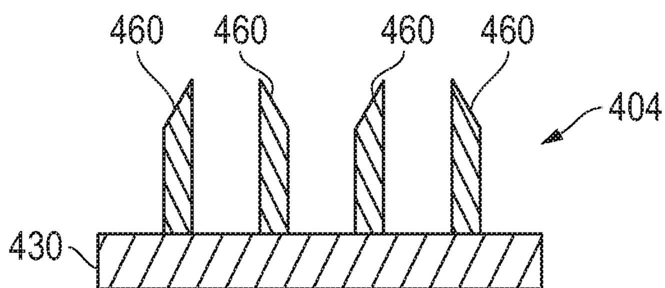


FIG. 4E

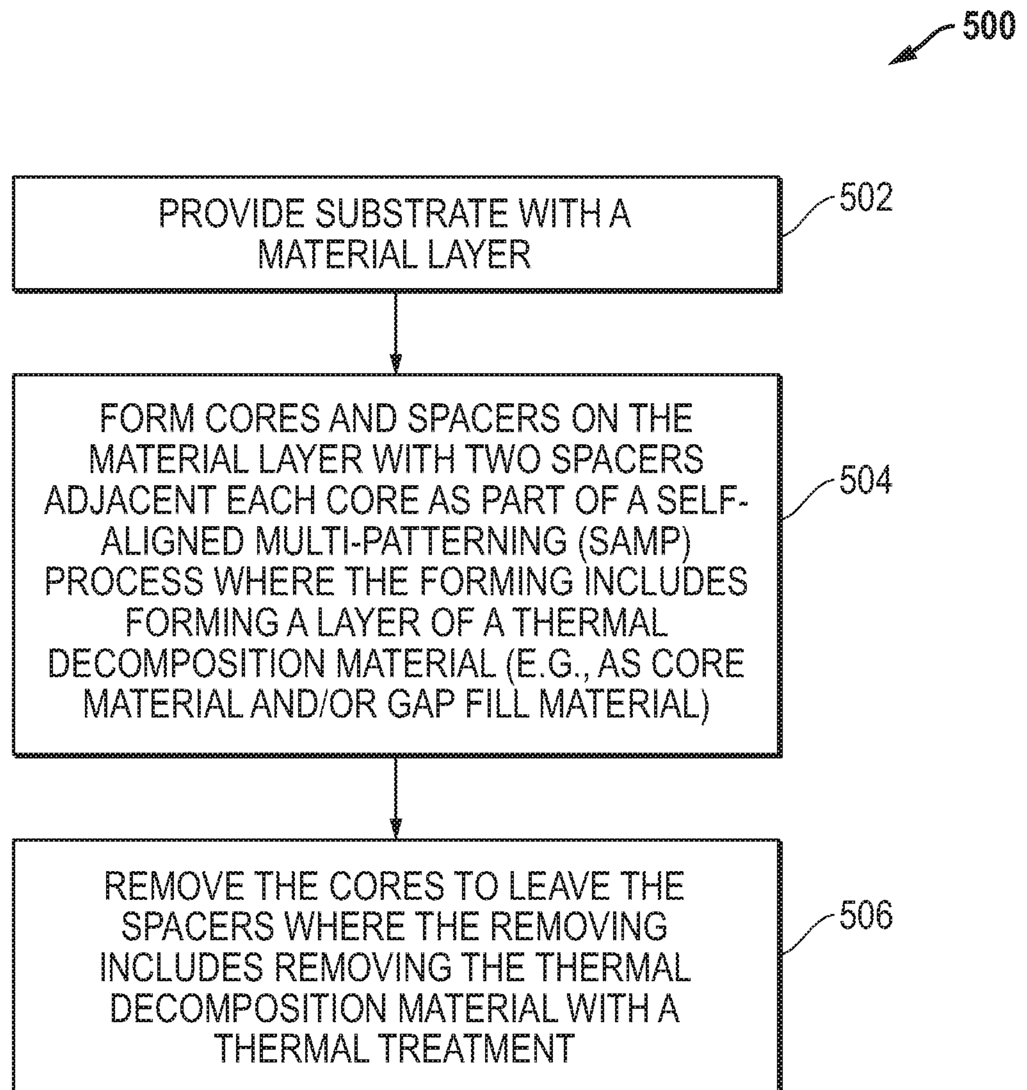


FIG. 5

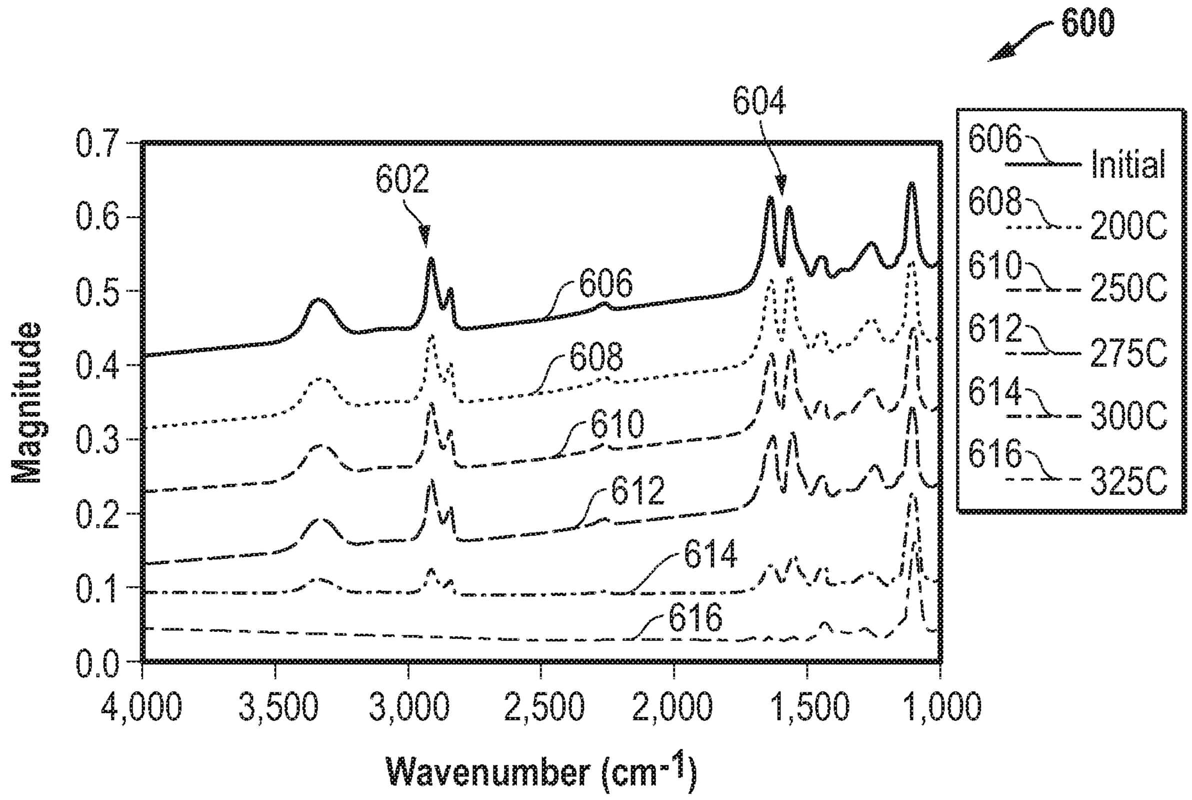


FIG. 6A

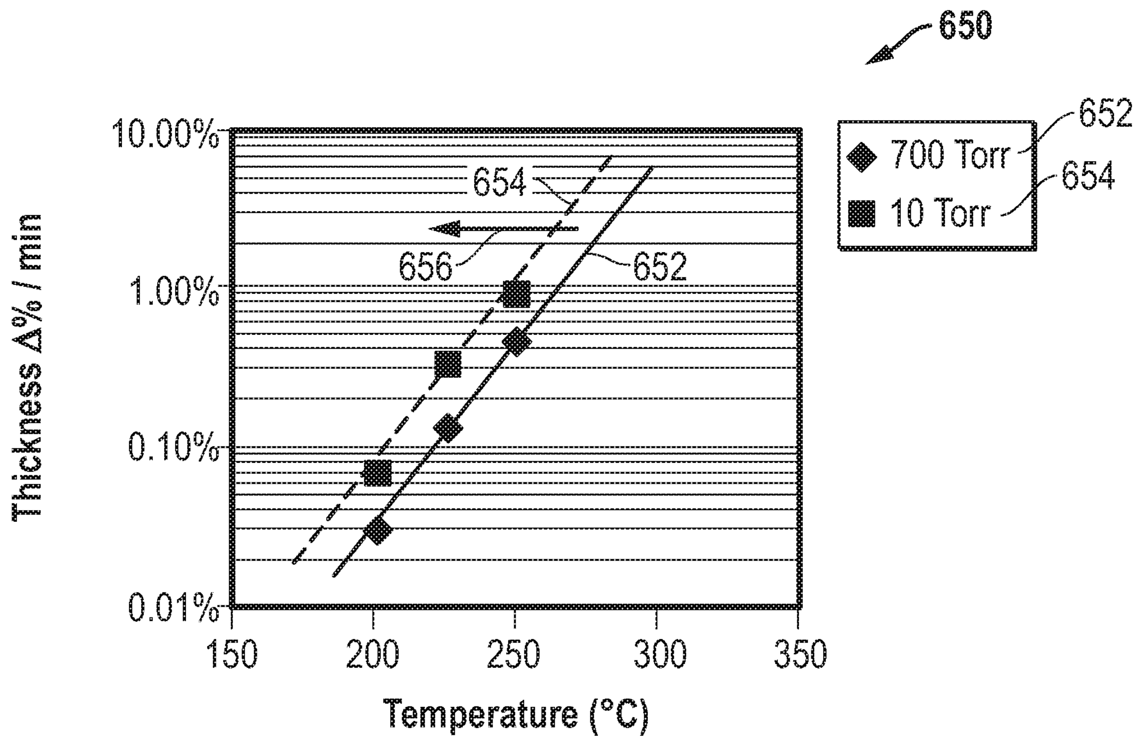


FIG. 6B

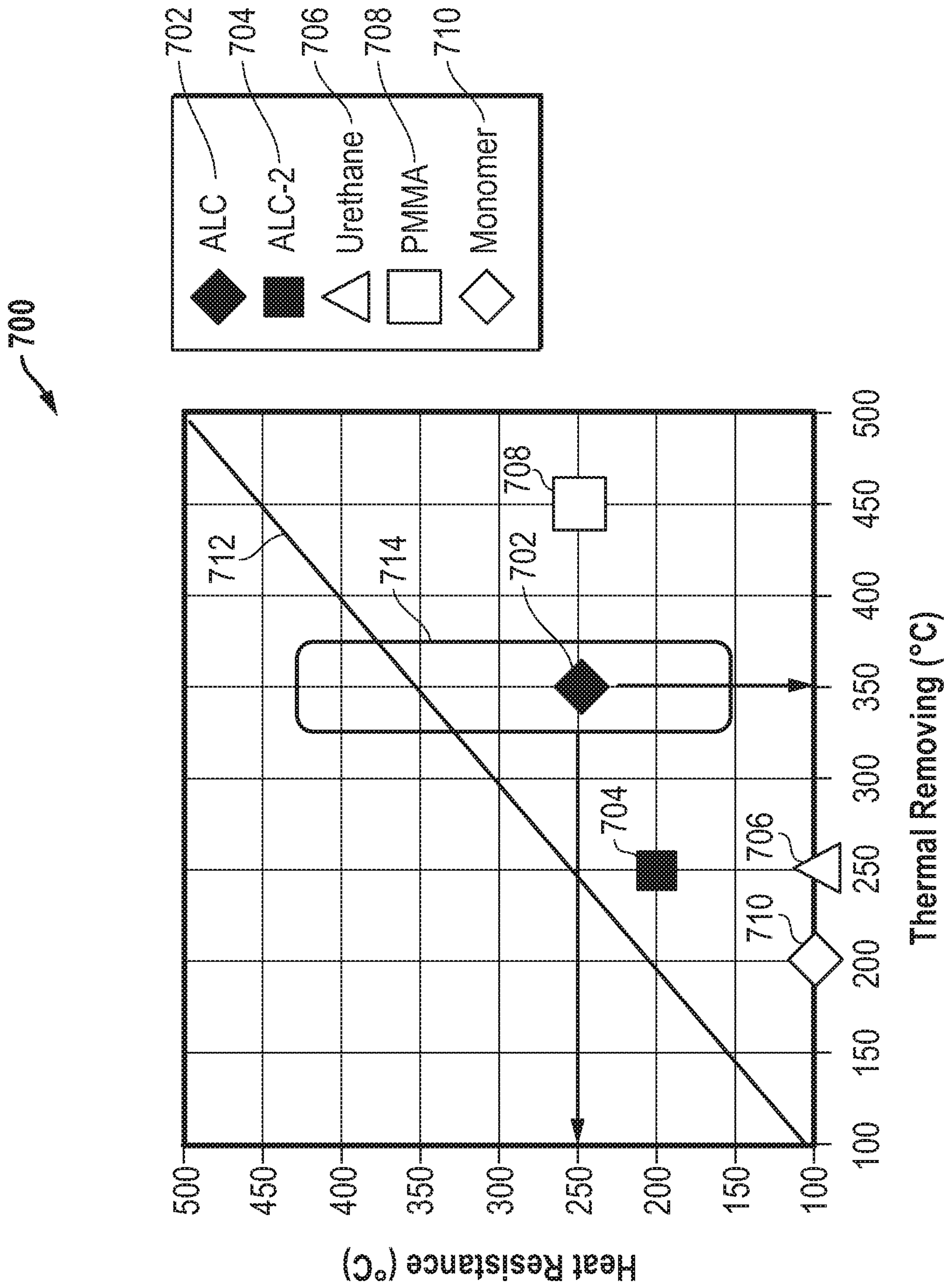


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/041193

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i, H01L 21/027(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; B05D 5/00; B05D 7/00; G21K 5/00; H01L 21/311; H01L 21/3213; H01L 21/428; H01L 21/027

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: SAMP(self-aligned multi-patterning), thermal-decomposition, gouging

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2008-0038467 A1 (RAMESH JAGANNATHAN et al.) 14 February 2008 See paragraphs 63-78; claims 1, 8; and figures 6a-6f.	1-20
Y	US 2008-0299774 A1 (GURTEJ SANDHU) 04 December 2008 See paragraphs 52-65; and figures 9-12.	1-20
Y	US 2009-0130863 A1 (DOREL I. TOMA et al.) 21 May 2009 See paragraphs 32-49; and figures 4A-4C.	2-10
A	US 2016-0225640 A1 (TOKYO ELECTRON LIMITED) 04 August 2016 See the entire document.	1-20
A	US 2018-0138078 A1 (TOKYO ELECTRON LIMITED) 17 May 2018 See the entire document.	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

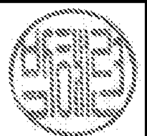
* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 October 2019 (30.10.2019)	**30 October 2019 (30.10.2019)**

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
PARK, Hye Lyun



Telephone No. +82-42-481-3463

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2019/041193

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008-0038467 A1	14/02/2008	CN 101174085 A	07/05/2008
		EP 1906237 A2	02/04/2008
		JP 2008-149447 A	03/07/2008
		KR 10-2008-0014715 A	14/02/2008
		TW 200821641 A	16/05/2008
US 2008-0299774 A1	04/12/2008	CN 101681812 A	24/03/2010
		CN 101681812 B	13/03/2013
		EP 2165355 A1	24/03/2010
		EP 2165355 B1	30/10/2013
		JP 2010-531051 A	16/09/2010
		JP 5110409 B2	26/12/2012
		KR 10-1547706 B1	26/08/2015
		KR 10-2010-0032397 A	25/03/2010
		TW 200908091 A	16/02/2009
		TW I360161 B	11/03/2012
		US 2011-0033786 A1	10/02/2011
		US 7923373 B2	12/04/2011
		WO 2008-150673 A1	11/12/2008
US 2009-0130863 A1	21/05/2009	CN 101828249 A	08/09/2010
		CN 101828249 B	23/05/2012
		JP 2011-503840 A	27/01/2011
		JP 5615180 B2	29/10/2014
		KR 10-2010-0074239 A	01/07/2010
		TW 200937575 A	01/09/2009
		TW I451528 B	01/09/2014
		US 7666754 B2	23/02/2010
		WO 2009-052117 A1	23/04/2009
US 2016-0225640 A1	04/08/2016	JP 2016-143890 A	08/08/2016
		KR 10-2016-0094893 A	10/08/2016
		TW 201642311 A	01/12/2016
		TW I596654 B	21/08/2017
		US 9673059 B2	06/06/2017
US 2018-0138078 A1	17/05/2018	TW 201830517 A	16/08/2018
		WO 2018-094071 A1	24/05/2018