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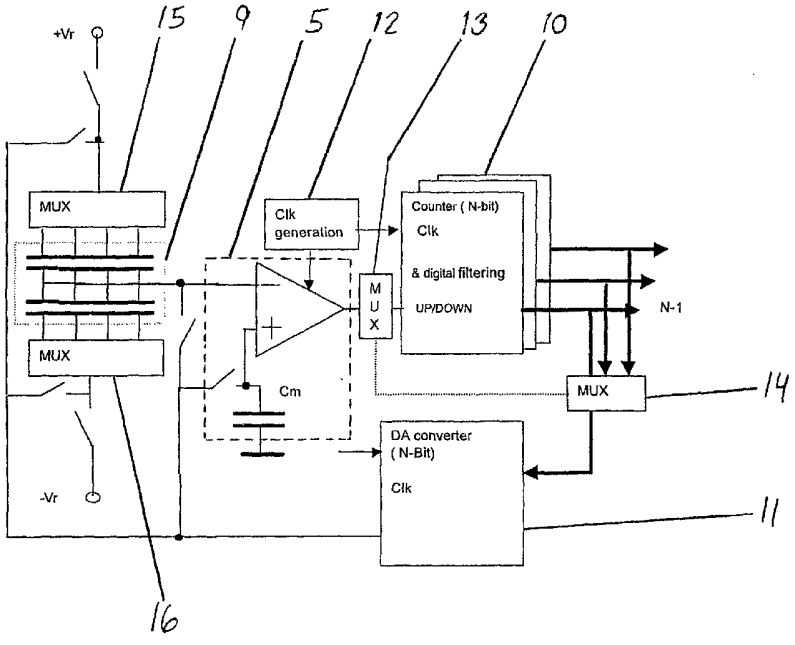
(54) **Title:** CAPACITIVE ACCELERATION SENSOR ARRANGEMENT



(57) **Abstract:** The present invention relates to measuring devices used in measuring acceleration, and, more specifically, to capacitive acceleration sensors. The improved sensor arrangement of the invention enables reliable and effective measuring of acceleration, in small capacitive acceleration sensor designs, in particular. The acceleration sensor arrangement measuring circuitry of the present invention can also be applied for multi-terminal sensors, such as, for example, acceleration sensors with three axes, by using time division signal multiplexing.

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Capacitive Acceleration Sensor Arrangement

Field of the Invention

The present invention relates to metering devices used in the measuring of acceleration and, more specifically, to capacitive acceleration sensors. The object of the invention is to provide an improved sensor arrangement, which enables reliable and effective measuring of acceleration, in particular in small capacitive acceleration sensor designs.

Background of the Invention

Measuring based on a capacitive acceleration sensor has proved to have a simple principle and to provide a reliable method in the measuring of acceleration. The capacitive measuring is based on a change in the gap between two surfaces of a pair of electrodes of the sensor. The capacitance between the surfaces, i.e. the capacity for storing electric charge, depends on the area of the surfaces and on the distance between the surfaces. Capacitive measuring can be used already at rather low measuring ranges of acceleration.

The measuring principle of the capacitive sensor essentially affects the precision of measurement of the sensor. One optimal method of measuring for a capacitive acceleration sensor is, in fact, to measure the sensor such, that the charge across the electrodes to be measured remains equal, whereby the electrostatic forces caused by the charge compensate each other and the error of measurement caused by them will be minimized.

Prior art will be described below with exemplifying reference to the appended drawing, in which:

Figure 1 shows a measuring circuitry of an acceleration sensor arrangement according to prior art.

Figure 1 shows a measuring circuitry of an acceleration sensor arrangement according to prior art. The measuring circuitry of the acceleration sensor arrangement according to prior art comprises a measured sensor 1, i.e. pairs of electrodes, a charge amplifier 2, an analog integrator 3 and a feedback connection 4.

In the measuring circuitry of an acceleration sensor arrangement according to prior art, the charge amplifier 2 detects the potential difference, which exists between the output signal Vm from the analog integrator 3 and the central electrode of the sensor 1, and transforms the charge, which, due to the potential difference, flows to the amplifier 2 into a voltage. The received voltage is integrated by the analog integrator 3, until a state is reached, where the output signal Vm represents an ideal voltage distribution. Thus, the circuit is in state, where there is a balance of charge ($Q_{C1}=Q_{C2}$) between the terminals of the capacitors C1 and C2 of the measured sensor 1.

The measuring circuitry of an acceleration sensor, according to prior art, transforms, out of the value of the capacitances C1 and C2 of the sensor, an analog voltage Vm = Vr * (C1-C2)/(C1+C2), which is proportional to the reference voltage Vr in use, and which has a very linear response in the utilized acceleration sensors.

The problems in the acceleration sensor measuring circuitry according to prior art are the offset errors in the analog integrator, which always, however, affect the functioning of the circuit. In addition, the analog integrator is sensitive to interference, in a multiplexed application, in particular.

There is also a problem in the acceleration sensor measuring circuitry according to prior art concerning the charge amplifier in a need for a large uniform range of operation because of the variation in sensor capacitances, and also, in the multiplexed case, a need for a large bandwidth, which presents a challenge for the design of the charge amplifiers and tends to increase the power consumption in the prestage.

Summary of the Invention

The object of the present invention is to provide an improved sensor arrangement, such that advantages of symmetry are achieved, and which arrangement enables reliable and effective measuring of acceleration, in particular in small capacitive acceleration sensor designs.

According to a first feature of the present invention there is provided a capacitive acceleration sensor arrangement, the arrangement comprising at least one measured pair of electrodes for the capacitive measuring of acceleration, such that the arrangement further comprises

- a digital comparator,
- a digital integrator,
- a D/A converter positioned in a feedback branch connection between the output from the digital integrator and the digital comparator, and
- a clock signal generator,

such, that the digital comparator detects the voltage difference between the output signal from the digital integrator, which signal has been converted into analog form in the D/A converter, and the central electrode of the measured pair of electrodes, and converts the difference in potential into a corresponding digital signal, and that the digital signal representing the difference in potential received from the digital comparator is added in the digital integrator, from which digital integrator a digital output signal is obtained as an output.

Preferably, the digital output signal output from the digital integrator is directed towards a state, where a balance of charge exists between the terminals of the capacitors of the measured pair of electrodes. Preferably, the digital integrator is implemented by means of an up-down counter. Alternatively, the digital integrator is implemented by means of digital counter logic. Further, preferably, the digital counter logic, in addition to controlling the digital integrator, also controls the D/A converter.

Preferably, the clocking from the clock signal generator is adapted to provide a suitable measuring function. Preferably, at the input, instead of the digital comparator, a combination of a charge amplifier and a comparator is being used. Preferably, there is an A/D conversion combined with the analog measuring function of the pair of electrodes to be measured. Preferably, further calibration of the pair of electrodes to be measured is performed digitally.

According to a second feature of the present invention there is provided a capacitive acceleration sensor arrangement, said arrangement comprising a set of pairs of electrodes to

be measured for capacitive measuring of acceleration, such, that the arrangement further comprises

- a digital comparator,
- a set of digital integrators,
- a set of time division multiplexors,
- control logic for the multiplexors,
- a D/A converter positioned in a feedback branch connection between the output from the digital integrators via the multiplexor and the digital comparator, and
- a clock signal generator,

such, that the digital comparator detects the voltage difference between the output signal from the digital integrators via the multiplexor, which signal has been converted into analog form in the D/A converter, and the central electrode of the measured pairs of electrodes, and converts the differences in potential into corresponding digital signals, and that the voltage representing each sensor, converted by the digital comparator, is added in the digital integrator, from which digital integrator a digital output signal is obtained as an output.

Preferably, time division multiplexing is used in the measuring, such that, using time division by means of the multiplexor, during one time slot the measuring of one sensor is performed and, correspondingly, the measuring of each consecutive sensor is performed during each subsequent time slot. Preferably, the digital output signal output from the digital integrator is directed towards a state, where a balance of charge exists between the terminals of the capacitors of the measured pair of electrodes for each sensor.

Preferably, the digital integrator is implemented by means of an up-down counter. Alternatively, the digital integrator is implemented by means of digital counter logic. Further, preferably, the digital counter logic, in addition to controlling the digital integrator, also controls the D/A converter.

Preferably, the clocking from the clock signal generator is adapted to provide a suitable measuring function. Preferably, at the input, instead of the digital comparator, a combination of a charge amplifier and a comparator is being used. Preferably, an A/D conversion is combined with the analog measuring functions of the pairs of electrodes to be measured. Preferably, further calibration of the pairs of electrodes to be measured is performed digitally.

The digital integrators are, preferably, implemented by means of sub-micron CMOS technology. Preferably, the circuitry is adapted to function at very low voltages, below 2.0 volts. Preferably, the sensitivity variations in connection with the processing of the pairs of electrodes to be measured are calibrated by adjusting the transfer function of the D/A converter.

Preferably, the digital output signal directly consists of the outputs of the digital integrators, which outputs are transferred to further processing as a signal in parallel form. Alternatively, the digital output signal directly consists of the outputs of the digital integrators, which outputs are transferred to further processing as a signal in serial form.

Preferably, the power consumption of the D/A converter is adapted to a low level by means of CMOS technology and SC circuit technique. Preferably, the arrangement is adapted for sensors with multiple terminals. Alternatively, the arrangement is adapted for an acceleration sensor with three axes.

Preferably, the arrangement further comprises circuit elements, by means of which parasitic capacitances are eliminated. Alternatively, the arrangement further comprises circuit elements, by means of which non-idealities are eliminated.

Brief Description of the Drawings

The present invention and its preferable embodiments will be described in detail below, with exemplifying reference to the accompanying drawings, of which:

Figure 1 shows a measuring circuitry of an acceleration sensor arrangement according to prior art,

Figure 2 shows a measuring circuitry of an acceleration sensor arrangement according to the present invention,

Figure 3 shows a measuring circuitry of an alternative acceleration sensor arrangement according to the present invention.

Figure 1 has been described above. Below, the present invention and preferable embodiments thereof will be described with reference to Figures 2-3.

Detailed Description of the Invention

Figure 2 shows a measuring circuitry of an acceleration sensor arrangement according to the present invention. The acceleration sensor arrangement measuring circuitry according to the present invention comprises a sensor 1 to be measured, i.e. pairs of electrodes, a digital comparator 5, a digital integrator 6, a clock signal generator 8 and a D/A converter 7 positioned in a feedback branch connection.

The digital comparator 5 in the acceleration sensor arrangement measuring circuitry according to the present invention detects the voltage difference existing between the output signal from the digital integrator 6 converted into analog form in the D/A converter 7 and the central electrode of the sensor 1, and converts the difference in potential into a corresponding digital signal.

The digital signal corresponding to the difference in potential obtained from the digital comparator 5 is added in the digital integrator 6, from which a digital output signal is received as output. The digital output signal from the digital integrator 6 is directed towards a state, where there is a balance of charge ($Q_{C1}=Q_{C2}$) between the terminals of the capacitors C1 and C2 of the measured sensor 1.

The digital integrator 6 can be implemented by, for instance, an up-down counter or by digital counter logic. In addition to the digital integrator 6, also the D/A converter 7 can be controlled by means of the digital counter logic.

The D/A converter 7 positioned in a feedback branch connection has been added to the acceleration sensor

measuring circuitry according to the present invention, which converter manages the necessary feedback to the comparator circuit 5. By the use of suitable clocking by means of the clock signal generator 8, a circuitry implementing a suitable measuring function is achieved. Alternatively, at the input, instead of the digital comparator 5, a combination of a charge amplifier and a comparator may be used.

By means of the solution according to the present invention, the signal will be converted into digital form. In the solution, the digital conversion is combined with the analog sensor measuring function, whereby a digital signal is provided as the output signal of the sensor. In the solution according to the present invention, further calibration of the sensor may thus be performed digitally immediately, and no separate A/D converter is required.

Figure 3 shows an alternative measuring circuitry of an acceleration sensor arrangement according to the present invention. The alternative acceleration sensor arrangement measuring circuitry according to the present invention comprises a set of sensors 9 to be measured, i.e. multiple pairs of electrodes, a digital comparator 5, a set of digital integrators 10, a clock signal generator 12, a D/A converter 11 positioned in a feedback branch connection, and time division multiplexors 13-16 and control logic for the multiplexors 13-16.

The measuring by the alternative measuring circuitry of an acceleration sensor according to the present solution is adapted for multi-terminal sensors using time division signal multiplexing. The measuring circuitry comprises the multiplexors 13-16, by means of which, taking turns, the

measuring of one sensor at a time is performed in one time slot, and the measuring of the next sensor, correspondingly, is performed during the following time slot, etc.

In the alternative acceleration sensor measuring circuitry according to the present solution, the digital comparator 5 detects the voltage differences, received from the sensors 9 to be measured, between the output signal from the digital integrators 10 via the multiplexor, converted into analog form in the D/A converter 11, and the central electrodes of the sensors 9, and converts the differences in potential into corresponding digital signals.

The voltage representing each sensor, converted by the digital comparator 5, is added in the digital integrator 10, from which a digital output signal is obtained as an output. The digital output signal output from the digital integrator 10 is directed towards a state, where a balance of charge ($Q_{C1}=Q_{C2}$) exists between the terminals of the capacitors C1 and C2 of each measured sensor 9.

The digital integrator 10 can be implemented, for example, by an up-down counter or by digital counter logic. In addition to the digital integrator 10, also the D/A converter 11 can be controlled by means of the digital counter logic.

The D/A converter 11 positioned in a feedback branch connection has been added to the acceleration sensor measuring circuitry according to the present invention, which converter manages the necessary feedback to the comparator circuit 5. By the use of suitable clocking by means of the clock signal generator 12, a circuitry implementing an appropriate measuring function is achieved. Alternatively, at

the input, instead of the digital comparator 5, a combination of a charge amplifier and a comparator may be used.

By means of the solution according to the present invention, the signal of each sensor will separately be converted into digital form. In the solution, the digital conversion is combined with the analog measuring functions for the sensors 9, whereby digital signals are provided as the output signals of the sensors 9. In the solution according to the present invention, further calibration of the sensors may thus be performed digitally immediately, and no separate A/D converters are required.

An advantage of the acceleration sensor measuring circuitry according to the present solution is the replacement of an analog integrator with a digital integrator, whereby the function of the circuit is unaffected by offset errors in the analog integrator. The integrators are also less sensitive to interference, in particular in the multiplexed application. The integrators can be implemented by means of modern sub-micron CMOS technology. The circuitry can also be designed to work at extremely low voltages, below 2.0 volts.

Sensitivity variations in connection with the processing of the sensor element can be calibrated away by adjusting the transfer function of the D/A converter. The digital output signal of the circuit is directly the output of the integrator, which can be transferred for further processing as a signal in either parallel or serial form. The power consumption of the D/A converter can achieve a very low level by means of CMOS technology (CMOS, Complementary Metal Oxide Semiconductor) by using the SC circuit technique (SC, Switched Capacitor).

A further advantage of the circuitry is the replacement of a charge amplifier by a fast comparator. The problem with a charge amplifier is the need for a large uniform range of operation because of the variation in sensor capacitances, as well as, in the multiplexing environment, a need for a wide bandwidth, which makes designing the charge amplifier a challenge and tends to increase the power consumption of the prestage. These problems largely disappear by means of a fast comparator.

The acceleration sensor arrangement measuring circuitry according to the present solution can also be applied to multi-terminal sensors such as, for example, an acceleration sensor with three axes, using time division multiplexing of the signal. The acceleration sensor measuring circuitry according to the present solution can also be developed further to higher precision, i.a, by adding circuit elements to the circuitry, by means of which parasitic capacitances and other non-idealities will be eliminated.

Patent Claims

1. A capacitive acceleration sensor arrangement, which arrangement comprises at least one pair of electrodes (1) to be measured for the capacitive measuring of acceleration, **characterized** in that the arrangement further comprises
- a digital comparator (5),
- a digital integrator (6),
- a D/A converter (7) positioned in a feedback branch between the output from the digital integrator (6) and the digital comparator (5), and
- a clock signal generator (8),

such, that
- the digital comparator (5) detects the voltage difference between the output signal from the digital integrator (6), converted into analog form in the D/A converter (7), and the central electrode of the pair of electrodes (1) to be measured, and converts the difference in potential into a corresponding digital signal,

and, that
- the digital signal corresponding to the difference in potential obtained from the digital comparator (5) is added in the digital integrator (6), from which digital integrator (6) a digital output signal is obtained as output.

2. The capacitive acceleration sensor arrangement according to Claim 1, **characterized** in that the digital output signal from the digital integrator (6) is directed towards a state, where a balance of charge prevails between the terminals of the capacitors in the pair of electrodes (1) to be measured.

3. The capacitive acceleration sensor arrangement according to Claim 1 or 2, **characterized** in that the digital integrator (6) is implemented by means of an up-down counter.

4. The capacitive acceleration sensor arrangement according to Claim 1 or 2, **characterized** in that the digital integrator (6) is implemented by means of digital counter logic.

5. The capacitive acceleration sensor arrangement according to Claim 4, **characterized** in that the digital counter logic, in addition to the digital integrator (6), also controls the D/A converter (7).

6. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 1-5, **characterized** in that the clocking of the clock signal generator (8) is adapted for achieving a suitable measuring function.

7. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 1-6, **characterized** in that, at the input, instead of the digital comparator (5), a combination of a charge amplifier and a comparator is being used.

8. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 1-7, **characterized** in that an A/D conversion is combined with a function for analog measuring of the pair of electrodes (1) to be measured.

9. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 1-8, **characterized** in that further calibration of the pair of electrodes (1) to be measured is performed digitally.

10. A capacitive acceleration sensor arrangement, which arrangement comprises a set of pairs of electrodes (9) to be measured for the capacitive measuring of acceleration, **characterized** in that the arrangement further comprises

- a digital comparator (5),
- a set of digital integrators (10),
- a set of time division multiplexors (13-16),
- control logic for the multiplexors (13-16),
- a D/A converter (11) positioned in a feedback branch between the output from the digital integrators (10) via the multiplexor (14) and the digital comparator (5), and
- a clock signal generator (12),

such, that

- the digital comparator (5) detects the voltage difference between the output signal from the digital integrators (10) via the multiplexor (14), converted into analog form in the D/A converter (11), and the central electrode of the pairs of electrodes (9) to be measured, and converts the differences in potential into corresponding digital signals,

and, that

- the voltage corresponding to each sensor, converted by the digital comparator (5), is added in the digital integrator (10), from which digital integrator (10) a digital output signal is obtained as output.

11. The capacitive acceleration sensor arrangement according to Claim 10, **characterized** in that time division signal multiplexing is being used such, that measuring one sensor at a time is performed in a time slot by taking turns using time division by means of the multiplexors (13-16) and, correspondingly, measuring each one of the following sensors is performed in each of the subsequent time slots.

12. The capacitive acceleration sensor arrangement according to Claim 10 or 11, **characterized** in that the digital output signal from the digital integrator (10) is directed towards a state, where a balance of charge prevails between the terminals of the capacitors in the pair of electrodes (9) to be measured for each sensor.

13. The capacitive acceleration sensor arrangement according to any one of the Claims 10-12, **characterized** in that the digital integrator (10) is implemented by means of an up-down counter.

14. The capacitive acceleration sensor arrangement according to anyone of the Claims 10-12, **characterized** in that the digital integrator (10) is implemented by means of digital counter logic.

15. The capacitive acceleration sensor arrangement according to Claim 14, **characterized** in that the digital counter logic, in addition to the digital integrator (10), also controls the D/A converter (11).

16. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-15, **characterized** in that the clocking of the clock signal generator (12) is adapted for achieving a suitable measuring function.

17. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-16, **characterized** in that, at the input, instead of the digital comparator (5), a combination of a charge amplifier and a comparator is being used.

18. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-17, **characterized** in that the A/D conversion is combined with functions for analog measuring of the pairs of electrodes (9) to be measured.

19. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-18, **characterized** in that further calibration of the pairs of electrodes (9) to be measured is performed digitally.

20. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-19, **characterized** in that the digital integrators (10) are implemented by means of sub-micron CMOS technology.

21. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-20, **characterized** in that the circuitry is adapted to work at extremely low voltages, below 2.0 volts.

22. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-21, **characterized** in that the variations in sensitivity associated with the processing of the pairs of electrodes (9) to be measured are calibrated by adjusting the transfer function of the D/A converter (11).

23. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-22, **characterized** in that the outputs of the digital integrators (10) directly constitute a digital output signal, which is transferred to further processing as a signal in parallel form.

24. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-22, **characterized** in that the outputs of the digital integrators (10) directly constitute a digital output signal, which is transferred to further processing as a signal in serial form.

25. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-24, **characterized** in that the power consumption of the D/A converter is adapted for a low level by means of CMOS technology an SC circuit technique.

26. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-25, **characterized** in that the arrangement is adapted for multi-terminal sensors.

27.The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-25, **characterized** in that the arrangement is adapted for acceleration sensors with three axes.

28. The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-27, **characterized** in that the arrangement further comprises circuit elements, by means of which parasitic capacitances are eliminated.

29.The capacitive acceleration sensor arrangement according to any one of the preceding Claims 10-27, **characterized** in that the arrangement further comprises circuit elements, by means of which non-idealities are eliminated.

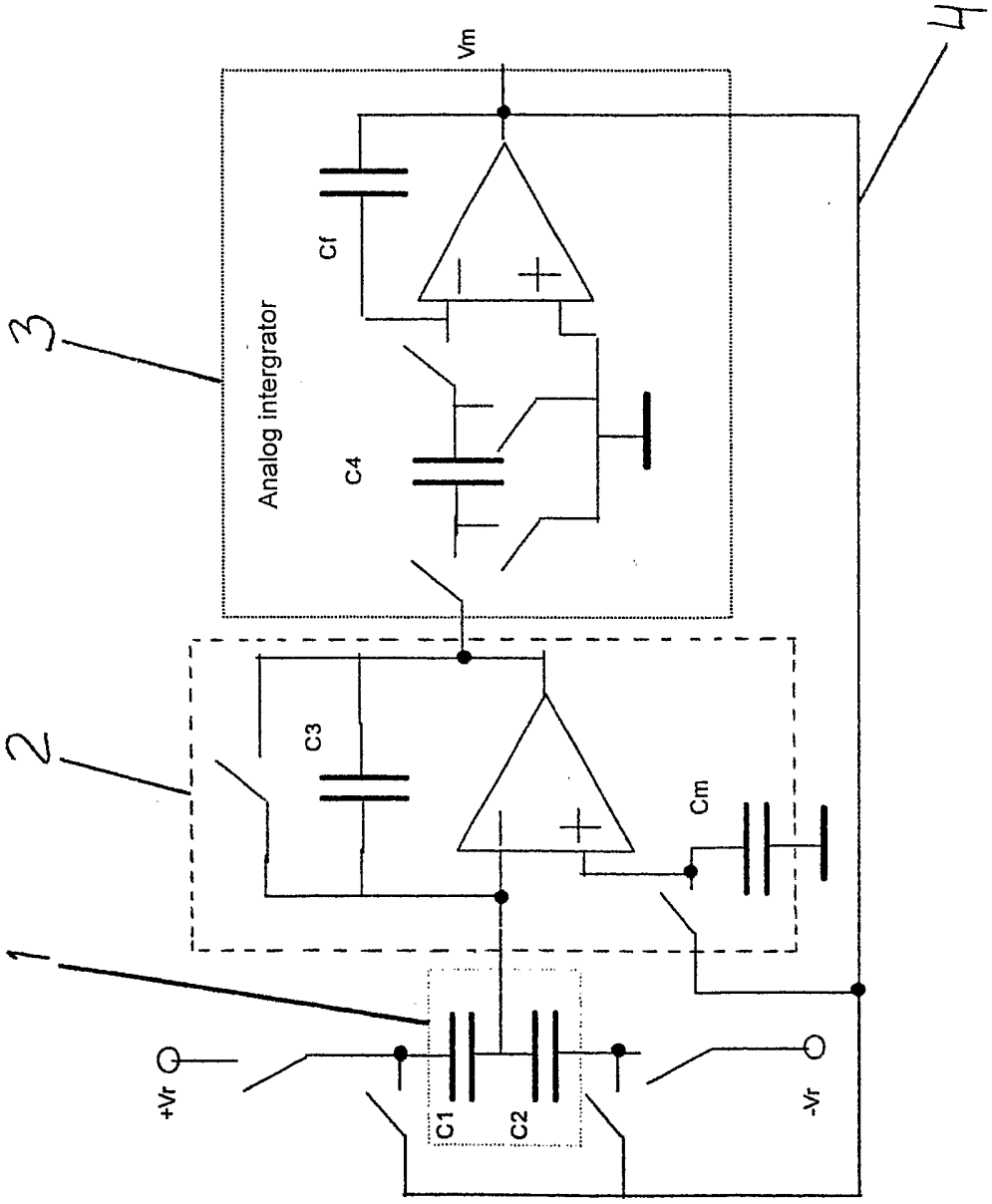
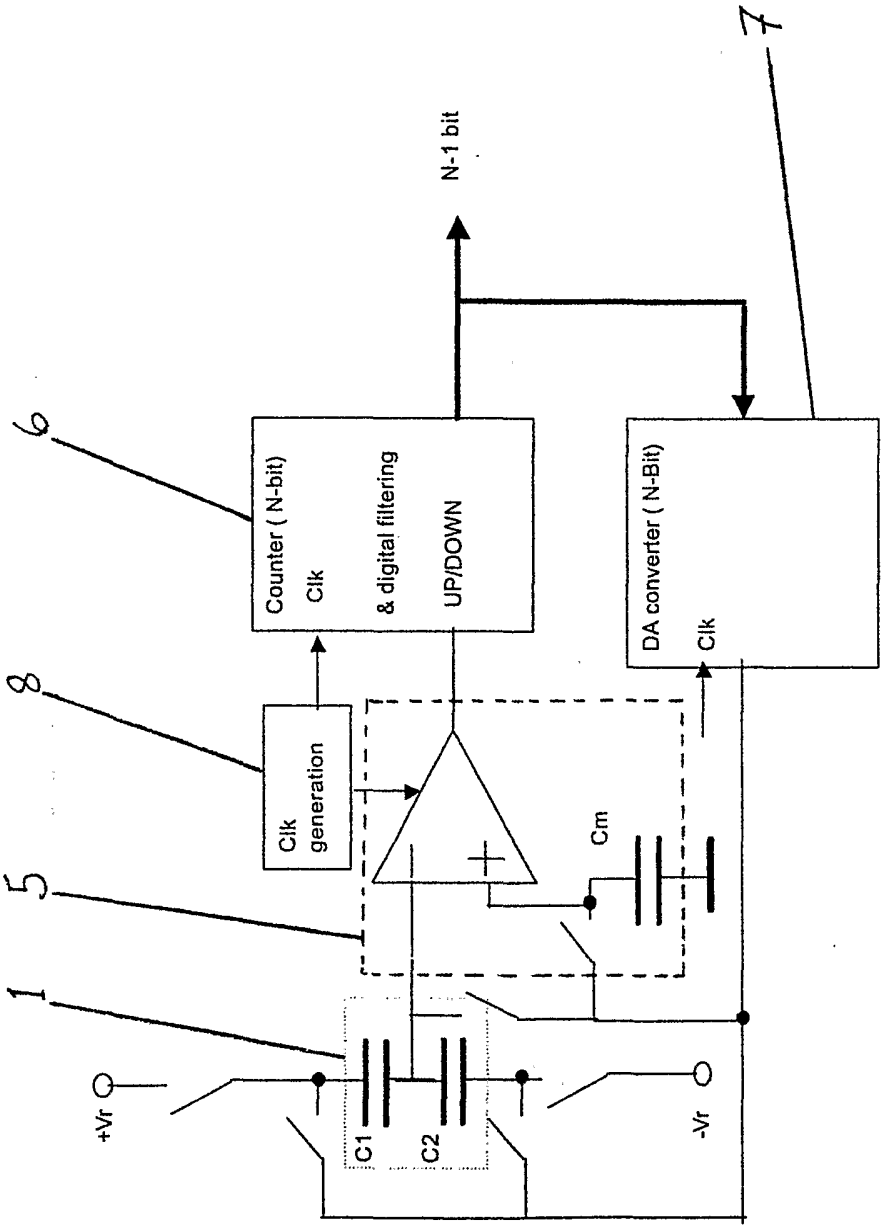


Fig. 1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& digital filtering
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DA converter (N-Bit)
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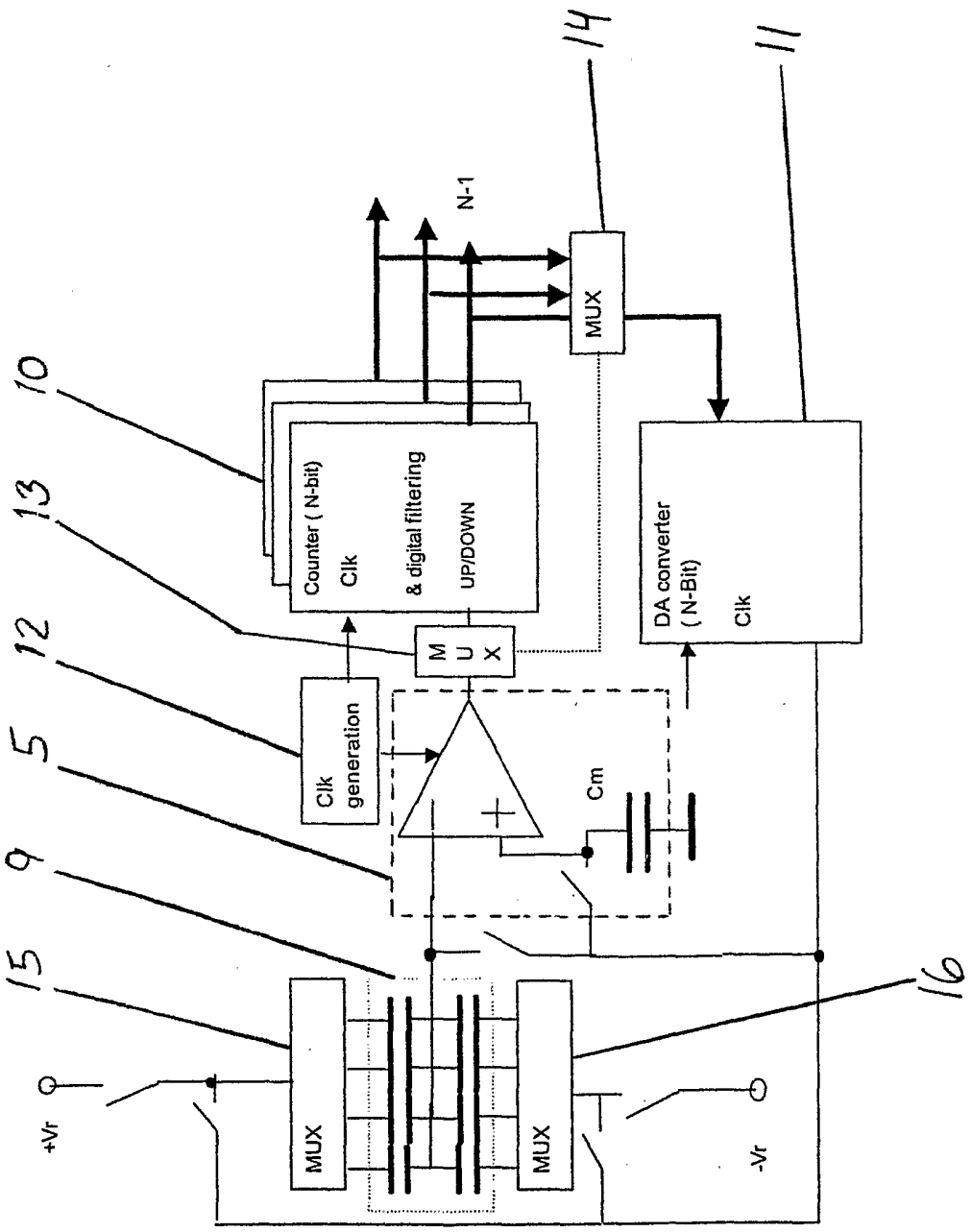
Fig. 2


14
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MUX
10
Counter (N-bit)
Clk
& digital filtering
UP/DOWN
DA converter
(N-Bit)
Clk
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X
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Clk
generation
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+Vr
MUX
MUX
-Vr

Fig. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/FI2004/000367

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01P15/125 G01R27/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G01P G01R H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 977 803 A (TSUGAI MASAHIRO) 2 November 1999 (1999-11-02) column 3, line 10 - line 15 column 7, line 20 - column 8, line 19 figures 5,15	1-29
A	US 4 860 232 A (LEE HAE-SEUNG ET AL) 22 August 1989 (1989-08-22) column 2, line 15 - column 31 column 5, line 1 - line 48 column 8, line 12 - line 15 column 8, line 53 - line 55 column 11, line 28 - line 29 figure 1	1-29

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
1 October 2004	13/10/2004

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
PCT/FI2004/000367

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KUNG J T ET AL: "DIGITAL CANCELLATION OF NOISE AND OFFSET FOR CAPACITIVE SENSORS" IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, IEEE INC. NEW YORK, US, vol. 42, no. 5, 1 October 1993 (1993-10-01), pages 939-942, XP000404057 ISSN: 0018-9456 the whole document	1-29

INTERNATIONAL SEARCH REPORT

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