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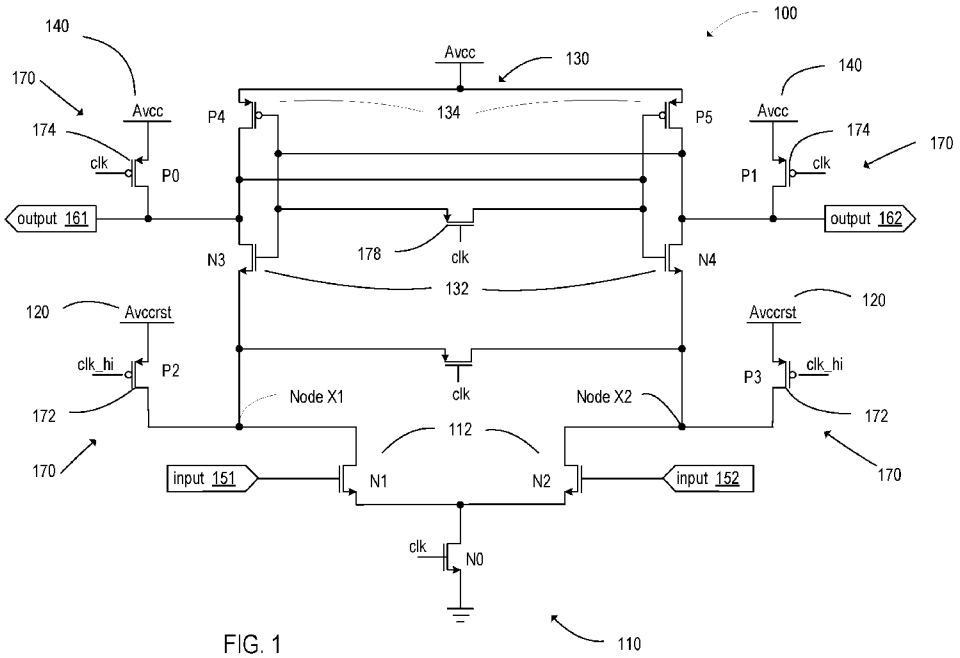

FIG. 1

(57) Abstract: Various implementations are presented herein that improve the performance of dynamic quantizers over process, voltage and temperature ("PVT") and input common mode (Vcm) variations. This can be accomplished by separating and then varying the voltage supply (1 10) to the reset devices (170) connected to the input devices of the quantizer while leaving the supply to the other parts of the quantizer unchanged. The timing performance of the quantizer can be improved (reduced clock-to-q) by lowering the voltage supply to the reset devices. The input referred RMS noise and offset voltage of the circuit can be improved (reduced) by raising the voltage supply to the reset devices. Similarly, increases in Vcm due to process and voltage scaling can be mitigated by raising the voltage supply to the reset devices. Control systems are also provided herein to control the voltage supply to the reset devices to accomplish these and other objectives.

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DYNAMIC QUANTIZERS HAVING MULTIPLE RESET LEVELS

TECHNICAL FIELD

The disclosure generally relates to quantizers, and more particularly to quantizers having multiple voltage supplies.

BACKGROUND

Quantizer circuits, sometimes referred to as “slicers”, are a type of high-speed clocked comparator which are used in serializer/deserializer (“SerDes”) and analog-to-digital conversion (“ADC”) circuits to quantize an analog signal to a digital bit. Three of the most important performance parameters of quantizers are timing measured as clock-to-q, input-referred RMS noise, and input-referred offset voltage. Input-referred RMS noise and offset voltage performance are linked by a common parameter, namely forward voltage gain, as both quantities are input-referred.

Quantizers can be broadly grouped into dynamic or static quantizers, wherein dynamic quantizers do not have any static power dissipation, and static quantizer types such as current mode logic (“CML”) quantizers do. Dynamic quantizers can be further sub-categorized into two groups, the first having what is sometimes referred to as having a STRONGARM®-type topology, sometimes referred to as a sense amplifier. The other group has what is sometimes referred to as a double-tail latch topology, which has comparatively greater sensitivity, lower input referred RMS noise and offset voltage for a given timing performance.

Dynamic quantizer timing performance is typically lowest at slow transistor process corner, high temperature and minimum supply voltage, as this process corner provides the minimum current and causes the slowest charging of the internal quantizer nodes. Input-referred RMS noise and offset voltage is typically worst at fast transistor process corner, high temperature and minimum supply voltage because that is the worst voltage gain process corner. As described herein, these process corners are referred to as the worst case timing and worst case RMS noise corners, respectively.

Previous approaches for improving input referred RMS noise and offset voltage of quantizers having the STRONGARM®-type topology have included reducing tail current, which raises the voltage gain of the quantizer. However,

this reduction in tail current increases clock-to-q time of the quantizer and thus degrades timing performance. Other approaches have included increasing tail current to improve clock-to-q time of the quantizer. However, this technique reduces gain and thus impairs input referred RMS noise and offset voltage. A further approach can include increasing the input device size to increase gain rather than reducing tail current to improve input referred RMS noise and offset voltage of the quantizer. However, this causes undesirable increases in input capacitance to driving circuits and internal parasitic capacitance which also degrades timing performance.

The present disclosure provides improvements for the configuration and operation of quantizers to address these and other issues, as set forth below.

SUMMARY

A number of implementations are directed toward a quantizer circuit for digitizing an analog signal. The quantizer typically includes an input circuit, a regeneration circuit and a reset circuit. The input circuit generally includes a plurality of input field effect transistors, and is coupled to a first voltage supply that supplies an input signal at a first voltage. The input circuit converts the input signal into an input current that is integrated during an input sampling phase of an active cycle of operation of the quantizer circuit. The regeneration circuit is coupled to the input circuit, and includes a plurality of regeneration field effect transistors. The regeneration circuit is connected to a second voltage supply at a second voltage. The second voltage is typically different in magnitude from the first voltage. The reset circuit, in turn, is coupled to the input circuit and the regeneration circuit.

In some implementations, the first voltage and second voltage can be fixed. If desired, the first voltage can be proportional to or derived from the second voltage. The first voltage can be configured to be higher than the second voltage to reduce noise and voltage offset in the quantizer circuit. In some implementations, the first voltage can be configured to be lower than the second voltage to improve timing performance of the quantizer circuit. The input circuit is preferably configured to receive a first time varying first clock signal, and the input circuit does not draw current when the first clock signal is below a threshold voltage.

In some implementations, the input circuit can be further configured to receive a second time varying clock signal. The magnitude of the second clock signal can be generated with reference to the first clock signal. For example, the second clock signal can be generated by a circuit supplied from a regulator that is configured to receive a signal indicative of the first clock signal.

In some implementations, the second voltage can be at ground and the first voltage can be lower than the second voltage to reduce noise and voltage offset in the quantizer circuit. In other implementations, the second voltage can be at ground, and the first voltage can be higher than the second voltage to improve timing performance of the quantizer circuit.

In accordance with further aspects of the disclosure, a control circuit is provided for operating quantizers in accordance with the present disclosure that is configured to increase or decrease the magnitude of the first voltage. The control circuit can include analog and/or digital components. In some implementations, an analog control circuit is provided that is configured to generate a reference signal representative of the first voltage. A regulator can be provided that is in operable communication with the analog control circuit that can be configured to output the first voltage to the quantizer circuit in response to the reference signal that is representative of the first voltage. If desired, the analog control circuit can generate the reference signal in response to a plurality of input signals. The input signals to the analog control circuit can include, for example, signals indicative of at least one of the magnitude of the second voltage, a process dependent voltage, a temperature dependent voltage, and/or a shift voltage.

In some implementations, the control circuit can include at least one analog to digital converter that is configured to receive a plurality of input signals and generate digital input signal data, a programmable integrated circuit operably coupled to the analog to digital converter, the programmable integrated circuit being configured to process the digital input signal data to determine circuit configuration data and generate a circuit configuration data digital output signal, and at least one digital to analog converter operably coupled to the processor. The at least one digital to analog converter can be configured to convert the circuit configuration data digital output signal into the reference signal representative of the first voltage. The input signals can include signals indicative of at least one of the magnitude of the second voltage, a process

dependent voltage, a common mode voltage, a temperature dependent voltage, and/or a shift voltage. The control circuit can further include a regulator in operable communication with the at least one digital to analog converter. The regulator can be configured to output the first voltage to the quantizer circuit in response to the reference signal that is representative of the first voltage. In various implementations, the programmable integrated circuit can be programmed with executable code for determining the configuration data. In further accordance with various embodiments, the quantizer circuit can include a topology typical of STRONGARM®-type quantizers and "double tail"-type quantizers, among others. Other features will be recognized from consideration of the Detailed Description and Claims, which follow.

BRIEF DESCRIPTION OF THE DRAWINGS

Various aspects and features of the disclosed devices and related methods will become apparent upon review of the following detailed description and upon reference to the drawings in which:

FIG. 1 depicts a quantizer in accordance with a first implementation of the present disclosure;

FIG. 2 depicts a quantizer in accordance with a second implementation of the present disclosure;

FIG. 3 depicts a quantizer in accordance with a third implementation of the present disclosure;

FIG. 4 depicts a quantizer in accordance with a fourth implementation of the present disclosure;

FIG. 5 depicts a quantizer in accordance with a fifth implementation of the present disclosure;

FIG. 6 depicts a quantizer in accordance with a sixth implementation of the present disclosure;

FIG. 7A depicts a first implementation of a control circuit for controlling a quantizer in accordance with the present disclosure;

FIG. 7B depicts an portion of the control circuit of FIG. 7A in accordance with the present disclosure;

FIG. 8 depicts a second implementation of a control circuit for controlling a quantizer in accordance with the present disclosure;

FIG. 9 depicts a circuit for analog process and temperature dependent voltage generation in accordance with the present disclosure;

FIG. 10 depicts a circuit for generating a low side reference for a regulator that supplies a clock generator that generates a clock signal in accordance with the present disclosure; and

FIG. 11 shows a programmable integrated circuit (IC) on which the disclosed circuits and processes may be implemented.

DETAILED DESCRIPTION

In the following description, numerous specific details are set forth to describe specific examples presented herein. It should be apparent, however, to one skilled in the art, that one or more other examples and/or variations of these examples may be practiced without all the specific details given below. In other instances, well known features have not been described in detail so as not to obscure the description of the examples herein. For ease of illustration, the same reference numerals may be used in different diagrams to refer to the same elements or additional instances of the same element.

Various implementations are presented herein that improve the overall performance of dynamic quantizers (or slicers) over process, voltage and temperature ("PVT") and input common mode (Vcm) variations. As set forth herein, certain embodiments are provided that improve the performance of a quantizer circuit by separating and then varying the voltage supply to the reset devices connected to the input devices of the quantizer while leaving the supply to the other parts of the quantizer unchanged. In some implementations, the timing performance of the quantizer can be improved (reduced clock-to-q) by lowering the voltage supply to the reset devices. In other implementations, the input referred RMS noise and offset voltage of the circuit can be improved (reduced) by raising the voltage supply to the reset devices. Similarly, increases in Vcm due to process and voltage scaling can be mitigated by raising the voltage supply to the reset devices. Control systems are provided herein to control the voltage supply to the reset devices to accomplish these and other objectives.

The disclosed embodiments permit tail current to be increased to meet the required timing performance and then subsequently increase the level of the

voltage supply to the reset devices in the aforementioned “worst case” RMS noise process corner to allow improvement of input referred RMS noise and offset voltage performance. Conversely, the disclosed embodiments permit the reduction of the tail current to meet the required input referred RMS noise and offset voltage performance and then lower the level of the voltage supply to the reset devices in the aforementioned “worst case” timing process corner to facilitate the improvement of timing performance.

Accordingly, the disclosed embodiments provide additional flexibility in the design of dynamic quantizers, such as those of the STRONGARM®-type or double-tail type latch topologies. In particular implementations, this is achieved by disconnecting the supply for the reset devices connected to the input devices from the main supply (referred to herein as Avcc or Avss) and connecting them to a separately controlled supply (referred to herein as Avccrst or Avssrst) to improve performance of the quantizer. This therefore facilitates raising/lowering the new Avccrst/Avssrst level to (i) improve input referred RMS noise and offset voltage performance of a quantizer and/or to (ii) mitigate Vcm increases. This also facilitates lowering/raising the Avccrst/Avssrst level to improve timing performance of a quantizer. These objectives can be facilitated by generating (i) a process and temperature (PT), (ii) process and voltage (PV), or (iii) process, voltage and temperature (PVT) dependent supply voltage to drive the new Avccrst/Avssrst supply, wherein “V” can be configured to be an appropriate combination of Avcc and Vcm.

Using a PVT compensated, logic Low supply to generate an Avccrst referenced clock allows reliable operation and avoids TDDB, HCI and BTI degradation, and which also generates a PVT compensated overdrive to the reset devices to enable them to operate at full clock rate.

The scope of the disclosure is applicable to dynamic quantizers, such as those of the STRONGARM®-type or double-tail type latch topologies. In the case of quantizers having a STRONGARM®-type topology, disclosed embodiments allow simultaneous improvement of timing performance and reduction of input referred RMS noise and offset voltage. While the disclosed embodiments are applicable to dynamic quantizers which are primarily used in the fields of serial communications and ADCs, they may also be used in other fields of detection, and are applicable to any circuit that makes use of resettable integration for signal gain. In the case of the double-tail latch quantizer topology,

the disclosed embodiments can be used for improvement of both (a) timing performance and (b) input referred RMS noise and offset voltage.

Turning now to the figures, for purposes of illustration, and not limitation, FIG. 1 depicts a quantizer in accordance with a first implementation of the present disclosure having a STRONGARM®-type topology. As illustrated in FIG. 1, a quantizer circuit 100 for digitizing an analog signal is presented that includes an input circuit, a regeneration circuit and a reset circuit. The input circuit 110 includes a plurality of input field effect transistors 112 and is coupled to a first voltage supply 120 that supplies an input signal at a first voltage, represented herein as Avccrst. As illustrated, the input circuit 110 is configured to receive a first time varying first clock signal (clk). The input circuit does not draw current when the first clock signal is below a threshold voltage and is active and consumes current when the first clock signal is above a threshold voltage.

The regeneration circuit 130 is coupled to the input circuit 110, and includes a plurality of regeneration field effect transistors 132, 134. The regeneration circuit is connected to a second voltage supply 140 at a second voltage Avcc. The second voltage Avcc is different in magnitude from the first voltage Avccrst (higher or lower, as desired) to bring about desired performance improvements as set forth herein.

The reset circuit 170 is coupled to the input circuit 110 and the regeneration circuit 130. The reset circuit 170 includes a first set of transistors 172 that couple the input circuit 110 to the first voltage supply 120, and a second set of transistors 174 that couple the regeneration circuit 130 to the second voltage supply 140, and a third transistor 178 that couples output pin 161 to output pin 162.

In operation the input circuit 110 converts the input signal via input pins 151, 152 into an input current that is integrated during an input sampling phase of an active cycle of operation of the quantizer circuit 100. During the input sampling phase, only devices N0, N1 and N2 (112) are initially on as the reset phase from the previous cycle is complete and PMOS's P0, P1, P2 and P3 (172, 174) of the reset circuit are off.

To improve gain and thus reduce noise/voltage offset, for example, it is desirable that the devices in input circuit 110 operate in saturation for as much of the active cycle as possible, albeit at the expense of timing performance as eventually all the devices enter the linear region (exit the saturation region) as regeneration occurs. The device N0 enters the linear region first once the voltage on its drain is less than Avcc –Vth0. This is followed later by devices N1 and N2 entering the linear region when nodes X1 and X2 become less than (Vcm-Vth1) and (Vcm-Vth2) respectively, wherein Vcm is the common mode voltage at the inputs 151,152 and Vth0, Vth1 and Vth2 are the respective threshold voltages of devices N0, N1 and N2. The input sampling phase ends approximately at the same time that N1 and N2 enter the linear region.

Towards the end of the input sampling phase (before N1 and N2 enter the linear region), and once nodes X1 and X2 become less than (Avcc – Vth34), wherein Vth34 is the threshold voltages of N3 and N4, the regeneration devices N3 and N4 turn on to from a secondary integration network. N3 and N4 are also saturated during this time, and regeneration around these devices begins. The quantizer circuit 100 remains in the second phase of operation as long as N1 – N4 remain in saturation.

Once N3 and N4 have been on long enough to discharge at output pins 161, 162 to less than (Avcc – Vthp12), wherein Vthp12 is the threshold voltages of P1 and P2, full regeneration begins. The regeneration circuit 130 amplifies the differential voltage, generated by the input circuit across nodes X1 and X2 (and also by N3/N4 across output pins 161, 162) during the input sampling phase, using positive feedback to create large signal voltages close to CMOS levels at output pins 161, 162.

As the quantizer circuit 100 enters a third phase of operation, P4, P5, N3 and N4 regenerate. This third phase begins when any of N1 to N4 are no longer saturated. N3 and N4 continue to regenerate in the third phase, and P4 and P5 start to conduct. The third phase of operation ends at reset on the falling edge of the clock signal.

Advantages in accordance with the disclosure originate from providing multiple voltage supplies to the quantizer 100, and in some embodiments, varying the relative voltage levels of the voltage supplies.

Input referred RMS noise and input referred offset voltage can both be reduced by increasing the quantizer gain. It should be noted that the exemplary quantizers illustrated herein are illustrated without offset correction. However, as will be appreciated, quantizers of all static and dynamic topologies can usually be provided with input referred voltage offset correction based on either current/voltage or capacitive correction as are known in the art.

Since the quantizer 100 operates in a sequence of phases as set forth above, the gain in earlier phases provide greater reduction of input referred RMS noise and offset voltage. Thus, by increasing the gain in the first phase of quantizer operation, input referred RMS noise and offset voltage can be reduced. Thus, Avccrst can be adjusted, or simply fixed to a value that is greater than Avcc to reduce RMS noise and voltage offset.

Conversely, Avccrst can be adjusted, or simply fixed to a value that is less than Avcc to reduce clock-to-q and improve timing. In accordance with further implementations, Avccrst can be controlled to be set at a value that tracks a combination of process, voltage and temperature (PVT) to improve timing and reduce RMS noise and voltage offset over various operating conditions of the quantizer.

In accordance with a further aspect of the disclosure, quantizers can compensate for an increase in input common mode voltage (Vcm) with minimal power increase. This is particularly advantageous where supply voltages scale down with geometry. Quantizers normally are placed at the boundary between the analog and digital signal processing. This usually means that its input is delivered from a higher analog supply domain than its own digital supply domain (e.g., Avcc). The average of this input is called the common mode input voltage, Vcm. High Vcm values reduce gain and thus increase RMS noise and offset voltage.

As process technologies scale down, digital supply also reduces (e.g. from 0.85v to 0.75v), for example, to mitigate reliability issues, to reduce digital power consumption for fixed processing performance, or to increase digital processing performance for constant or reduced power consumption. Accordingly, the analog supply does not reduce or its reduction is less than the digital supply reduction which means the Vcm of the quantizer has effectively been raised relative to the new lower Avcc value of the quantizer.

In this situation, notwithstanding the present disclosure, the skilled artisan would only have two options with respect to the present sense amplifier (e.g., STRONGARM®-type) quantizer topologies. One could tolerate lower gain and thus higher RMS noise and voltage offset, or do not scale down quantizer supply to preserve quantizer gain. However, the latter option results in having to tolerate higher power consumption in quantizer, needing to add a regulator to generate an older, unscaled Avcc level, and to level shift the quantizer output down to Avcc. However, by employing the present teachings, Avccrst can retain the older, unscaled Avcc supply voltage level (e.g. 0.85v). This preserves gain and thus RMS noise and offset voltage are improved. The remainder of quantizer is then powered by the scaled Avcc level (e.g. 0.75v).

In accordance with the present disclosure, Avccrst can be fixed, or it can be varied in a controlled manner, depending on the desired application. Thus, in some implementations, the first voltage (Avccrst) and second voltage (Avcc) can be fixed relative to one another. If desired, the first voltage (Avccrst) can be proportional to or derived from the second voltage (Avcc). As mentioned above, the first voltage (Avccrst) can be higher than the second voltage (Avcc) to reduce noise and voltage offset in the quantizer circuit. In some embodiments, the first voltage (Avccrst) can be lower than the second voltage (Avcc) to improve timing performance of the quantizer circuit, as described above.

FIGS. 2 and 3 depict further embodiments of quantizers 200, 300, respectively in accordance with the present disclosure. Quantizers 200, 300 are of the “double tail” type, and include input circuits 210 and 310, respectively. Each of the input circuits includes N0, N1, N2, N5 and N6 (wherein N5 and N6 provide additional gain) and a regeneration circuit 230, 330 including N3, N4, P4 and P5 (and N7 and N8 in the case of circuit 300). N7 and N8 can be considered to be a part of the reset circuit for simplicity, although they also provide additional gain as they combine with P0 and P1 (FIG. 3).

Each of circuits 210, 230 has separate currents which allow input stage gain and regeneration stage timing to be optimized separately. Specifically, the input devices (N1, N2, N5, N6) have separate currents from the regeneration devices (N3, N4, P4, P5).

The quantizer 200 of FIG. 2 includes a dual phase clock, whereas the quantizer of FIG. 3 includes a single phase clock. The embodiment of FIG. 3

includes an extra gain path from Nodes X1, X2 to out, outb by way of P0, P1, N7, N8.

The input circuit 210, 310 integrates the input in exactly the same way as the embodiment of FIG. 1 onto nodes X1 and X2. Input circuit 210, 310 contributes gain from the input 251, 252 (351, 352) as long as the input devices N1 and N2 are saturated. However, by adding Avccrst pins, it is possible to increase the initial voltage as with the embodiment of FIG. 1. Increasing the initial starting voltage in such a manner has the same practical effect as reducing the tail current in terms of increasing the time that occurs before the input pair N1, N2 come out of saturation. This increases integration time and therefore increases gain, and thus reduces RMS noise and offset voltage.

In some implementations, the second voltage can be at ground and the first voltage can be lower than the second voltage to reduce noise and voltage offset in the quantizer circuit. For example, the second voltage can be at ground, and the first voltage can be higher than the second voltage to improve timing performance of the quantizer circuit.

For purposes of illustration, and not limitation, FIG. 4, 5 and 6 depict quantizers 400, 500, 600 in accordance with further implementations of the present disclosure. In some implementations, it can be convenient to use a low input common mode voltage (Vcm) at the point where the analog signal is quantized to a digital bit. This leads to a low input Vcm for the quantizer. The quantizers 100, 200 described herein above have NMOS input pair(s) which are suited to a high input Vcm. Each of the aforementioned quantizers can be inverted from a high input Vcm, NMOS input pair(s) quantizer to a low input Vcm, PMOS input pair(s) quantizer. In such low input Vcm circuits, the reset voltage is swapped from Avcc to ground (Gnd), or Avss. In the case of the double tail latch topology, the output reset is swapped from ground (Avss) to Avcc. FIGS. 4, 5 and 6 illustrate these low input Vcm, PMOS input pair quantizers for three topologies, including a STRONGARM®-type technology (FIG. 4), a double tail latch topology (FIG. 5) and a modified double tail latch topology (FIG. 6).

The low input Vcm, PMOS input pair(s) quantizers of FIGS. 4-6 all integrate the input in the input circuits (410, 510, 610) onto nodes X1 and X2 in the same way as the embodiments of FIGS. 1-3. The input circuit of these embodiments contributes gain from the input as long as the input devices P1 and P2 are saturated. Ordinarily, in such topologies, the drains are reset to Avss and

are then pulled upwards towards Avcc by the common mode current. In accordance with the present disclosure, the initial voltage can be decreased by adding pins to apply Avssrst rather than Avss. This acts to decrease the initial voltage Avssrst to a voltage less than ground (Avss), resulting in increased integration time, which in turn increases gain and decreases input referred RMS noise and input offset voltage. Conversely, increasing Avssrst to a voltage that is greater than ground decreases integration time, which increases timing performance by reducing clock-to-q. In the same way as previously described the level of Avssrst can be fixed, or varied over PVT in an optimized manner to improve both input referred RMS noise and input offset voltage, and/or timing performance.

In accordance with further aspects of the disclosure, embodiments of a control circuit are provided that are configured to increase or decrease the magnitude of the first voltage with respect to Avcc or Avss for operating quantizers in accordance with the present disclosure.

As illustrated in FIGS. 7A-7B, the control circuit can include an analog control circuit 700 that is configured to generate a reference signal representative of the first voltage. A regulator 710 can be provided that is in operable communication with the analog control circuit 700. The regulator 710 can be configured to output the first voltage to the quantizer circuit in response to the reference signal that is representative of the first voltage. The analog control circuit can generate the reference signal (Vref_reg) in response to a plurality of input signals (702, 704, Avcc, Vcm). The input signals can include signals indicative of at least one of the magnitude of the second voltage, a process dependent voltage, a temperature dependent voltage, or a shift voltage. FIG. 7B depicts a possible implementation of a summer used in the control circuit of FIG. 7A, where other summer topologies, both voltage & current summers, may also be used by those skilled in the art, in accordance with the present disclosure. As will be appreciated, process dependent voltage and temperature dependent voltage inputs, along with Avcc (or Avss) can be provided to a programmable switch or summer 706 which is then processed in circuit 720 to produce the reference voltage which is outputted to the regulator.

The processing circuit 720 includes an operational amplifier that will output a voltage that is more or less than Avcc depending on the input process and temperature dependent voltage. Thus, by selecting the input process and

temperature dependent voltage appropriately, the reference voltage, and thus Avccrst can be more or less than Avcc. Similarly, if Avss is being referenced, the input process and temperature dependent voltage can be selected to have Avssrst be more or less than Avss. As will be appreciated, FIGS. 7A-7B (as well as the other figures herein) are intended to be illustrative and not limiting.

As illustrated in FIG. 8, in some implementations, the control circuit 800 can include at least one analog to digital converter 808 that is configured to receive a plurality of input signals and generate digital input signal data, a programmable integrated circuit (810) operably coupled to the at least one analog-to-digital converter ("ADC") 808, the programmable integrated circuit (810) being configured to process the digital input signal data to determine circuit configuration data and generate a circuit configuration data digital output signal, and at least one digital to analog converter (812) operably coupled to the processor. The at least one digital to analog converter can be configured to convert the circuit configuration data digital output signal into the reference signal representative of the first voltage.

The input signals can include signals indicative of at least one of the magnitude of the second voltage, a magnitude of the common mode voltage (Vcm), a process dependent voltage 802, a temperature dependent voltage 804, or a shift voltage. As depicted, a single ADC and a multiplexer can sequentially poll these four analog inputs to generate a digital code from the selected analog input signal. However, it is also possible (although more costly in terms of hardware) to use a larger number of ADC's, such as one ADC per input signal (e.g., four total) and send four digital codes, one corresponding to each input signal, to the processor, in parallel.

The control circuit (800) can further include a regulator (814) in operable communication with the at least one digital to analog converter (812). The regulator can be configured to output the first voltage (Avccrst) to the quantizer circuit in response to the reference signal (Vref_reg) that is representative of the first voltage. In various embodiments, the programmable integrated circuit (810) can be programmed with executable code for determining the configuration data.

FIG. 9 depicts a circuit 900 for analog process and temperature dependent voltage generation in accordance with the present disclosure. The analog Vref_reg generation circuit needs an analog process and temperature dependent voltage (Vproc_temp). One embodiment of the analog process and

temperature dependent voltage generation is shown here. As illustrated in FIG. 9, a current is forced into a stack of X NMOS devices. The number of devices, X, is chosen to set the required Vproc_temp. The device at the top of the stack can be selected to match N3/N4 in the circuit (e.g., 100) order to track Vt, and lower devices can be selected to match i/p beta (N1/N2) and track gm.

FIG. 10 depicts a circuit 950 for generating a low side reference for a regulator that supplies a clock generator that generates a clock signal in accordance with the present disclosure. In some implementations, the input circuit (e.g., 110) can be further configured to receive a second time varying clock signal (clk_hi). The magnitude of the second clock signal can be generated with reference to the first clock signal. The second clock signal (clk_hi) can be generated by a circuit that is configured to receive a signal indicative of the first clock signal and is supplied from a regulator that is configured to receive a low side reference voltage.

When Avccrst > Avcc the PMOS the reset devices P2, P3 in the quantizer need a clock (clk_hi) that has a logic High level of Avccrst rather than Avcc. The clock buffer for the quantizer 100 generates a clock named clk which has a logic High level of Avcc. Clk_hi can be generated from clk using a high speed, AC coupled clock generator as described in the literature. However the low logic level of this clock, clk_hi, cannot be zero volts zero volts in modern CMOS processes when Avccrst > Avcc. That would create reliability problems. Thus, a new logic low level for the clk_hi generator is provided, labeled Vneg_clk_ref herein. This is in turn generated by a regulator which has reference Vneg_clk_ref. However, when Avccrst < Avcc and is at its minimum value the value of Vneg_clk_ref must float downwards with Avccrst towards Avss. To do this Vneg_clk_ref is generated with respect to Avccrst supply. The reference is implemented as a stack of PMOS devices (P1…Px) as illustrated in FIG. 10 which are matched to P2, P3 in the quantizer.

The disclosure further contemplates the bulk or well connection of the devices (100, 200…). In general, PMOS devices have their bulk connection tied to the highest voltage supply which is normally Avcc as illustrated in the present Figures. In general, NMOS devices have their bulk connection tied to the lowest voltage supply which is normally Avss in these diagrams. However the addition of Avccrst and Avssrst means that Avcc and Avss are not necessarily the highest and lowest supplies, respectively. It is easiest to retain the Avcc and Avss bulk

connection for all PMOS and NMOS devices disclosed herein, respectively, except for the reset devices connected to Avccrst or Avssrst. However, it is also possible, in accordance with the disclosure, for connecting all PMOS and NMOS bulk connections to Avccrst or Avssrst, respectively. The bulk connection of PMOS and NMOS reset devices powered from Avccrst or Avssrst is thus application dependent.

Modern high-volume CMOS processes typically use a p-substrate with electrically isolated N-wells. PMOS devices reside in N-wells. The N-wells can be at different potentials and are connected to one or many positive supply voltages. NMOS devices reside in P-wells which are not electrically isolated from the p-substrate. The p-substrate is typically connected to zero volts and is usually denoted as Gnd or Avss.

Use of Avssrst < Avss is believed to be facilitated by either (a) a deep N-well to create electrically isolated p-substrate islands on p-substrate process, or (b) n-substrate process with electrically isolated P-wells.

It is possible to achieve connection of all PMOS/NMOS device bulks to Avccrst/Avssrst. In this instance, one can connect all PMOS device bulks to Avccrst in a high Vcm, NMOS i/p quantizer. It is also possible to connect all NMOS device bulks to Avssrst in a low Vcm, PMOS i/p quantizer. This can be advantageous as it provides for a denser layout, as all wells are of the same potential. However, the disadvantage in both cases is an increased Vt (planar processes) of all the non- reset devices whose source is still either Avcc or Avss. There are two basic options to connect the bulk of PMOS reset devices powered from Avccrst. First, one can connect the bulk to Avccrst. Second, the bulk can be connected to Avcc. Similarly, the bulk of NMOS reset devices can be connected to Avssrst, or Avss. Connecting the bulk of the reset devices to Avccrst/Avssrst tends to be safer electrically, but may take up more space. This is believed to be the best connection for non-FinFET processes where non-zero values of bulk to source voltage can impair performance.

FIG. 11 shows a programmable integrated circuit (IC) 1000 on which the disclosed circuits and processes may be implemented. The programmable IC may also be referred to as a System on Chip (SOC) that includes field programmable gate array logic (FPGA) along with other programmable resources. FPGA logic may include several different types of programmable logic blocks in the array. For example, FIG. 11 illustrates a programmable IC

1000 that includes a large number of different programmable tiles including multi-gigabit transceivers (MGTs) 1001, configurable logic blocks (CLBs) 1002, blocks of random access memory (BRAMs) 1003, input/output blocks (IOBs) 1004, configuration and clocking logic (CONFIG/CLOCKS) 1005, digital signal processing blocks (DSPs) 1006, specialized input/output blocks (I/O) 1007, for example, clock ports, and other programmable logic 1008 such as digital clock managers, analog-to-digital converters, system monitoring logic, and so forth. Some programmable IC having FPGA logic also include dedicated processor blocks (PROC) 1010 and internal and external reconfiguration ports (not shown).

In some FPGA logic, each programmable tile includes a programmable interconnect element (INT) 1011 having standardized connections to and from a corresponding interconnect element in each adjacent tile. Therefore, the programmable interconnect elements taken together implement the programmable interconnect structure for the illustrated FPGA logic. The programmable interconnect element INT 1011 also includes the connections to and from the programmable logic element within the same tile, as shown by the examples included at the top of FIG. 11.

For example, a CLB 1002 can include a configurable logic element CLE 1012 that can be programmed to implement user logic, plus a single programmable interconnect element INT 1011. A BRAM 1003 can include a BRAM logic element (BRL) 1013 in addition to one or more programmable interconnect elements. Often, the number of interconnect elements included in a tile depends on the height of the tile. In the pictured implementation, a BRAM tile has the same height as five CLBs, but other numbers (e.g., four) can also be used. A DSP tile 1006 can include a DSP logic element (DSPL) 1014 in addition to an appropriate number of programmable interconnect elements. An IOB 1004 can include, for example, two instances of an input/output logic element (IOL) 1015 in addition to one instance of the programmable interconnect element INT 1011. As will be clear to those of skill in the art, the actual I/O bond pads connected, for example, to the I/O logic element 1015, are manufactured using metal layered above the various illustrated logic blocks, and typically are not confined to the area of the input/output logic element 1015.

In the pictured implementation, a columnar area near the center of the die (shown shaded in FIG. 11) is used for configuration, clock, and other control logic. Horizontal areas 1009 extending from the column are used to distribute

the clocks and configuration signals across the breadth of the programmable IC. Note that the references to "columnar" and "horizontal" areas are relative to viewing the drawing in a portrait orientation.

Some programmable ICs utilizing the architecture illustrated in FIG. 11 include additional logic blocks that disrupt the regular columnar structure making up a large part of the programmable IC. The additional logic blocks can be programmable blocks and/or dedicated logic. For example, the processor block PROC 1010 shown in FIG. 11 spans several columns of CLBs and BRAMs.

Note that FIG. 11 is intended to illustrate only an example of programmable IC architecture. The numbers of logic blocks in a column, the relative widths of the columns, the number and order of columns, the types of logic blocks included in the columns, the relative sizes of the logic blocks, and the interconnect/logic implementations included at the top of FIG. 11 are provided purely as examples. For example, in an actual programmable IC, more than one adjacent column of CLBs is typically included wherever the CLBs appear, to facilitate the efficient implementation of user logic.

For the various flow diagrams depicted herein, the particular orders of the blocks and associated functions are provided as examples. The ordering is not necessarily limiting and can be varied according to various implementations.

Those skilled in the art will appreciate that various alternative computing arrangements, including one or more processors and a memory arrangement configured with program code, would be suitable for hosting the processes and data structures that may carry out functions disclosed herein. In addition, the processes may be provided via a variety of computer-readable storage media or delivery channels such as magnetic or optical disks or tapes, electronic storage devices, or as application services over a network.

Though aspects and features may in some cases be described in individual figures, it will be appreciated that features from one figure can be combined with features of another figure even though the combination is not explicitly shown or explicitly described as a combination.

The methods and system are thought to be applicable to a variety of systems that use RAM circuits. Other aspects and features will be apparent to those skilled in the art from consideration of the specification. The portions of the methods and system may be implemented as one or more processors configured to execute software, as an application specific integrated circuit

(ASIC), or as a logic on a programmable logic device. Moreover, the various circuits identified herein may share hardware circuitry, such as use of a common computer processing unit or digital processing unit. It is intended that the specification and drawings be considered as examples only, with a true scope of the invention being indicated by the following claims.

CLAIMS

What is claimed is:

1. A quantizer circuit for digitizing an analog signal, comprising:

an input circuit including a plurality of input field effect transistors, the input circuit being coupled to a first voltage supply that supplies an input signal at a first voltage, wherein the input circuit converts the input signal into an input current that is integrated during an input sampling phase of an active cycle of operation of the quantizer circuit;

a regeneration circuit coupled to the input circuit, the regeneration circuit including a plurality of regeneration field effect transistors, the regeneration circuit being connected to a second voltage supply at a second voltage, the second voltage being different from the first voltage; and

a reset circuit coupled to the input circuit and the regeneration circuit.

2. The quantizer circuit of Claim 1, wherein the first voltage is higher than the second voltage to reduce noise and voltage offset in the quantizer circuit or the first voltage is lower than the second voltage to improve timing performance of the quantizer circuit.

3. The quantizer circuit of Claim 1 or claim 2, wherein:

the input circuit is configured to receive a first time varying first clock signal;

the input circuit is further configured to receive a second time varying clock signal; and

the magnitude of the second clock signal is generated with reference to the first clock signal.

4. The quantizer circuit of Claim 3, wherein the second clock signal is generated by a circuit supplied from a regulator that is configured to receive a signal indicative of the first clock signal.

5. The quantizer circuit of any of Claims 1-4, wherein the second voltage is at ground and the first voltage is lower than the second voltage to reduce noise and voltage offset in the quantizer circuit or wherein the second voltage is at

ground and the first voltage is higher than the second voltage to improve timing performance of the quantizer circuit.

6. The quantizer circuit of any of Claims 1-5, further comprising a control circuit that is configured to increase or decrease magnitude of the first voltage, wherein the control circuit includes an analog control circuit that is configured to generate a reference signal representative of the first voltage.

7. The quantizer circuit of Claim 6, further comprising a regulator in operable communication with the analog control circuit, the regulator being configured to output the first voltage to the quantizer circuit in response to the reference signal that is representative of the first voltage.

8. The quantizer circuit of Claim 6, wherein the analog control circuit generates the reference signal in response to a plurality of input signals.

9. The quantizer circuit of any of Claims 1-8, further comprising a control circuit that is configured to increase or decrease magnitude of the first voltage, wherein the control circuit includes:

at least one analog-to-digital converter that is configured to receive a plurality of input signals and generate digital input signal data, wherein the input signals include signals indicative of at least one of a magnitude of the second voltage, a process dependent voltage, a magnitude of a common mode voltage, a temperature dependent voltage, or a shift voltage;

a programmable integrated circuit operably coupled to the at least one analog-to-digital converter, the programmable integrated circuit being configured to process the digital input signal data to determine circuit configuration data and generate a circuit configuration data digital output signal, wherein the programmable integrated circuit is programmed with executable code for determining the configuration data; and

at least one digital-to-analog converter operably coupled to the programmable integrated circuit, the at least one digital-to-analog converter being configured to convert the circuit configuration data digital output signal into the reference signal representative of the first voltage.

10. The quantizer circuit of Claim 9, further comprising a regulator in operable communication with the at least one digital-to-analog converter, the regulator being configured to output the first voltage to the quantizer circuit in response to the reference signal that is representative of the first voltage.

11. The quantizer circuit of Claim 8, wherein the quantizer includes a bulk or well connection.

12. The quantizer circuit of any of Claims 1-11, wherein the plurality of input field effect transistors include N- type field effect transistors, and further wherein the input circuit does not draw current when the first clock signal is below a threshold voltage.

13. The quantizer circuit of any of Claims 1-12, wherein the plurality of input field effect transistors include P- type field effect transistors, and further wherein the input circuit does not draw current when the first clock signal is above a threshold voltage.

14. The quantizer of any of Claims 1-13, wherein the reset circuit includes a first set of transistors that couple the input circuit to the first voltage supply, a second set of transistors that couple the regeneration circuit to the second voltage supply, and a third transistor that couples a plurality of output pins of the quantizer to each other.

15. The quantizer of any of Claims 1-14, wherein the each of the input circuit and regeneration circuit are configured and arranged to have separate currents and a plurality of clock signal inputs which allow input stage gain and regeneration stage timing to be controlled separately.

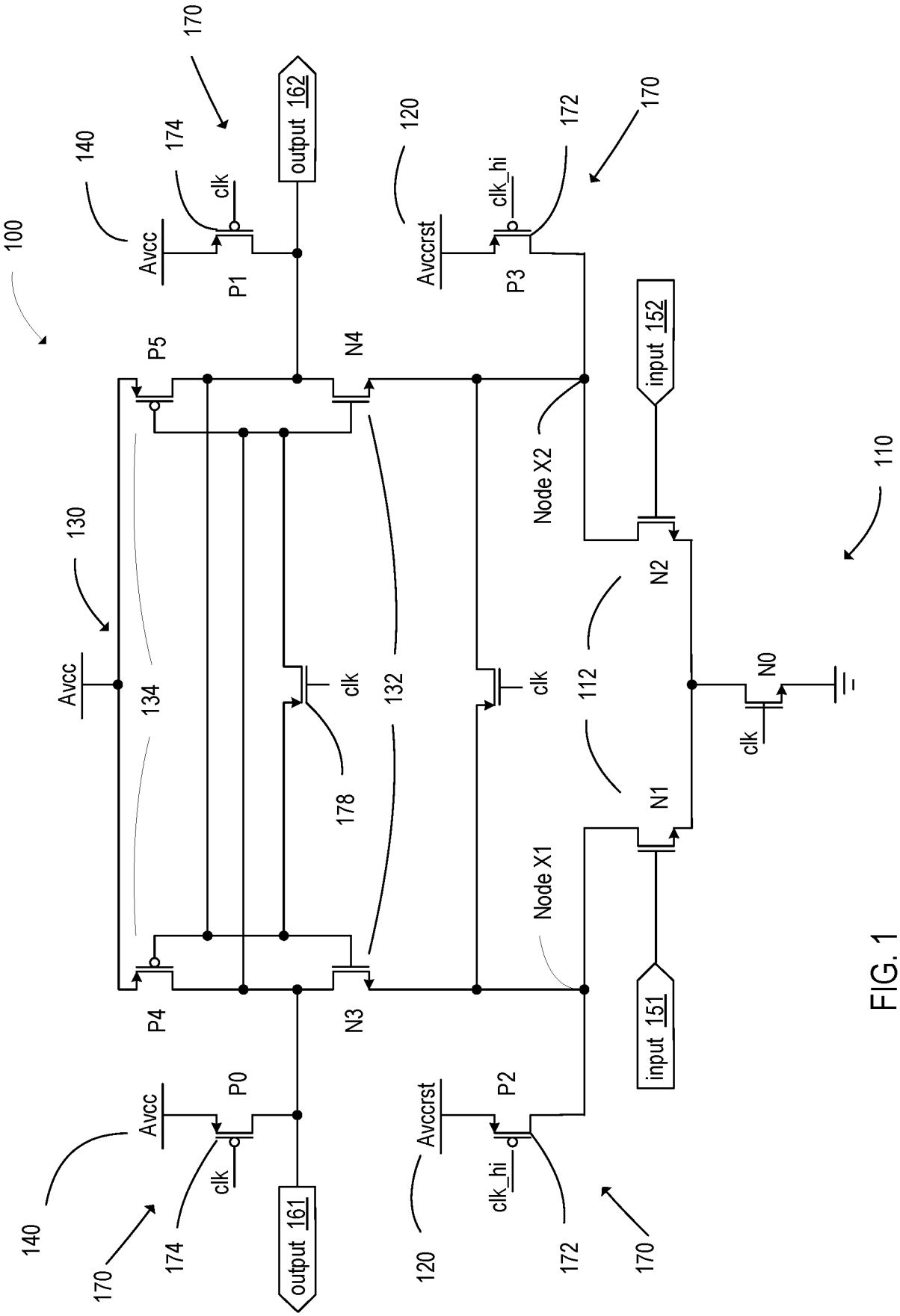
100
110
120
130
132
134
140
170
172
174
178
112
Avcc
Avccrst
clk
clk_hi
P0
P1
P2
P3
P4
P5
N0
N1
N2
N3
N4
Node X1
Node X2
input 151
input 152
output 161
output 162

FIG. 1

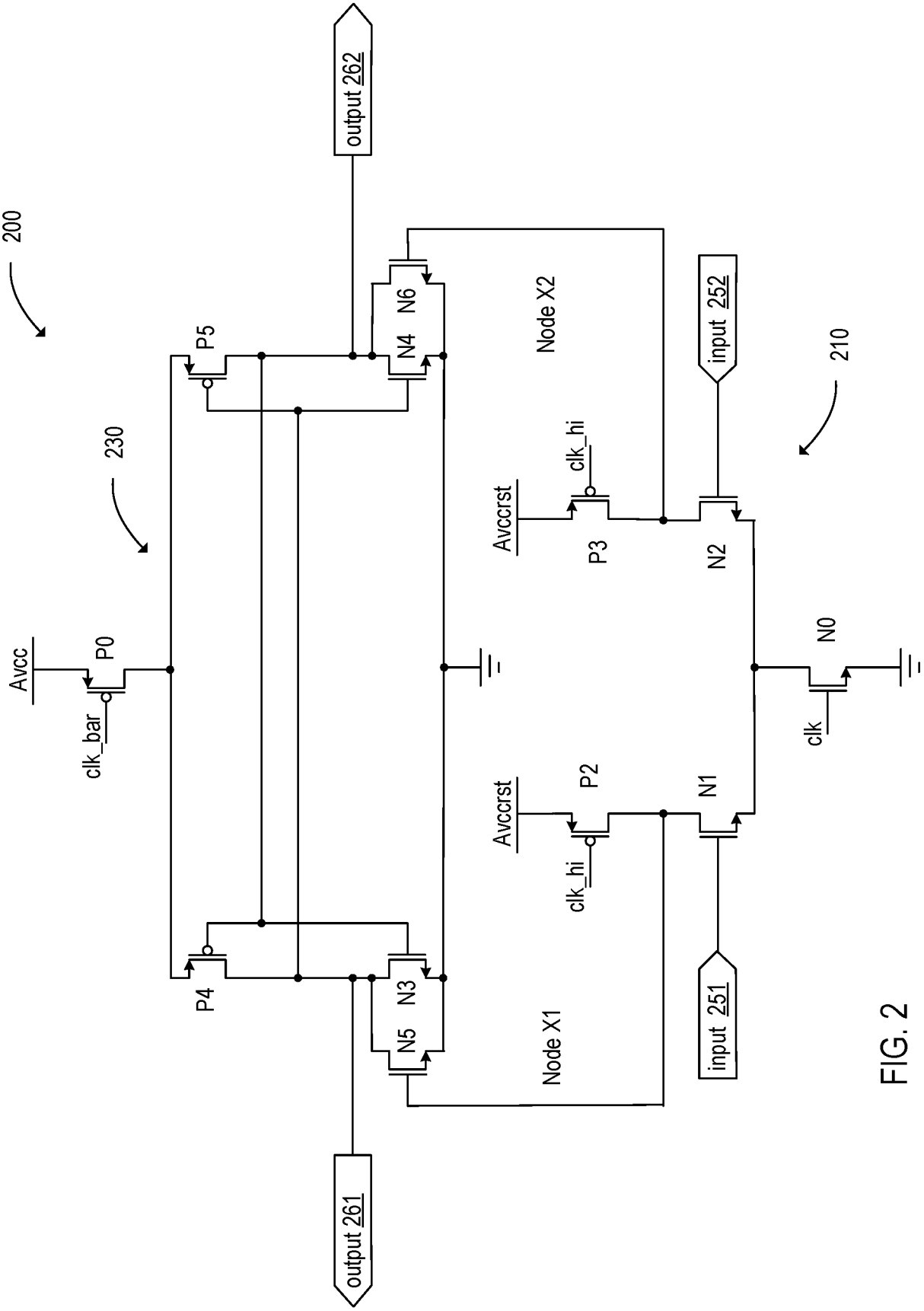
200
230
210
output 262
output 261
input 252
input 251
Node X2
Node X1
Avcc
clk_bar
clk_hi
Avccrst
clk
P0
P2
P3
P4
P5
N0
N1
N2
N3
N4
N5
N6

FIG. 2

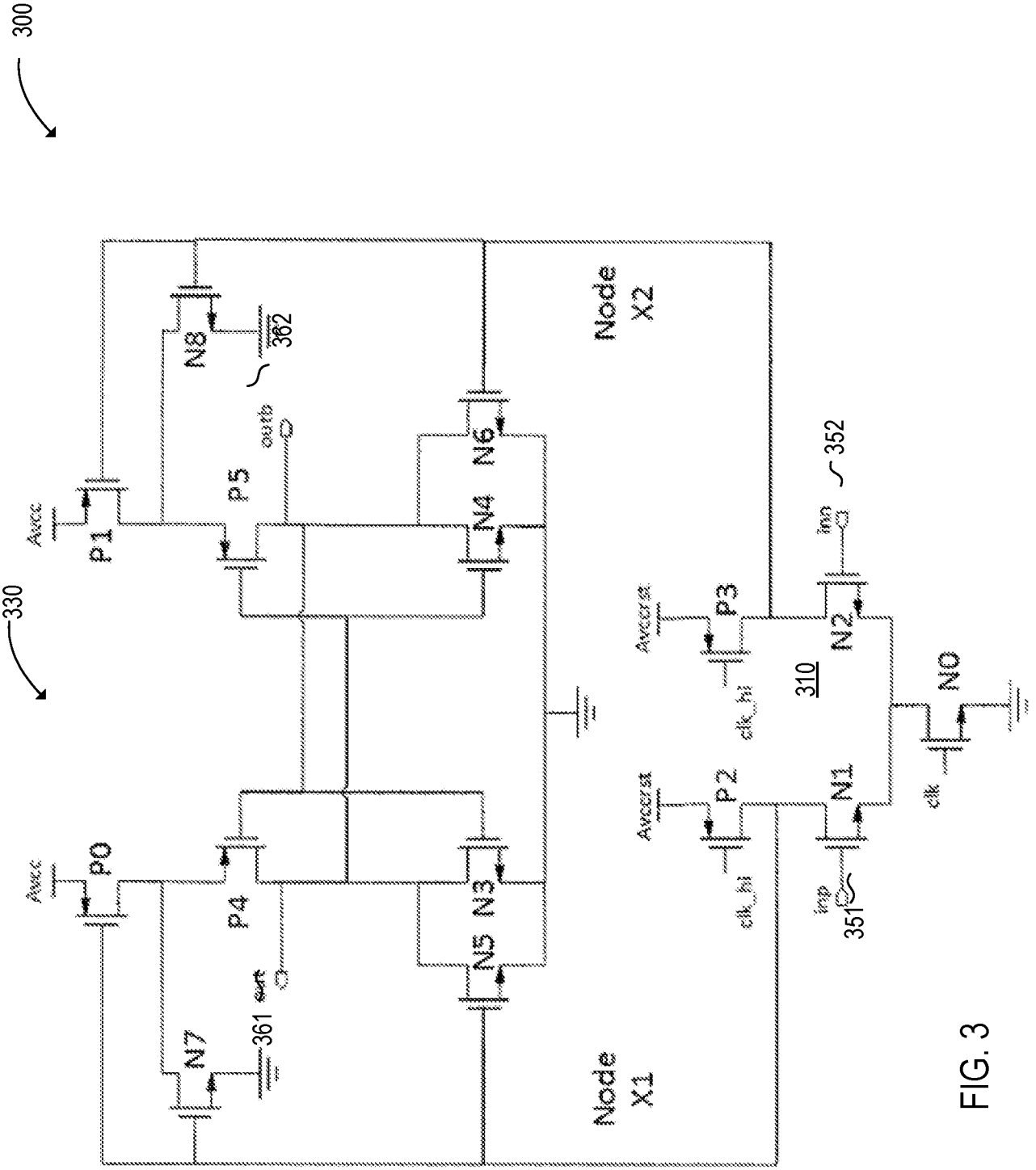
300
330
Avcc
P0
P1
P2
P3
P4
P5
N0
N1
N2
N3
N4
N5
N6
N7
N8
Avccra
clk_hi
clk
inp
inn
outb
outt
351
352
361
362
310
Node X1
Node X2

FIG. 3

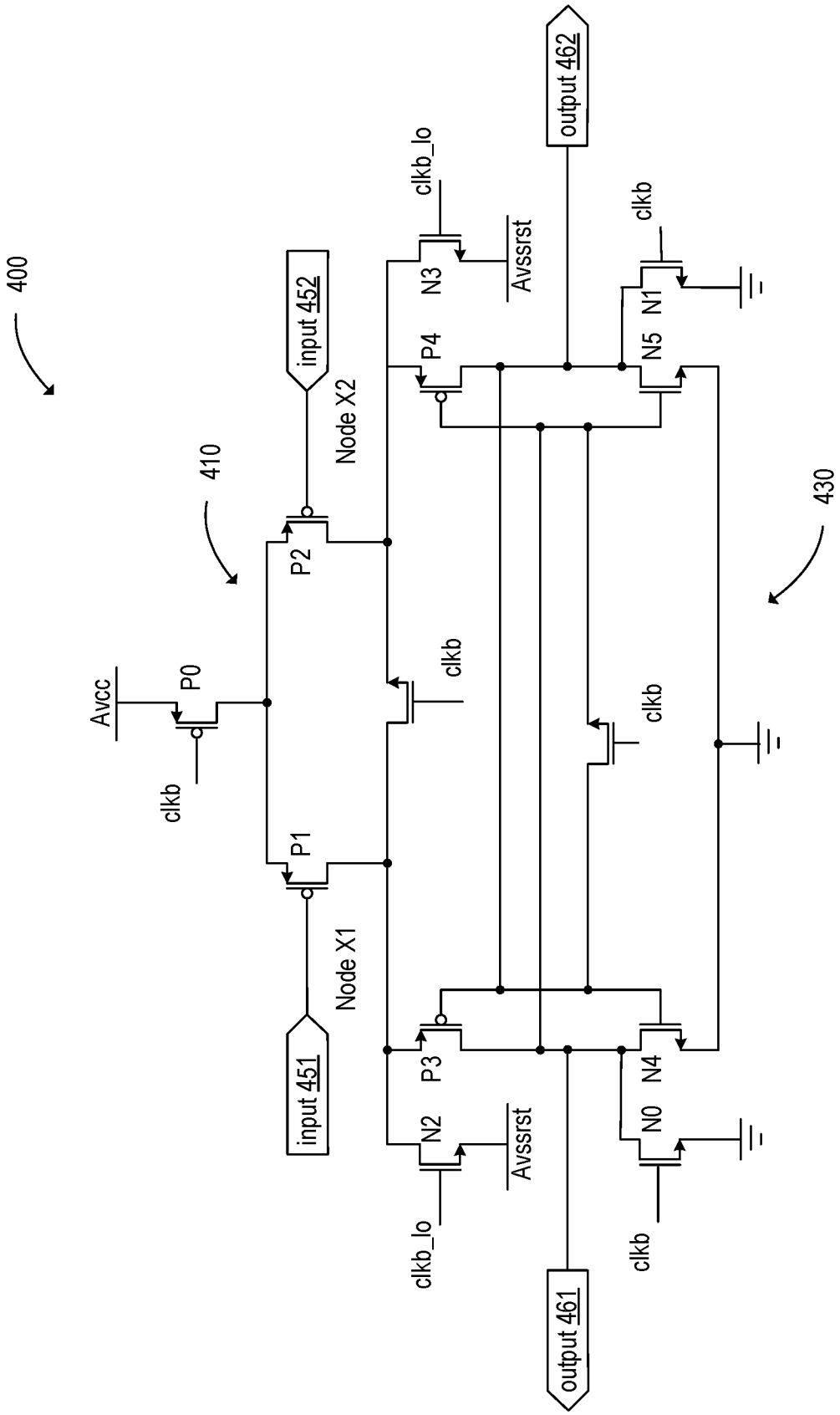
400
410
430
Avcc
P0
clkb
P1
P2
input 452
Node X2
input 451
Node X1
clkb
clkb_lo
N3
Avssrst
P4
output 462
clkb
N1
N5
clkb
P3
N2
Avssrst
clkb_lo
N4
N0
clkb
output 461

FIG. 4

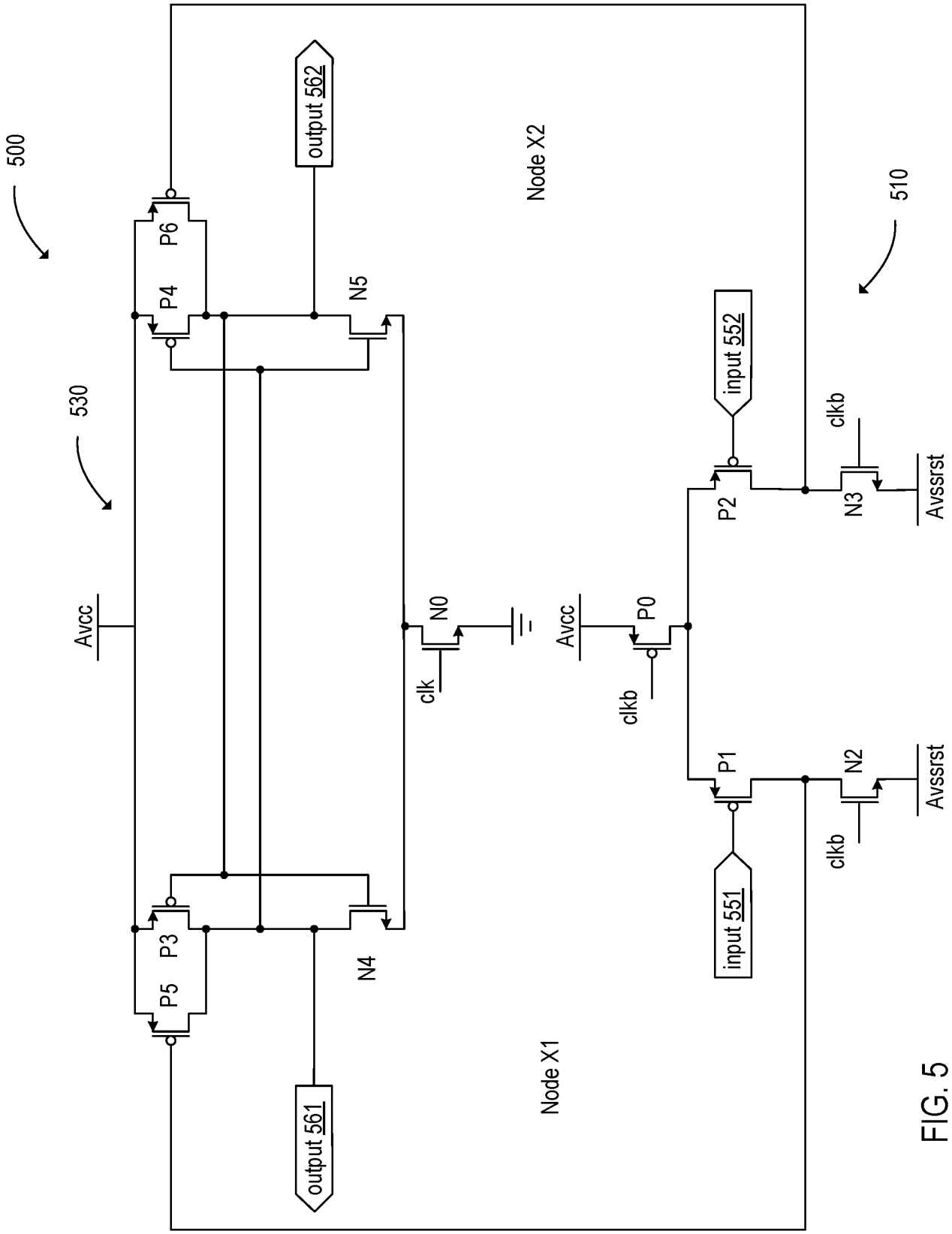
500
510
530
output 562
output 561
Node X2
Node X1
P6
P4
P3
P5
N5
N4
N0
clk
Avcc
P0
clkb
P1
P2
N2
N3
input 551
input 552
Avssrst

FIG. 5

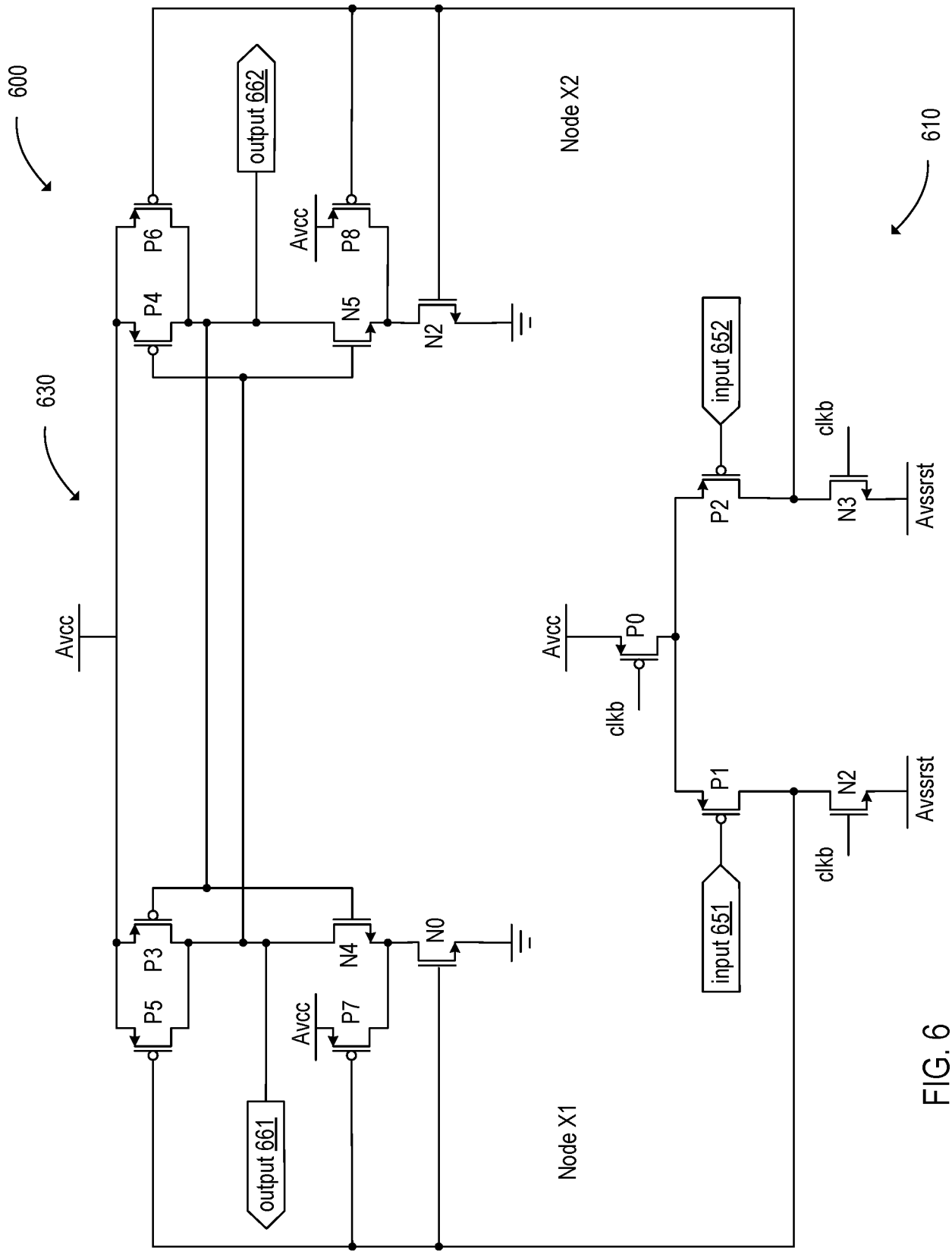
600
630
610
output 662
output 661
Node X2
Node X1
Avcc
P6
P4
P8
N5
N2
P3
P5
P7
N4
N0
input 652
input 651
P2
P1
P0
N3
N2
clkb
Avssrst

FIG. 6

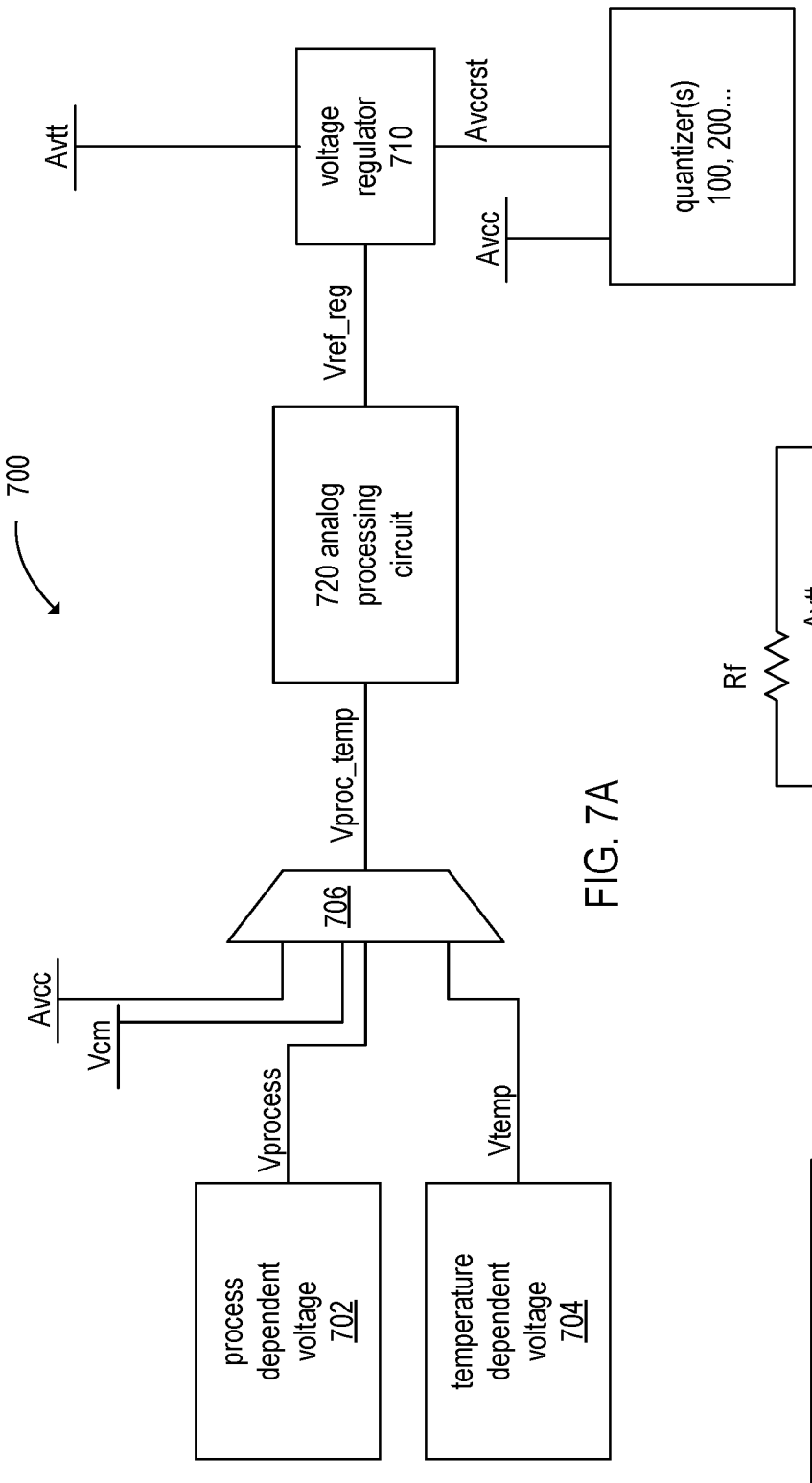
700
Avtt
voltage regulator 710
Avccrst
quantizer(s) 100, 200...
Avcc
Vref_reg
720 analog processing circuit
Vproc_temp
706
Avcc
Vcm
Vprocess
Vtemp
process dependent voltage 702
temperature dependent voltage 704

FIG. 7A

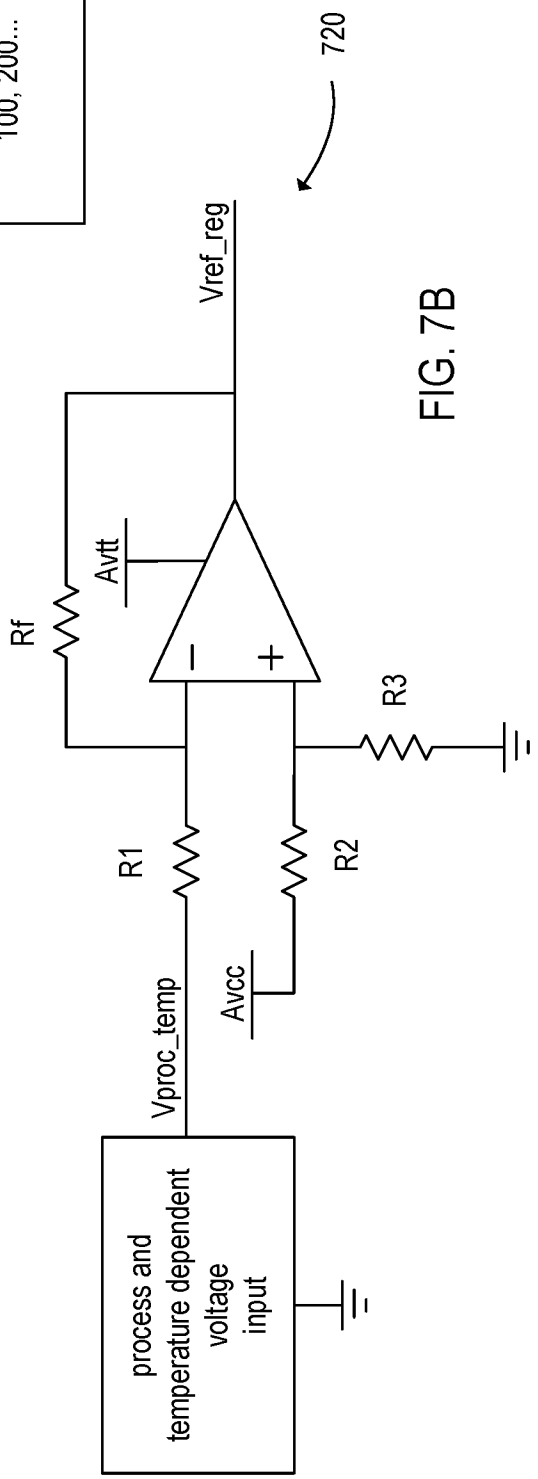
720
Vref_reg
Avtt
Rf
R3
R1
R2
Avcc
Vproc_temp
process and temperature dependent voltage input

FIG. 7B

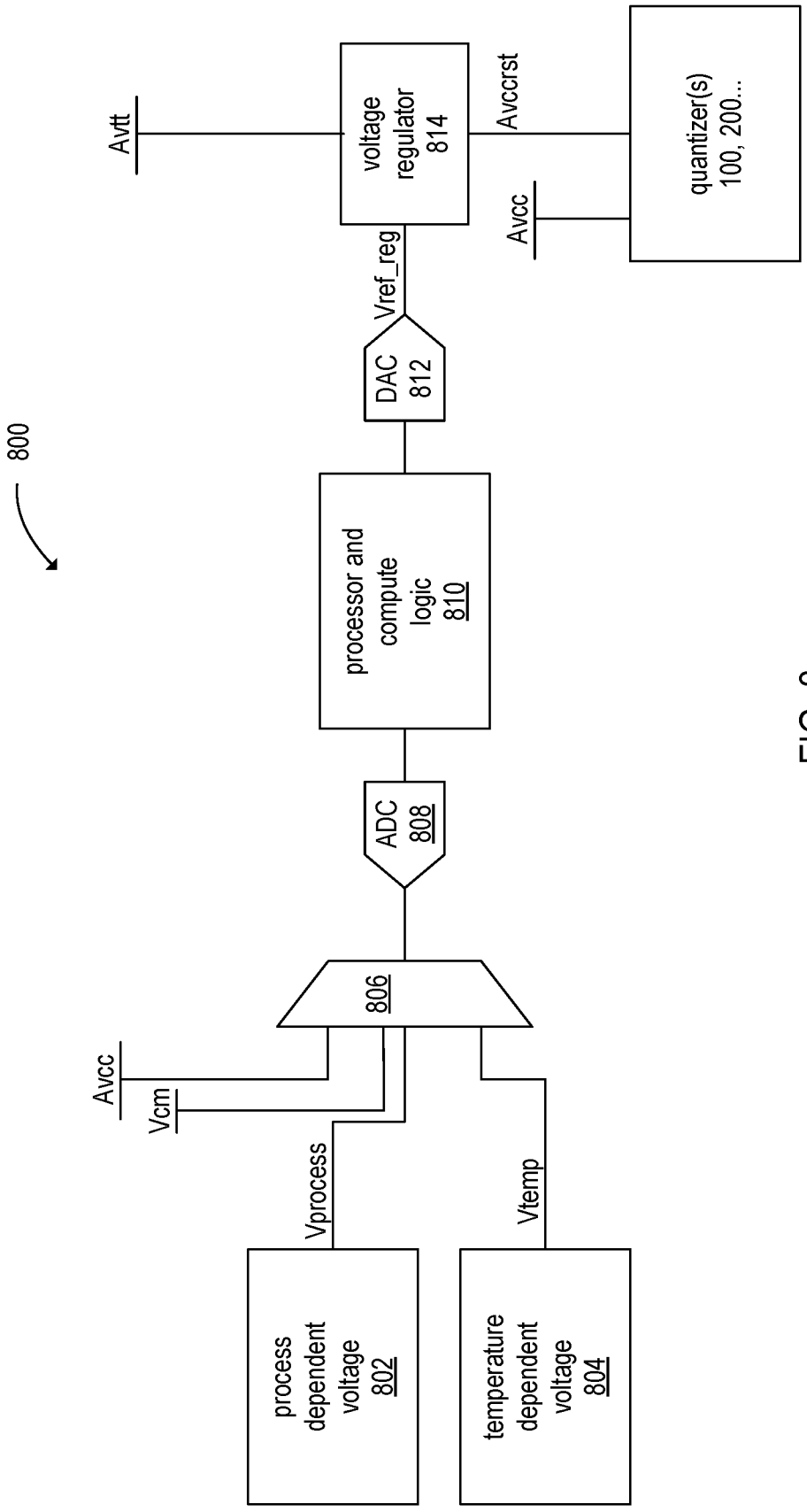
800
Avtt
voltage regulator 814
Avccrst
quantizer(s) 100, 200...
Avcc
Vref_reg
DAC 812
processor and compute logic 810
ADC 808
806
Avcc
Vcm
Vprocess
Vtemp
process dependent voltage 802
temperature dependent voltage 804

FIG. 8

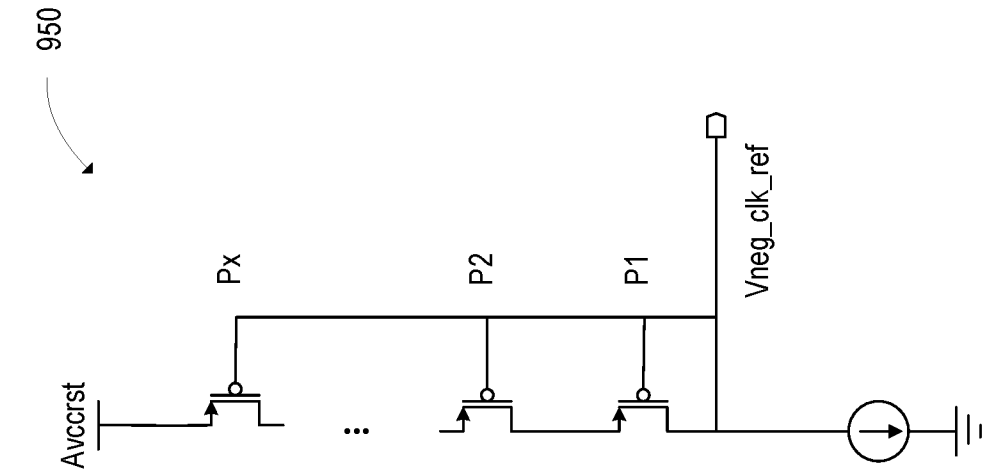

FIG. 10

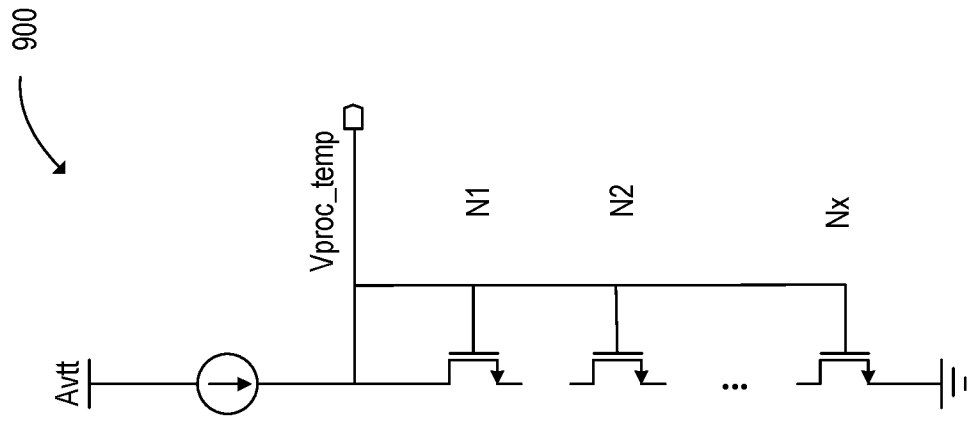

FIG. 9

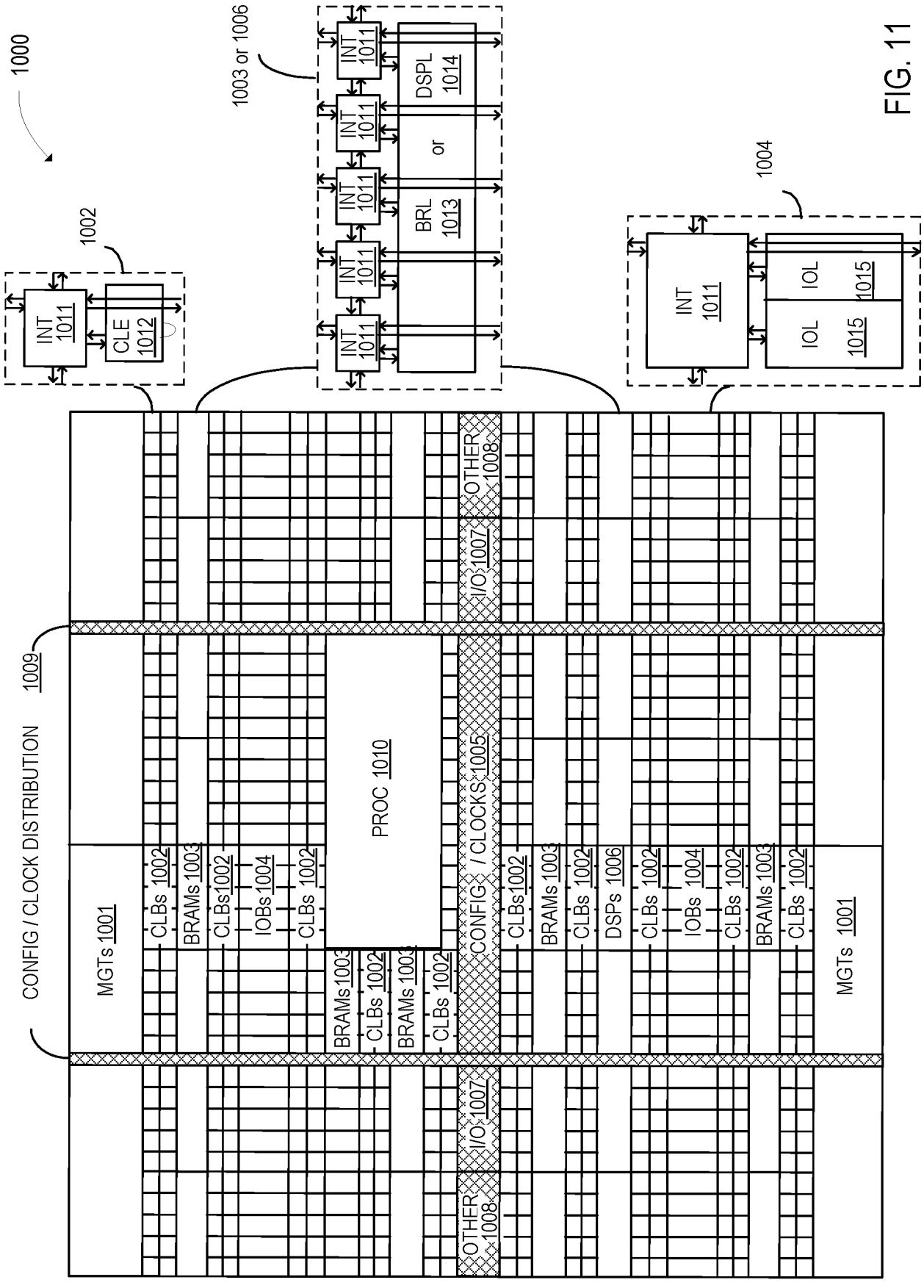
1000
1002
INT 1011
CLE 1012
1003 or 1006
INT 1011
BRL 1013
or
DSPL 1014
1004
INT 1011
IOL 1015
CONFIG / CLOCK DISTRIBUTION 1009
MGTs 1001
CLBs 1002
BRAMs 1003
IOBs 1004
PROC 1010
CONFIG / CLOCKS 1005
DSPs 1006
I/O 1007
OTHER 1008

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/018255

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K5/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 8 040 159 B1 (LALL RAVINDAR MOHAN [US]) 18 October 2011 (2011-10-18) column 4, line 26 - line 57; figures 2A,2B,2C,2D	1,2,5-8, 11-15
A	US 9 077 323 B1 (ATESOGLU ALI [US] ET AL) 7 July 2015 (2015-07-07) column 7, line 19 - column 10, line 18; figures 1,8	1,2,5-8, 11-15
A	US 6 392 449 B1 (TAFT ROBERT CALLAGHAN [DE]) 21 May 2002 (2002-05-21) column 6, line 17 - column 7, line 45; figure 5	1,2,5-8, 11-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 April 2018	26/06/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Riccio, Ettore

2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/018255

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1, 2, 5-8, 11-15

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1, 2, 5-8, 11-15

A quantizer circuit for digitizing an analog signal, comprising:an input circuit including a plurality of input field effect transistors, the input circuit being coupled to a first voltage supply that supplies an input signal at a first voltage, wherein the input circuit converts the input signal into an input current that is integrated during an input sampling phase of an active cycle of operation of the quantizer circuit; a regeneration circuit coupled to the input circuit, the regeneration circuit including a plurality of regeneration field effect transistors, the regeneration circuit being connected to a second voltage supply at a second voltage, the second voltage being different from the first voltage; anda reset circuit coupled to the input circuit and the regeneration circuit, wherein the first voltage is higher than the second voltage to reduce noise and voltage offset in the quantizer circuit or the first voltage is lower than the second voltage to improve timing performance of the quantizer circuit

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2. claims: 3, 4

A quantizer circuit for digitizing an analog signal, comprising:an input circuit including a plurality of input field effect transistors, the input circuit being coupled to a first voltage supply that supplies an input signal at a first voltage, wherein the input circuit converts the input signal into an input current that is integrated during an input sampling phase of an active cycle of operation of the quantizer circuit; a regeneration circuit coupled to the input circuit, the regeneration circuit including a plurality of regeneration field effect transistors, the regeneration circuit being connected to a second voltage supply at a second voltage, the second voltage being different from the first voltage; anda reset circuit coupled to the input circuit and the regeneration circuit, wherein:the input circuit is configured to receive a first time varying first clock signal;the input circuit is further configured to receive a second time varying clock signal; andthe magnitude of the second clock signal is generated with reference to the first clock signal

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3. claims: 9, 10

A quantizer circuit for digitizing an analog signal, comprising:an input circuit including a plurality of input field effect transistors, the input circuit being coupled to a first voltage supply that supplies an input signal at a first voltage, wherein the input circuit converts the input

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

signal into an input current that is integrated during an input sampling phase of an active cycle of operation of the quantizer circuit; a regeneration circuit coupled to the input circuit, the regeneration circuit including a plurality of regeneration field effect transistors, the regeneration circuit being connected to a second voltage supply at a second voltage, the second voltage being different from the first voltage; anda reset circuit coupled to the input circuit and the regeneration circuit, wherein:further comprising a control circuit that is configured to increase or decrease magnitude of the first voltage, wherein the control circuit includes:at least one analog-to-digital converter that is configured to receive a plurality of input signals and generate digital input signal data, wherein the input signals include signals indicative of at least one of a magnitude of the second voltage, a process dependent voltage, a magnitude of a common mode voltage, a temperature dependent voltage, or a shift voltage;a programmable integrated circuit operably coupled to the at least one analog-to-digital converter, the programmable integrated circuit being configured to process the digital input signal data to determine circuit configuration data and generate a circuit configuration data digital output signal, wherein the programmable integrated circuit is programmed with executable code for determining the configuration data; andat least one digital-to-analog converter operably coupled to the programmable integrated circuit, the at least one digital-to-analog converter being configured to convert the circuit configuration data digital output signal into the reference signal representative of the first voltage.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2018/018255

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 8040159 B1	18-10-2011	US 8040159 B1	18-10-2011
		US 8169237 B1	01-05-2012
US 9077323 B1	07-07-2015	US 8692582 B1	08-04-2014
		US 9077323 B1	07-07-2015
US 6392449 B1	21-05-2002	NONE	