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(54) Title: GATE DRIVING CIRCUIT AND DRIVING METHOD OF THE SAME, ARRAY SUBSTRATE AND DISPLAY APPARATUS

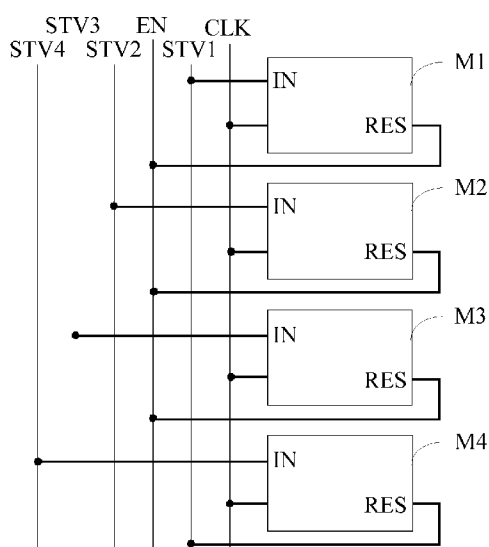


Fig. 1

(57) Abstract: A gate driving circuit, which comprises at least two scan modules (M1, M2, M3, M4) coupled to a same clock signal (CLK). Each of the at least two scan modules (M1, M2, M3, M4) may have an input terminal (IN), a reset terminal (RES), and at least one stage of shift register unit. The reset terminal (RES) of at least one of the at least two scan modules (M1, M2, M3, M4) is coupled to a touch control enable signal line (EN).



1 **[0005]** Accordingly, one example of the present disclosure is a gate driving circuit. The gate
2 driving circuit may comprise at least two scan modules coupled to a same clock signal. Each of
3 the at least two scan modules may have an input terminal, a reset terminal, and at least one stage
4 of shift register unit. The reset terminal of at least one of the at least two scan modules may be
5 coupled to a touch control enable signal line. Each of the at least two scan modules may be
6 configured to enable the at least one stage of the shift register unit thereof to output a gate
7 turning-on voltage stage by stage, starting from the first stage, in accordance with a flip of a level
8 of the clock signal when the input terminal thereof receives an active level and to stop the last
9 stage of the shift register unit thereof from outputting a gate turning-on voltage when the reset
10 terminal thereof receives an active level.

11 **[0006]** A display period the gate driving circuit corresponds to may include alternate display
12 scan periods and touch scan periods. Each of the at least two scan modules may correspond to
13 one of the display scan periods respectively. The touch control enable signal line may be
14 configured to load an active level at the reset terminal during each of the touch scan periods.
15 Each of input terminals of the at least two scan modules may be coupled to a start signal line
16 respectively.

17 **[0007]** Among the at least two scan modules other than scan modules whose reset terminals are
18 coupled to the touch control enable signal line, a reset terminal of at least a current scan module
19 may be coupled to an input terminal of a subsequent scan module. The subsequent scan module
20 is a scan module whose corresponding display scan period is most closely subsequent to a
21 display scan period the current scan module corresponds to.

22 **[0008]** A reset terminal of a scan module corresponding to a last display scan period in the
23 display period may be coupled to an input terminal of a scan module corresponding to a first
24 display scan period of a next display period.

25 **[0009]** Each of the at least one stage of the shift register unit may comprise an input terminal; an
26 output terminal; and a reset terminal. An input terminal of a first stage of shift register unit in a
27 scan module may be coupled to an input terminal of the scan module. A reset terminal of a last

1 stage of shift register unit in the scan module may be coupled to a reset terminal of the scan
2 module.

3 **[0010]** In a scan module having more than one stage of shift register units, except a first stage of
4 the shift register, an input terminal of any of the remaining stages of shift register units may be
5 coupled to an output terminal of a previous stage of shift register unit. Furthermore, except a last
6 stage of the shift register unit, a reset terminal of any of the remaining stages of shift register
7 units may be coupled to an output terminal of a next stage of shift register unit. The clock signal
8 may be provided by a first clock signal line and a second clock signal line.

9 **[0011]** Each of the at least one stage of the shift register unit may comprise a first transistor, a
10 first capacitor, a second transistor, a third transistor, a fourth transistor, and a fifth transistor. A
11 gate of the first transistor may be coupled to a first electrode of the first capacitor C1, a first
12 electrode thereof may be coupled to the first clock signal line, and a second electrode thereof
13 may be coupled to an output terminal of the shift register unit. A second electrode of the first
14 capacitor C1 may be coupled to the output terminal of the shift register unit. A gate and a first
15 electrode of the second transistor T2 may be coupled to an input terminal of the shift register unit,
16 and a second electrode thereof may be coupled to the first electrode of the first capacitor C1. A
17 gate and a first electrode of the third transistor T3 may be coupled to a reset terminal of the shift
18 register unit, and a second electrode thereof may be coupled to a gate of the fourth transistor T4
19 and a gate of the fifth transistor T5. A first electrode of the fourth transistor T4 may be coupled
20 to the output terminal of the shift register unit, and a second electrode thereof may be coupled to
21 an inactive level voltage line. A first electrode of the fifth transistor T5 may be coupled to the
22 first electrode of the first capacitor C1, and a second electrode thereof may be coupled to the
23 inactive level voltage line. The first electrode and the second electrode refer to one of a source
24 and a drain respectively.

25 **[0012]** Each of the at least one stage of the shift register unit may further comprise a sixth
26 transistor T6, a seventh transistor T7, an eighth transistor T8, a ninth transistor T9, a tenth
27 transistor T10, and an eleventh transistor T11. A gate of the sixth transistor T6 may be coupled
28 to a gate of the seventh transistor T7, a first electrode thereof may be coupled to the first

1 electrode of the first capacitor C1, and a second electrode thereof may be coupled to the inactive
2 level voltage line Vss. A first electrode of the seventh transistor T7 may be coupled to the output
3 terminal of the shift register unit, and a second electrode thereof may be coupled to the invalid
4 level voltage line Vss. A gate of the eighth transistor T8 may be coupled to a second electrode of
5 the tenth transistor T10, a first electrode of the eighth transistor T8 may be coupled to the
6 second clock signal line, and a second electrode thereof may be coupled to the gate of the sixth
7 transistor T6. A gate of the ninth transistor T9 may be coupled to the first electrode of the first
8 capacitor C1, a first electrode may be coupled to the gate of the sixth transistor T6, a second
9 electrode may be coupled to the invalid level voltage line Vss. A gate and a first electrode of the
10 tenth transistor T10 may be coupled to the second clock signal line CK2. A gate of the eleventh
11 transistor T11 may be coupled to the first electrode of the first capacitor C1, a first electrode
12 thereof may be coupled to the gate of the eighth transistor T8, and a second electrode thereof
13 may be coupled to the invalid level voltage line Vss.

14 **[0013]** In another embodiment, the gate driving circuit may comprise at least two scan modules
15 coupled to a same clock signal. Each of the at least two scan modules may have an input terminal,
16 a reset terminal, and at least one stage of shift register unit. Among the at least two scan modules,
17 a reset terminal of at least a current scan module may be coupled to an input terminal of a
18 subsequent scan module. The subsequent scan module is a scan module whose corresponding
19 display scan period is most closely subsequent to a display scan period the current scan module
20 corresponds to. Each of the at least two scan modules may be configured to enable the at least
21 one stage of the shift register unit thereof to output a gate turning-on voltage stage by stage,
22 starting from the first stage, in accordance with a flip of a level of the clock signal when the input
23 terminal thereof receives an active level and to stop the last stage of the shift register unit thereof
24 from outputting a gate turning-on voltage when the reset terminal thereof receives an active level.

25 **[0014]** Another example of the present disclosure is a driving method of the gate driving circuit
26 according to one embodiment of the present disclosure. The method may comprise providing an
27 active level to an input terminal of a scan module corresponding to a display scan period at a
28 beginning of the display scan period. The method may further comprise providing a same clock

1 signal to the at least two scan modules and having the clock signal stop flipping during each of
2 the touch scan periods. The method may further comprise providing a touch control enable signal
3 to a reset terminal of the scan module.

4 **[0015]** Another example of the present disclosure is an array substrate comprising the gate
5 driving circuit according to one embodiment of the present disclosure.

6 **[0016]** Another example of the present disclosure is a display apparatus comprising the array
7 substrate according to one embodiment of the present disclosure.

8 **BRIEF DESCRIPTION OF THE DRAWINGS**

9 **[0017]** The subject matter which is regarded as the invention is particularly pointed out and
10 distinctly claimed in the claims at the conclusion of the specification. The foregoing and other
11 objects, features, and advantages of the invention are apparent from the following detailed
12 description taken in conjunction with the accompanying drawings in which:

13 **[0018]** Fig. 1 is a block diagram of a gate driving circuit according to one embodiment of the
14 present disclosure;

15 **[0019]** Fig. 2 is a circuit timing diagram of a gate driving circuit according to one embodiment
16 of the present disclosure;

17 **[0020]** Fig. 3 is a block diagram of a gate driving circuit according to one embodiment of the
18 present disclosure.

19 **[0021]** Fig. 4 is a circuit timing diagram of a gate driving circuit according to one embodiment
20 of the present disclosure;

21 **[0022]** Fig. 5 is a circuit diagram of a shift register unit according to one embodiment of the
22 present disclosure;

23 **[0023]** Fig. 6 is a circuit timing diagram of a shift register unit according to one embodiment of
24 the present disclosure.

DETAILED DESCRIPTION

[0024] The present invention will be described in further detail with reference to the accompanying drawings and embodiments in order to provide a better understanding of the technical solutions of the present invention by those skilled in the art. Throughout the description of the invention, reference is made to Figs. 1-6. When referring to the figures, like structures and elements shown throughout are indicated with like reference numerals.

[0025] Fig. 1 is a block diagram of a gate driving circuit according to one embodiment of the present disclosure. The gate driving circuit includes at least two scan modules. The at least two scan modules are coupled to a same clock signal line. Each of the scan modules has an input terminal and a reset terminal. The reset terminal of at least one of the at least two scan modules is coupled to a touch control enable signal line. In one embodiment, as shown in Fig. 1, there are four scan modules M1, M2, M3 and M4. The four scan modules M1, M2, M3 and M4 are coupled to the same clock signal line CLK. The reset terminals RES of the scan modules M1, M2, and M3 in Fig. 1 are coupled to a touch control enable signal line EN.

[0026] In one embodiment, each of the scan modules includes at least one stage of shift register unit. The number of the stages of shift register units may be one, five, ten, twenty, or fifty, etc. The number of stages of the shift register units in different scan modules can be different. Moreover, each of the scan modules has the following function: when an input terminal of the scan module receives an active level, internal shift register units thereof start outputting a gate turning-on voltage stage by stage, starting from the first stage, in accordance with a flip of a level of the clock signal. When a reset terminal of the scan module receives an active level, the last stage of shift register unit thereof stops outputting a gate turning-on voltage.

[0027] In one embodiment, scan module M1 includes a plurality of cascaded shift register units. For each stage of the shift register unit, when a level of a clock signal flips at first time after an input terminal thereof receives a gate turning-on voltage, the stage of the shift register unit can output a gate turning-on voltage to an output terminal thereof. Furthermore, when a reset terminal thereof receives a gate turning-on voltage, the stage of the shift register unit stops outputting a gate turning-on voltage to the output terminal thereof. When an input terminal of the

1 first stage of shift register unit is coupled to an input terminal of the scan module M1 and a reset
2 terminal of the last stage of shift register unit is coupled to a reset terminal of the scan module
3 M1, the scan module M1 can achieve the above function: when an input terminal of the scan
4 module receives an active level, internal shift register units thereof start outputting a gate
5 turning-on voltage stage by stage, starting from the first stage, in accordance with a flip of a level
6 of the clock signal. Furthermore, when a reset terminal of the scan module receives an active
7 level, the last stage of the shift register unit thereof stops outputting a gate turning-on voltage.
8 The shift register unit of this embodiment can be realized with reference to a Gate driver on
9 Array (GOA) unit circuit in the prior art, and an example of its circuit structure is disclosed later.

10 **[0028]** Fig. 2 is a circuit timing diagram of a gate driving circuit according to one embodiment
11 of the present disclosure. Specifically, Fig. 2 shows a partial circuit timing diagram of scan
12 module M1 and scan module M2 according to one embodiment. A display period to which a gate
13 driving circuit of the present embodiment corresponds comprises alternate display scan periods
14 and touch scan periods such as display scan period t_{M1} , touch scan period t_{12} , and display scan
15 period t_{M2} arranged in turn as shown in Fig. 2. After this, the display period may further
16 include a plurality of alternate display scan periods and touch scan periods. Among the above at
17 least two scan modules, each of the scan modules corresponds to one of the display scan periods.
18 For example, the display scan period t_{M1} in Fig. 2 corresponds to scan module M1. The display
19 scan period t_{M2} in Fig. 2 corresponds to scan module M2. The touch control enable signal line
20 is used to load an active level signal at a reset terminal of the scan module during each of the
21 touch scan periods. For example, as shown in Fig. 2, the touch control enable signal line EN is at
22 a high level during the touch scan period t_{12} and a low level during the display scan period t_{M1}
23 and the display scan period t_{M2} .

24 **[0029]** Since the touch control enable signal line loads an active level at the reset terminal of the
25 scan module during each of the touch scan periods, for each of the scan modules whose reset
26 terminals are coupled to the touch control enable signal line, the last stage of the shift register
27 unit thereof stops outputting a gate turning-on voltage or the last stage of the shift register unit

1 thereof remains in a state of not outputting the gate turning-on voltage during each of the touch
2 scan periods.

3 **[0030]** In one embodiment, as shown in Figs. 1 and 2, scan module M1 is coupled to a start
4 signal line STV1. Scan module M2 is coupled to a start signal line STV2. Scan module M3 is
5 coupled to a start signal line STV3. Scan module M4 is coupled to a start signal line STV4. Each
6 of the start signal lines is coupled to a scan control signal respectively. As such, touch scans and
7 display scans can be performed alternately in accordance with the following procedure:

8 **[0031]** As shown in Fig. 2, at the beginning of display scan period t_{M1} , the start signal line
9 STV1 outputs an active level to the input terminal of scan module M1. As a result, during
10 display scan period t_{M1} , internal shift register units of scan module M1 start outputting a gate
11 turning-on voltage stage by stage, starting from the first stage, in accordance with a flip of a level
12 of the clock signal, until an output terminal Gn of the last stage of shift register unit thereof starts
13 outputting a gate turning-on voltage. Then, at the beginning of the subsequent touch scan period
14 t_{12} , scan module M1 stops the last stage of the internal shift register unit thereof from outputting
15 a gate turning-on voltage under an action of the active level of the touch control enable signal
16 line EN. Accordingly, the output terminal Gn outputs a waveform as shown in Fig. 2. The active
17 level of the touch control enable signal line EN continues until the end of the touch scan period
18 t_{12} . Thereafter, at the beginning of display scan period t_{M2} , the start signal line STV2 outputs
19 an active level to the input terminal of scan module M2. As a result, during display scan period
20 t_{M2} , internal shift register units of scan module M2 start outputting a gate turning-on voltage
21 stage by stage, starting from the first stage, in accordance with a flip of a level of a clock signal.
22 Accordingly, the output terminal Gn + 1 of the first stage of the shift register unit of scan module
23 M2 outputs a waveform as shown in Fig 2. Likewise, the last stage of shift register unit of scan
24 module M2 stops outputting a gate turning-on voltage under an action of an active level of the
25 touch control enable signal line EN at the end of the display scan period t_{M2} . Then, scan
26 module M3 starts outputting a gate turning-on voltage stage by stage at the beginning of the
27 corresponding display scan period under an action of the start signal line STV3. The last stage of
28 the shift register unit of scan module M3 stops outputting a gate turning-on voltage under an

1 action of an active level on the touch control enable signal line EN at the end of the
2 corresponding display scan period. Then, scan module M4 starts outputting a gate turning-on
3 voltage stage by stage at the beginning of the corresponding display scan period under an action
4 of the start signal line STV4. The last stage of the shift register unit of scan module M4 stops
5 outputting a gate turning-on voltage under an action of the start signal line STV1 of the next
6 display period at the end of the corresponding display scan period. As such, touch scans and
7 display scans are performed alternately.

8 **[0032]** It can be seen that a reset terminal of at least one of the at least two scan modules is
9 coupled to a touch control enable signal line. As such, at least a part of control signal lines can be
10 replaced by the touch control enable signal line commonly used in a touch control circuits. As a
11 result, this part of the control signal lines can be saved, which can not only reduce the number of
12 signal ports, but also compress a part of wiring space, thereby facilitating simplifying circuit
13 structure of a product and narrowing display borders.

14 **[0033]** The active and inactive levels herein refer to two different pre-configured ranges of
15 voltages against a particular circuit node respectively. Both ranges of the voltages are based on a
16 voltage of common terminal. For example, active levels of all circuit nodes are high levels in the
17 digital circuit. Alternatively, active levels of all circuit nodes are low levels in the digital circuit.
18 Alternatively, active levels of reset terminals of scan modules are high levels in the digital circuit
19 and active levels of input terminals of scan modules are low levels in the digital circuit. This is
20 not limited hereto.

21 **[0034]** In one embodiment, the above-described touch control enable signal line refers to a touch
22 signal line commonly used in a touch control circuit. Typically, periods of an active level of the
23 touch control enable signal line are completely coincident with all touch scan periods. As such,
24 the touch control enable signal line can be used to distinguish and identify touch scan periods
25 and non-touch scan periods. In another embodiment, a signal on a touch control enable signal
26 line is a signal obtained after processing a signal of the touch control signal line. For example, a
27 touch control enable signal line is a signal line coupled to a touch control signal line via a voltage
28 follower. Alternatively, a touch control enable signal line is a signal line coupled to a touch

1 control signal line via a step-up conversion circuit. This is not limited hereto. In addition, in one
2 embodiment, the touch control enable signal line may be coupled to reset terminals of any
3 number or any combination of scan modules among the at least two scan modules included in the
4 gate driving circuit. The more the number of connected scan modules is, the more conducive to
5 reduce the number of signal ports and compress the wiring space.

6 **[0035]** Fig. 3 shows a block diagram of a gate driving circuit according to one embodiment of
7 the present disclosure. The gate driving circuit of the present embodiment includes at least two
8 scan modules. The at least two scan modules are coupled to a same clock signal. Each scan
9 module has an input terminal and a reset terminal. The input terminal of each of the at least two
10 scan modules is coupled to a start signal line respectively. In addition, a reset terminal of at least
11 one of the at least two scan modules is coupled to an input terminal of a subsequent scan module.
12 In one embodiment as shown in Fig. 3, a gate driving circuit includes four scan modules M1, M2,
13 M3 and M4. The four scan modules M1, M2, M3 and M4 are coupled to the same clock signal
14 line CLK. Furthermore, an input terminal IN of scan module M1 is coupled to a start signal line
15 STV1. An input terminal IN of scan module M2 is coupled to a start signal line STV2. An input
16 terminal IN of scan module M3 is coupled to a start signal line STV3. An input terminal IN of
17 scan module M4 is coupled to a start signal line STV4. In addition, a reset terminal RES of scan
18 module M1 is coupled to an input terminal IN of scan module M2. A reset terminal RES of scan
19 module M2 is coupled to an input terminal IN of scan module M3. A reset terminal RES of scan
20 module M3 is coupled to an input terminal IN of scan module M4. A reset terminal RES of scan
21 module M4 is coupled to an input terminal IN of scan module M1.

22 **[0036]** In one embodiment, each of the scan modules includes at least one stage of shift register
23 unit. The number of the stages of shift register units may be one, five, ten, twenty, or fifty, etc.
24 The number of stages of the shift register units in different scan modules can be different.
25 Moreover, each of the scan modules has the following function: when an input terminal of the
26 scan module receives an active level, internal shift register units thereof start to output a gate
27 turning-on voltage stage by stage, starting from the first stage, in accordance with a flip of a level

1 of the clock signal. When a reset terminal of the scan module receives an active level, the last
2 stage of shift register unit thereof stops outputting a gate turning-on voltage.

3 **[0037]** In one embodiment, a scan module M1 includes a plurality of cascaded shift register units.
4 For each stage of the shift register unit, when a level of a clock signal flips at the first time after
5 an input terminal thereof receives a gate turning-on voltage, the stage of the shift register unit
6 can output a gate turning-on voltage to an output terminal thereof. Furthermore, when a reset
7 terminal thereof receives a gate turning-on voltage, the stage of the shift register unit stops
8 outputting a gate turning-on voltage to the output terminal thereof. When an input terminal of the
9 first stage of shift register unit is coupled to an input terminal of the scan module M1 and a reset
10 terminal of the last stage of shift register unit is coupled to a reset terminal of the scan module
11 M1, the scan module M1 can achieve the following function: when an input terminal of the scan
12 module receives an active level, internal shift register units thereof start outputting a gate
13 turning-on voltage stage by stage, starting from the first stage, in accordance with a flip of a level
14 of the clock signal. Furthermore, when a reset terminal of the scan module receives an active
15 level, the last stage of the shift register unit thereof stops outputting a gate turning-on voltage.
16 The shift register unit of this embodiment can be realized with reference to a Gate driver on
17 Array (GOA) unit circuit in the prior art, and an example of its circuit structure is disclosed later.

18 **[0038]** Fig. 4 is a circuit timing diagram of a gate driving circuit according to one embodiment
19 of the present disclosure. Specifically, Fig. 4 shows partial circuit timing diagram of scan module
20 M1, scan module M2 and scan module M3. A display period to which the gate driving circuit of
21 the present embodiment corresponds includes alternate display scan periods and touch scan
22 periods. As shown in Fig. 4, the display period includes display scan period t_M1, touch scan
23 period t12, display scan period t_M2, touch scan period t23, display scan period t_M3, which are
24 arranged in turn. The display period may further include a plurality of alternate display scan
25 periods and touch scan periods after those shown in Fig. 4. Among the above at least two scan
26 modules, each of the scan modules corresponds to a display scan period. For example, as shown
27 in Fig. 4, display scan period t_M1 corresponds to scan module M1. Display scan period t_M2
28 corresponds to scan module M2. Display scan period t_M3 corresponds to scan module M3. For

1 each of the scan modules of the present embodiment, a subsequent scan module of a current scan
2 module is one whose corresponding display scan period is closely subsequent to the
3 corresponding display scan period of the current scan module. That is, a reset terminal of each of
4 the scan modules is coupled to a start signal line respectively. For two scan modules coupled to a
5 same start signal line, a display scan period corresponding to a scan module whose reset terminal
6 is coupled to the same start signal line and a display scan period corresponding to a scan module
7 whose input terminal is coupled to the same start signal line are disposed immediately before and
8 after a same touch scan period respectively, or disposed as the last display scan period of a
9 display period and the first display scan period of the next display period respectively. For
10 example, as shown in Fig. 4, for scan module M2 that corresponds to display scan period t_{M2} ,
11 display scan period t_{M3} is most closely subsequent to display scan period t_{M2} . Thus, the scan
12 module M3 corresponding to scan period t_{M3} is the subsequent scan module of scan module
13 M2. Furthermore, the display scan period corresponding to scan module M4 is the last display
14 scan period of the display period, and its most closely subsequent display scan period is the first
15 display scan period of the next display period, that is, the display scan period t_{M1} which
16 corresponds to scan module M1. Therefore the subsequent scan module of scan module M4 is
17 scan module M1.

18 **[0039]** As shown in Figs. 3 and 4, In a case where each of the start signal lines is coupled to a
19 scan control signal respectively, alternate touch scans and display scans can be performed using
20 the following method:

21 **[0040]** As shown in Fig. 4, at the beginning of display scan period t_{M1} , a start signal line STV1
22 outputs an active level to an input terminal of scan module M1. As a result, scan module M1
23 enables internal shift register units thereof to output a gate turning-on voltage stage by stage,
24 starting from the first stage, in accordance with a flip of a level of a clock signal in the
25 corresponding display scan period t_{M1} , until an output terminal Gn of the last stage of the shift
26 register unit starts outputting a gate turning-on voltage. Then, at the beginning of a subsequent
27 touch scan period t_{12} , the voltage line for providing the gate turning-on voltage temporally stops
28 providing the gate turning-on voltage. As such, the output terminal Gn does not output a gate

1 turning-on voltage during the touch scan period t_{12} . Thereafter, at the beginning of a display
2 scan period t_{M2} , a start signal line STV2 outputs an active level to both an input terminal of
3 scan module M2 and a reset terminal of scan module M1. As a result, the last stage of the shift
4 register unit of the scan module M1 stops outputting a gate turning-on voltage. Accordingly, the
5 output terminal G_n outputs a waveform as shown in Fig. 4. Under an action of an active level of
6 the start signal line STV2, scan module M2 enables its internal shift register units to output a
7 gate turning-on voltage stage by stage, starting from the first stage, in accordance with a flip of a
8 level of a clock signal in the corresponding display scan period t_{M2} . For example, an output
9 terminal G_{n+1} of the first stage of the shift register unit of scan module M2 outputs a waveform
10 as shown in Fig. 4. Likewise, an output terminal G_{2n} of the last stage of the shift register unit of
11 scan module M2 does not output a gate turning-on voltage during touch scan period t_{23} . The
12 output terminal G_{2n} stops outputting a gate turning-on voltage under an action of an active level
13 of the start signal line STV2 at the beginning of the display scan period t_{M3} . Accordingly, a
14 waveform as shown in Fig. 4 is formed. At the beginning of the display scan period t_{M3} , scan
15 module M3 starts outputting a gate turning-on voltage stage by stage under an action of the start
16 signal line STV3. For example, an output terminal G_{2n+1} of the first stage of shift register unit
17 of scan module M3 outputs a waveform as shown in Fig 4. At the beginning of the display scan
18 period corresponding to scan module M4, the last stage of shift register unit of scan module M3
19 stops outputting a gate turning-on voltage under an action of an active level on the start signal
20 line STV4. Scan module M4 starts outputting a gate turning-on voltage stage by stage under an
21 action of the start signal line STV4 at the beginning of the corresponding display scan period. At
22 the beginning of the display scans period t_{M1} , the last stage of the shift register unit of scan
23 module M4 stops outputting a gate turning-on voltage under an action of an active level of the
24 start signal line STV1 of the next display period. As a result, touch scans and display scans are
25 performed alternately.

26 **[0041]** It can be seen that a reset terminal of at least one of the at least two scan modules is
27 coupled to an input terminal of the subsequent scan module thereof. The embodiment of the
28 present disclosure can reduce the number of control signal lines by sharing a part of control

1 signal lines. It can not only reduce the number of signal ports, but also compress a part of wiring
2 space, thereby facilitating simplifying circuit structure of a product and narrowing display
3 borders.

4 **[0042]** The active and inactive levels herein refer to two different pre-configured ranges of
5 voltages against a particular circuit node respectively. Both ranges of the voltages are based on a
6 voltage of common terminal. For example, active levels of all circuit nodes are high levels in the
7 digital circuit. Alternatively, active levels of all circuit nodes are low levels in the digital circuit.
8 Alternatively, active levels of reset terminals of scan modules are high levels in the digital circuit
9 and active levels of input terminals of scan modules are low levels in the digital circuit. This is
10 not limited hereto.

11 **[0043]** It is to be noted that among the at least two scan modules included in the gate driving
12 circuit, there may be any number or combination of scan modules whose reset terminals are
13 coupled to an input terminal of a subsequent scan module respectively. The more the number of
14 scan modules whose reset terminals are coupled to the input terminal of the subsequent scan
15 module respectively, the more the number of signal ports is reduced and the more wiring space is
16 compressed.

17 **[0044]** In another embodiment, a gate driving circuit includes at least two scan modules. A reset
18 terminal of at least one of the at least two scan modules is coupled to a touch control enable
19 signal line. A reset terminal of at least one of the at least two scan modules other than scan
20 modules whose reset terminals are coupled to the touch control enable signal line is coupled to
21 an input terminal of the subsequent scan module thereof. As such, a combination of the above
22 two methods can reduce the number of the control signal lines. This can not only reduce the
23 number of signal ports, but also compress a part of wiring space, thereby facilitating simplifying
24 circuit structure of a product and narrowing display borders.

25 **[0045]** In another embodiment, a gate driving circuit includes at least two scan modules. Input
26 terminals of the at least two scan modules are coupled to start signal lines respectively. A reset
27 terminal of the scan module corresponding to the last display scan period in the display period is
28 coupled to an input terminal of the scan module corresponding to the first display scan period in

1 the display period. As shown in Fig. 1 and Fig. 4, a reset terminal RES of scan module M4
2 corresponding to the last display scan period in the display period is coupled to an input terminal
3 IN of scan module M1 corresponding to the first display scan period in the display period. As
4 such, the signal line coupled to the input terminal of the first scan module corresponding to the
5 first scan period in the display period can be utilized to reset the scan module corresponding to
6 the last display scan period in the previous display period. As a result, the number of the control
7 signal lines can be further reduced. This can not only reduce the number of signal ports, but also
8 compress a part of the wiring space, thereby facilitating simplifying circuit structure of a product
9 and narrowing display borders.

10 **[0046]** In one embodiment, in any of the above-described gate driving circuits, a shift register
11 unit included in the scan module may have an input terminal, an output terminal, and a reset
12 terminal. An input terminal of the first stage of the shift register unit of each scan module is
13 coupled to an input terminal of the scan module. A reset terminal of the last stage of shift register
14 unit of each scan module is coupled to a reset terminal of the scan module. Furthermore, in a
15 scan module having more than one stage of shift register units, except the first stage of the shift
16 register unit, an input terminal of any of the remaining stages of shift register units is coupled to
17 an output terminal of the previous stage of shift register unit. Except the last stage of shift
18 register unit, a reset terminal of any of the remaining stages of shift register units is coupled to
19 the output terminal of the next stage of shift register unit. As such, the function of the above-
20 described scan module can be realized according to the above-described examples of the shift
21 register units.

22 **[0047]** Fig. 5 shows a circuit diagram of a shift register unit according to one embodiment of the
23 present disclosure. Fig. 6 shows a circuit timing diagram corresponding to the shift register unit.
24 In one embodiment, the clock signals include positive phase clock signals and inverted phase
25 clock signals provided by first clock signal line CK1 and second clock signal line CK2
26 respectively. The first clock signal line CK1 of the shift register unit which is coupled to an odd
27 numbered scan line is loaded with a positive phase clock signal. The second clock signal line
28 CK2 thereof is loaded with an inverted phase clock signal. The first clock signal line CK1 of the

1 shift register unit which is coupled to an even numbered scan line is loaded with the inverted
2 clock signal. The second clock signal line CK2 thereof is loaded with the positive phase clock
3 signal. In one embodiment, the transistors shown in Fig. 5 are all N-type transistors, which can
4 be manufactured by a same production method to lower manufacturing cost. According to the
5 specific type of transistors, connections for the source and the drain thereof can be set
6 respectively to match a direction of a current flowing through the transistor. When a transistor
7 has a structure in which the source and the drain thereof are symmetrical, the source and the
8 drain can be regarded as two electrodes that are not specifically differentiated. Hereinafter, a first
9 electrode and a second electrode denote one of the source and the drain respectively.

10 **[0048]** As shown in Fig. 5, the shift register unit includes a first transistor T1, a first capacitor C1,
11 a second transistor T2, a third transistor T3, a fourth transistor T4, and a fifth transistor T5. A
12 gate of the first transistor T1 is coupled to a first node PU. A first electrode thereof is coupled to
13 a first clock signal line CK1. A second electrode thereof is coupled to an output terminal GO of
14 the shift register unit. The first and the second electrodes are one of the source and the drain
15 respectively. A first electrode of the first capacitor C1 is coupled to the first node PU. A second
16 electrode thereof is coupled to the output terminal GO of the shift register unit. A gate and a first
17 electrode of the second transistor T2 are coupled to an input terminal GI of the shift register unit.
18 A second electrode thereof is coupled to the first node PU. A gate and a first electrode of the
19 third transistor T3 are coupled to a reset terminal GR of the shift register unit. A second electrode
20 thereof is coupled to a gate of the fourth transistor T4 and a gate of the fifth transistor T5. A first
21 electrode of the fourth transistor T4 is coupled to the output terminal GO of the shift register unit.
22 A second electrode thereof is coupled to an inactive level voltage line Vss. A first electrode of
23 the fifth transistor T5 is coupled to the first node PU, and a second electrode thereof is coupled to
24 the inactive level voltage line Vss.

25 **[0049]** With a combination of the first transistor T1, the first capacitor C1, the second transistor
26 T2, the third transistor T3, the fourth transistor T4, and the fifth transistor T5, the shift register
27 unit can start outputting a gate turning-on voltage to the output terminal GO thereof when an
28 voltage level of the first clock signal flips at the first time after the input terminal GI thereof

1 receives a gate turning-on voltage. The shift register unit can stop outputting a gate turning-on
2 voltage to the output terminal GO thereof when the reset terminal GR receives a gate turning-on
3 voltage.

4 **[0050]** In another embodiment, as shown in Fig. 5, the shift register unit further includes a sixth
5 transistor T6, a seventh transistor T7, an eighth transistor T8, a ninth transistor T9, a tenth
6 transistor T10, and an eleventh transistor T11. A gate of the sixth transistor T6 is coupled to a
7 second node PD. A first electrode thereof is coupled to the first node PU, a second electrode
8 thereof is coupled to the invalid level voltage line Vss. A gate of the seventh transistor T7 is
9 coupled to the second node PD. A first electrode thereof is coupled to the output terminal GO of
10 the shift register unit. A second electrode thereof is coupled to the invalid level voltage line Vss.
11 A gate of the eighth transistor T8 is coupled to a third node PC. A first electrode of the eighth
12 transistor T8 is coupled to the second clock signal line CK2, and a second electrode thereof is
13 coupled to the second node PD. A gate of the ninth transistor T9 is coupled to the first node PU.
14 A first electrode thereof is coupled to the second node PD, a second electrode thereof is coupled
15 to the invalid level voltage line Vss. A gate and a first electrode of the tenth transistor T10 are
16 coupled to the second clock signal line CK2. A second electrode thereof is coupled to the third
17 node PC. A gate of the eleventh transistor T11 is coupled to the first node PU. A first electrode
18 thereof is coupled to the third node PC and a second electrode thereof is coupled to the invalid
19 level voltage line Vss.

20 **[0051]** With a combination of the sixth transistor T6, the seventh transistor T7, the eighth
21 transistor T8, the ninth transistor T9, the tenth transistor T10, and the eleventh transistor T11, the
22 shift register unit can fulfill the above function with additional advantages such as less output
23 noise and better operating stability.

24 **[0052]** Referring to Figs. 5 and 6, an operational principle of the above shift register unit is
25 described as follows:

26 **[0053]** Prior to a first stage ①, the input terminal GI and the reset terminal GR of the shift
27 register unit are maintained at a low level. Thus, the second transistor T2, the third transistor T3,
28 the fifth transistor T5, and the fourth transistor T4 remain turned off. The clock signals on the

1 first clock signal line CK1 and the second clock signal line CK2 flip periodically so that the tenth
2 transistor T10 turns on periodically and the third node PC is set at a high level periodically. Then,
3 the eighth transistor T8 is turned on so that the second node PD is set at a high level. Under an
4 action of the high level of the second node PD, the sixth transistor T6 and the seventh transistor
5 T7 are turned on so that the first node PU and the output terminal GO remain at a low level. The
6 ninth transistor T9 and the eleventh transistor T11 remain turned off so that potentials of the
7 second node PD and the third node PC are not pulled down. The first transistor T1 remains
8 closed so that the potential at the output terminal GO is not pulled up.

9 **[0054]** During the first stage ①, the input terminal GI is changed to be at a high level. The
10 second clock signal line CK2 is at a high level, and the first clock signal line CK1 is at a low
11 level. As such, the second transistor T2 is turned on so that the first node PU is pulled up to a
12 high level. As a result, the first transistor T1, the ninth transistor T9, and the eleventh transistor
13 T11 are turned on. The second node PD and the third node PC are set at a low level, and the
14 potentials of the first node PU and the output terminal GO are stopped being pulled down. Since
15 the first transistor T1 is turned on, the output terminal GO remains at the low level under an
16 action of the first clock signal line CK1. During this stage, the first terminal of the first capacitor
17 C1 is at a high level and the second terminal thereof is at a low level. That is, charging of both
18 terminals of the capacitor is completed during this stage.

19 **[0055]** During the second stage ②, the input terminal GI is changed to be at a low level. The
20 second clock signal line CK2 is at a low level and the first clock signal line CK1 is at a high
21 level. Under an action of charge retention effect of the first capacitor C1, the first node PU jumps
22 to a level higher than a high potential as the first clock signal line CK1 changes from a low level
23 to a high level. As such, the first transistor T1 is fully turned on and the potential at the output
24 terminal GO is pulled up quickly. That is, the output terminal GO starts outputting a gate
25 turning-on voltage.

26 **[0056]** During the third stage ③, the reset terminal GR is changed to be at a high level. The
27 second clock signal line CK2 is at the high level. The first clock signal line CK1 is at the low
28 level. Under an action of the high level at the reset terminal GR, the third transistor T3 is turned

1 on. As such, the fifth transistor T5 pulls down the potential at the first node PU. The fourth
2 transistor T4 pulls down the potential at the output terminal GO. As a result, the first node PU is
3 set at a low level. Furthermore, the ninth transistor T9 stops pulling down the potential at the
4 second node PD. The eleventh transistor T11 stops pulling down the potential at the third node
5 PC. Under an action of a high level on the second clock signal line CK2, the tenth transistor T10
6 is turned on and the third node PC is set at a high level. Then, the eighth transistor T8 is turned
7 on and the second node PD is set at a high level. After that, under an action of the high level of
8 the second node PD, the sixth transistor T6 and the seventh transistor T7 are turned on and
9 accordingly the first node PU and the output terminal GO are set at a low level. That is,
10 outputting of the gate turning-on voltage is stopped. Thereafter, the shift register unit continues
11 to be in a state as prior to the first stage ① until the first stage of next period starts.

12 **[0057]** As can be seen from the above principle of operation, the shift register unit starts
13 outputting a gate turning-on voltage to the output terminal GO thereof when the level of the
14 clock signal flips at the first time after the input terminal GI thereof receives a gate turning-on
15 voltage. Furthermore, the shift register unit stops outputting a gate turning-on voltage to the
16 output terminal GO thereof when the reset terminal GR receives a gate turning-on voltage.
17 Moreover, the shift register unit has a certain capability in resisting noise and maintaining the
18 output signal stable. Thus, any one of the above-described scan modules and any of the above-
19 described gate driving circuits can be formed using, for example, the shift register unit according
20 to one embodiment.

21 **[0058]** Based on the same inventive concept, in one embodiment, a driving method for the gate
22 driving circuit according to one embodiment of the present disclosure is provided. The driving
23 method includes: at the beginning of any of the display scan periods, the input terminal of the
24 scan module corresponding to the display scan period is set at an active level. As such, an
25 operational timing of the gate driving circuit shown in Fig. 2 or Fig. 4 can be realized. In
26 addition, the driving method of the present embodiment may further include: providing the same
27 clock signal to the at least two scan modules, and having the clock signal temporarily stop
28 flipping during each of the touch scan periods. As a result, during each of the touch scan periods,

1 outputting of the gate turning-on voltage stage by stage is suspended. The suspension of
2 provision of the gate turning-on voltage during each of the above-mentioned touch scan periods
3 can be realized in conjunction with the circuit structure shown in Fig 5.

4 **[0059]** Based on the same inventive concept, in another embodiment, an array substrate is
5 provided. The array substrate includes the gate driving circuit according to one embodiment of
6 the present disclosure. It is possible to reduce the number of control signal lines for achieving
7 alternation of touch scans and display scans in any of the above-described gate driving circuits so
8 that the gate driving circuit has simpler circuit structure and smaller footprint thereof. As a result,
9 the array substrate can have a smaller GOA region so that it is possible for the array substrate to
10 achieve at least one of the following: increasing display area, reducing a size of the array
11 substrate, and narrowing borders.

12 **[0060]** Based on the same inventive concept, in another embodiment, a display apparatus is
13 provided. The display apparatus includes any of the array substrates according to one
14 embodiment of the present disclosure. The display apparatus in the embodiment of the present
15 disclosure may be a display panel, a mobile phone, a tablet computer, a television, a monitor, a
16 notebook computer, a digital photo frame, a navigator, or any product or component having
17 display capability. It can be seen that, based on any of the above-described gate driving circuits
18 and any of the above-described array substrates and the features thereof, it is possible for the
19 display apparatus to achieve at least one of the following advantages: increasing screen area,
20 reducing panel size and narrowing borders.

21 The descriptions of the various embodiments of the present disclosure have been presented for
22 purposes of illustration, but are not intended to be exhaustive or limited to the embodiments
23 disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art
24 without departing from the scope and spirit of the described embodiments. The terminology used
25 herein was chosen to best explain the principles of the embodiments, the practical application or
26 technical improvement over technologies found in the marketplace, or to enable others of
27 ordinary skill in the art to understand the embodiments disclosed herein.

28

CLAIMS

1
2 What is claimed is:

3 1. A gate driving circuit comprising:

4 at least two scan modules coupled to a same clock signal, each of the at least two
5 scan modules having an input terminal, a reset terminal, and at least one stage of shift
6 register unit,

7 wherein the reset terminal of at least one of the at least two scan modules is
8 coupled to a touch control enable signal line, and

9 wherein each of the at least two scan modules is configured to enable the at least
10 one stage of the shift register unit thereof to output a gate turning-on voltage stage by
11 stage, starting from the first stage, in accordance with a flip of a level of the clock signal
12 when the input terminal thereof receives an active level and to stop the last stage of the
13 shift register unit thereof from outputting a gate turning-on voltage when the reset
14 terminal thereof receives an active level.

15 2. The gate driving circuit according to claim 1, wherein a display period the gate driving
16 circuit corresponds to includes alternate display scan periods and touch scan periods, and
17 each of the at least two scan modules corresponds to one of the display scan periods
18 respectively, and

19 wherein the touch control enable signal line is configured to load an active level at
20 the reset terminal during each of the touch scan periods.

21 3. The gate driving circuit according to any one of claim 1 and claim 2, wherein each of
22 input terminals of the at least two scan modules is coupled to a start signal line
23 respectively.

24 4. The gate driving circuit according to any one of claims 1-3, wherein among the at least
25 two scan modules other than scan modules whose reset terminals are coupled to the touch
26 control enable signal line, a reset terminal of at least a current scan module is coupled to
27 an input terminal of a subsequent scan module;

- 1 wherein the subsequent scan module is a scan module whose corresponding
2 display scan period is most closely subsequent to a display scan period the current scan
3 module corresponds to.
- 4 5. The gate driving circuit according to claim 4, a reset terminal of a scan module
5 corresponding to a last display scan period in the display period is coupled to an input
6 terminal of a scan module corresponding to a first display scan period of a next display
7 period.
- 8 6. The gate driving circuit according to any one of claims 1 to 5, wherein each of the at least
9 one stage of the shift register unit comprises:
10 an input terminal;
11 an output terminal; and
12 a reset terminal;
- 13 wherein an input terminal of a first stage of shift register unit in a scan module is
14 coupled to an input terminal of the scan module; and a reset terminal of a last stage of
15 shift register unit in the scan module is coupled to a reset terminal of the scan module.
- 16 7. The gate driving circuit according to claim 6, wherein in a scan module having more than
17 one stage of shift register units, except a first stage of the shift register, an input terminal
18 of any of the remaining stages of shift register units is coupled to an output terminal of a
19 previous stage of shift register unit, and
20 except a last stage of the shift register unit, a reset terminal of any of the
21 remaining stages of shift register units is coupled to a output terminal of a next stage of
22 shift register unit.
- 23 8. The gate driving circuit according to any one of claims 1-7, wherein the clock signal is
24 provided by a first clock signal line and a second clock signal line.
- 25 9. The gate driving circuit according to any one of claims 1-8, wherein each of the at least
26 one stage of the shift register unit comprises a first transistor, a first capacitor, a second
27 transistor, a third transistor, a fourth transistor, and a fifth transistor, wherein

1 a gate of the first transistor is coupled to a first electrode of the first capacitor C1,
2 a first electrode thereof is coupled to the first clock signal line, a second electrode thereof
3 is coupled to an output terminal of the shift register unit,

4 a second electrode of the first capacitor C1 is coupled to the output terminal of
5 the shift register unit;

6 a gate and a first electrode of the second transistor T2 are coupled to an input
7 terminal of the shift register unit, and a second electrode thereof is coupled to the first
8 electrode of the first capacitor C1 ;

9 a gate and a first electrode of the third transistor T3 are coupled to a reset
10 terminal of the shift register unit, and a second electrode thereof is coupled to a gate of
11 the fourth transistor T4 and a gate of the fifth transistor T5;

12 a first electrode of the fourth transistor T4 is coupled to the output terminal of the
13 shift register unit, and a second electrode thereof is coupled to an inactive level voltage
14 line; and

15 a first electrode of the fifth transistor T5 is coupled to the first electrode of the
16 first capacitor C1, and a second electrode thereof is coupled to the inactive level voltage
17 line,

18 wherein the first electrode and the second electrode refer to one of a source and a
19 drain respectively.

20 10. The gate driving circuit according to claim 9, wherein each of the at least one stage of the
21 shift register unit further comprises a sixth transistor T6, a seventh transistor T7, an
22 eighth transistor T8, a ninth transistor T9, a tenth transistor T10, and an eleventh
23 transistor T11,

24 wherein a gate of the sixth transistor T6 is coupled to a gate of the seventh
25 transistor T7, a first electrode thereof is coupled to the first electrode of the first capacitor
26 C1, a second electrode thereof is coupled to the inactive level voltage line Vss;

1 a first electrode of the seventh transistor T7 is coupled to the output terminal of
2 the shift register unit, and a second electrode thereof is coupled to the invalid level
3 voltage line Vss;

4 a gate of the eighth transistor T8 is coupled to a second electrode of the tenth
5 transistor T10, a first electrode of the eighth transistor T8 is coupled to the second clock
6 signal line, and a second electrode thereof is coupled to the gate of the sixth transistor T6 ;

7 a gate of the ninth transistor T9 is coupled to the first electrode of the first
8 capacitor C1, a first electrode is coupled to the gate of the sixth transistor T6, a second
9 electrode is coupled to the invalid level voltage line Vss;

10 a gate and a first electrode of the tenth transistor T10 are coupled to the second
11 clock signal line CK2, and

12 a gate of the eleventh transistor T11 is coupled to the first electrode of the first
13 capacitor C1, a first electrode thereof is coupled to the gate of the eighth transistor T8,
14 and a second electrode thereof is coupled to the invalid level voltage line Vss.

15 11. A driving method of the gate driving circuit according to any one of claims 1 to 10,
16 comprising:

17 providing an active level to an input terminal of a scan module corresponding to
18 a display scan period at a beginning of the display scan period.

19 12. The driving method according to claim 11, further comprising:

20 providing a same clock signal to the at least two scan modules; and

21 having the clock signal stop flipping during each of the touch scan periods

22 13. The driving method according to claim 11, further comprising:

23 providing a touch control enable signal to a reset terminal of the scan module.

24 14. An array substrate comprising the gate driving circuit according to any one of claims 1 to
25 10.

26
27 15. A display apparatus comprising the array substrate according to claim 14.

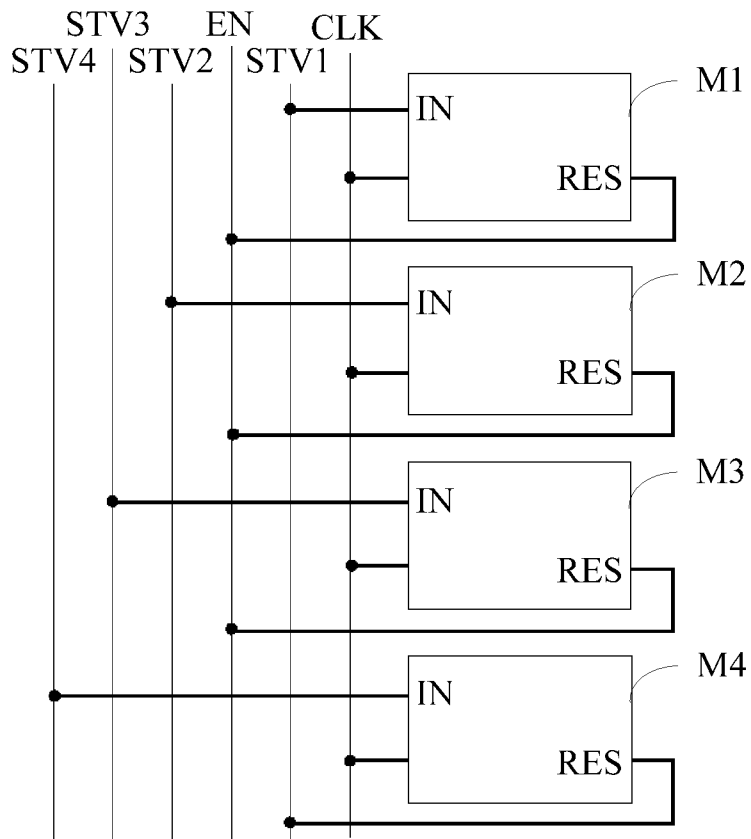


Fig. 1

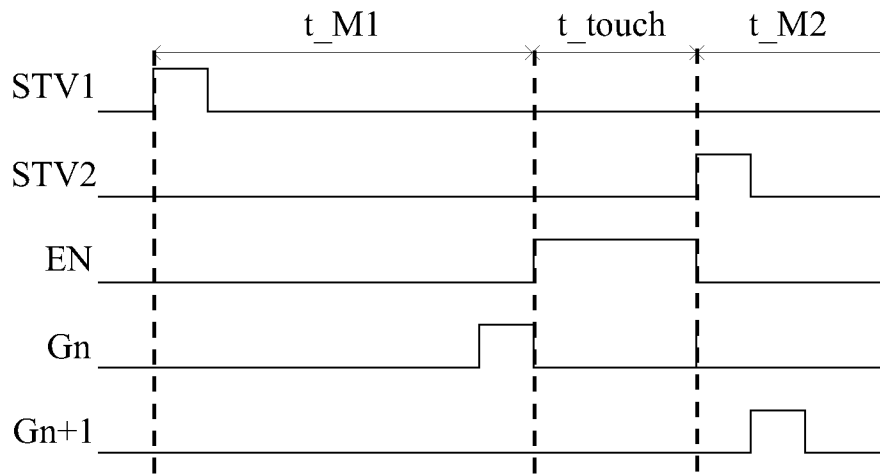


Fig. 2

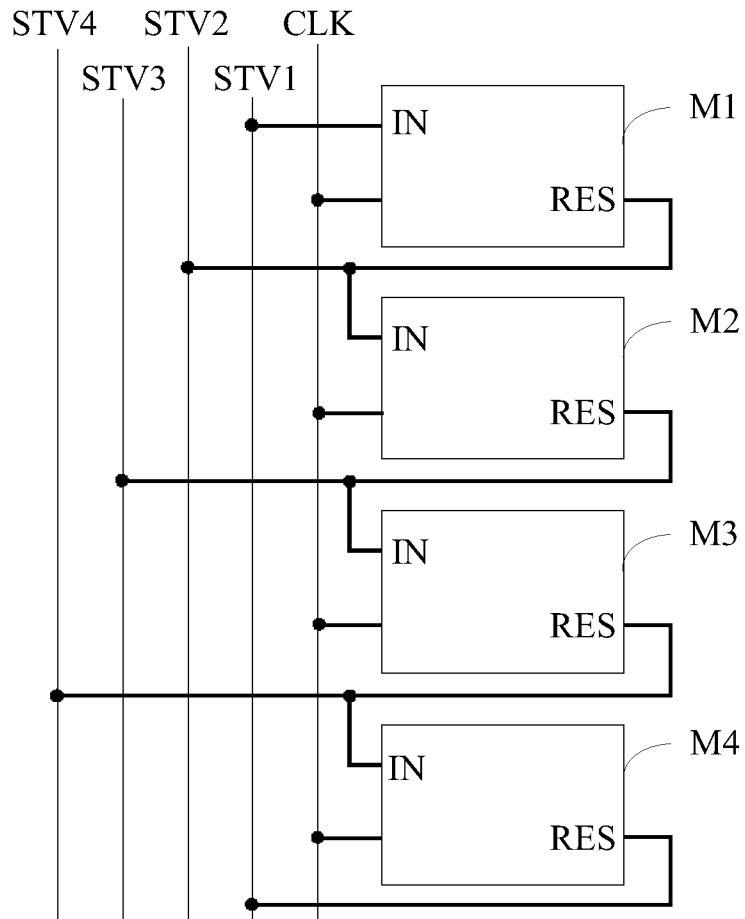


Fig. 3

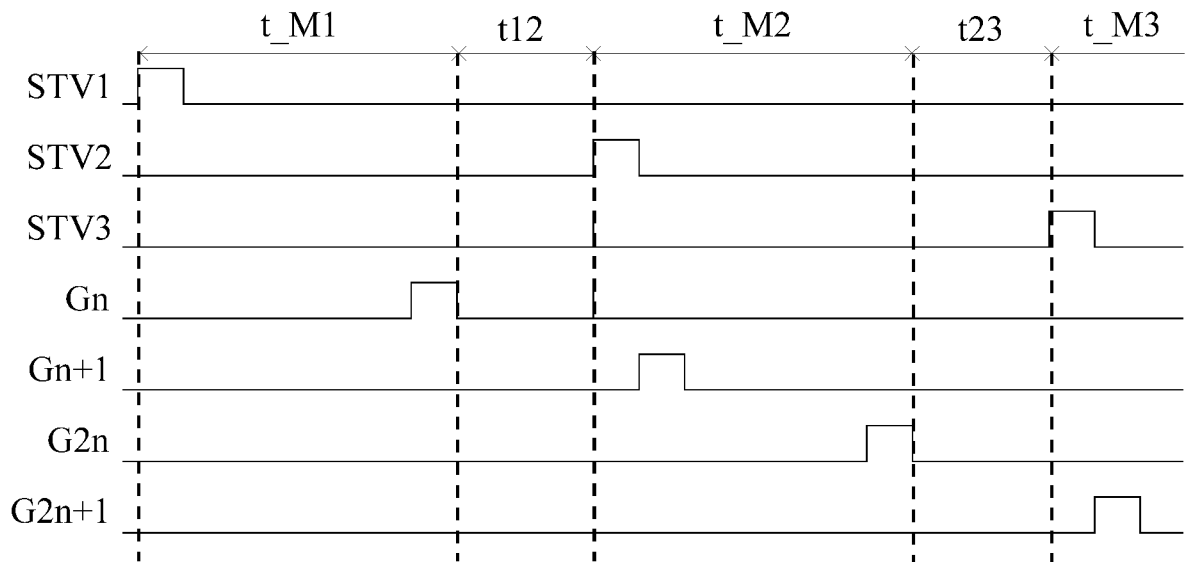


Fig. 4

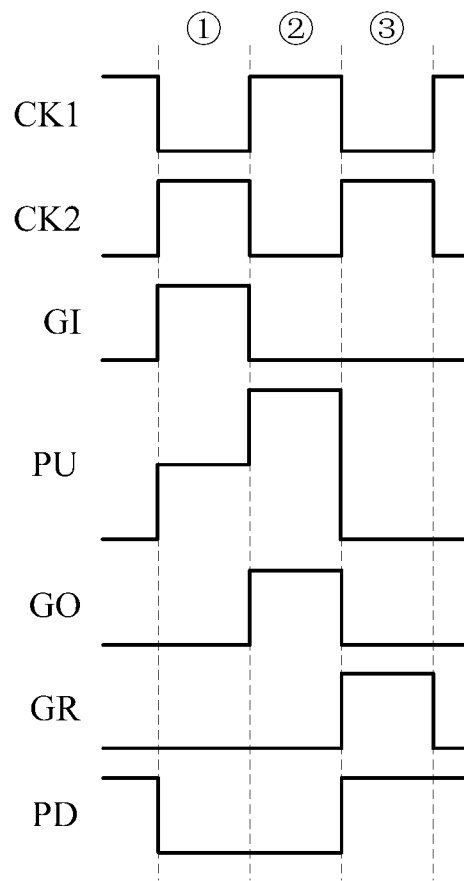


Fig. 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2017/093318

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/32(2016.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G; G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, WPI, EPODOC: display, shift, register, gate, GOA, touch+, scan+, start, STV, STV2, clock, CLK, CK, reset+, RES, RST, enable, EN, stage, group, narrow, border

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 104537994 A (SHENZHEN CHINA STAR OPTOELECTRONICS TECH.) 22 April 2015 (2015-04-22) claims 1-10, description paragraphs [0063]-[0094], figures 1, 2, 8	1-15
A	CN 203673454 U (BOE TECHNOLOGY GROUP CO., LTD.) 25 June 2014 (2014-06-25) the whole document	1-15
A	CN 104240631 A (BOE TECHNOLOGY GROUP CO., LTD.) 24 December 2014 (2014-12-24) the whole document	1-15
A	CN 106326859 A (BOE TECHNOLOGY GROUP CO., LTD.) 11 January 2017 (2017-01-11) the whole document	1-15
A	JP 2007183192 A (SEIKO EPSON CORP.) 19 July 2007 (2007-07-19) the whole document	1-15
A	JP 2011085680 A (EPSON IMAGING DEVICES CORP.) 28 April 2011 (2011-04-28) the whole document	1-15

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

17 January 2018

Date of mailing of the international search report

29 January 2018

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2017/093318

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				WO	2016106926	A1	07 July 2016
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				US	9727162	B2	08 August 2017
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