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(54) IMPROVEMENTS IN OR RELATING TO PHASE-CONTROLLED OSCILLATOR CIRCUITS

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company, of Berlin and Munich, Federal Republic of Germany, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement: —

This invention relates to phase-controlled oscillator circuits, and is particularly but not exclusively concerned with phase-controlled oscillator circuits which are particularly suited for use with so-called displacement pick-ups in non-mechanical printers.

It is known for example from German Specification No. 2 512 349 to use, as a so-called displacement pick-up for the production of electrical timing signals at times at which predetermined points of a path of travel are passed, a light-transmissive rod which is arranged along the path of travel and has marks at the levels of the predetermined points, and a light beam which is directed onto the light-transmissive rod and is influenced by the marks in such manner that it falls onto a detector whose output signals constitute the timing signals.

If such a pick-up is used, for example, in a non-mechanical printer which, employing a laser beam, effects a recording upon the surface of a recording drum, a part of the actual main recording beam produces the timing pulses required to record upon one row with the aid of the pick-up.

The dimensions of the pick-up cause the timing pulses to be produced with large intervals therebetween, and it is necessary to produce from the pulse train frequency of the timing pulses a frequency-multiplied and regulated pulse train. Such pulse train production can be carried out for example using a phase-controlled oscillator circuit as described in U.S. Patent Specification No. 3 705 361.

When such a phase-controlled oscillator circuit is employed in association with a displacement pick-up as described above, gaps are formed in the produced pulse train when the recording and scanning beam which serves to scan the displacement pick-up returns from the end of the recording process to the beginning. A pulse gap of this kind can, for example, constitute 20% of the time of the total, horizontal cycle of the scanning beam. Therefore it is necessary to compensate in a suitable manner for the breakdown of the pulse train frequency during this gap.

According to this invention there is provided a phase-controlled oscillator circuit comprising an oscillator which serves to emit timing pulses, a frequency divider arranged to frequency-divide the timing pulses to produce frequency-divided pulses, a phase comparator arranged to compare the phase of the frequency-divided pulses with the phase of synchronising pulses supplied thereto and to cause the frequency of the timing pulses emitted by the oscillator to be controlled in dependence upon the phase comparison result, and means for interrupting the supply of the frequency-divided pulses to the phase comparator during an interruption in the synchronising pulses.

Preferably said means comprises a bistable stage, an AND element having an output connected to an input of the phase comparator for the frequency-divided pulses, one input connected to an output of the frequency divider, and another input connected to an output of the bistable stage, and a pulse counter and decoder which are responsive to the synchronising pulses to set the bistable stage to a state in which the AND element is blocked in response to an anticipated interruption in the synchronising pulses and to reset the

bistable stage to a state in which the AND element is enabled in response to a recurrence of the synchronising pulses.

Expediently the frequency divider is presettable and means are provided to preset the frequency divider in accordance with the phase state of the synchronising pulses relative to the frequency-divided pulses on the recurrence of the synchronising pulses following an interruption.

Such a phase-controlled oscillator circuit is particularly suited to being synchronised by synchronising pulses supplied by a displacement pick-up, and in the event of an interruption in the synchronising pulses continues to produce the timing pulses having the desired frequency. With presetting of the frequency divider in accordance with the likely phase state of the displacement pick-up synchronising pulses relative to the frequency-divided pulses, on the recurrence of the synchronising pulses disturbing build-up processes which would otherwise be likely to occur are avoided.

The invention will be further understood from the following description by way of example with reference to the accompanying drawing, in which: —

Fig. 1 schematically illustrates a known phase-controlled oscillator circuit; and

Fig. 2 schematically illustrates a phase-controlled oscillator circuit in accordance with an embodiment of the invention.

The known circuit illustrated in Fig. 1 comprises a phase comparator 1, a subsequently connected low-pass filter consisting of a resistor R1 and a capacitor C1, a voltage-controlled oscillator 2 which emits timing pulses F3, and a frequency divider 3 which produces timing pulses F2, by frequency division of the timing pulses F3, and supplies these to one input of the phase comparator 1. The phase comparator 1 compares the phase state of input timing pulses F1 with the phase state of the timing pulses F2 and, in dependence thereupon, modifies the voltage across the capacitor C1 and thereby controls the frequency at which the oscillator 2 produces the timing pulses F3.

If such a circuit is used in association with a displacement pick-up such as is described in German Specification No. 2 512 349, the timing pulses from which constitute the timing pulses F1, the production of the timing pulses F3 is impeded in that the timing pulses F1 exhibit gaps which are formed by the return of the scanning beam which moves along the light-transmissive, e.g. glass, rod at the end of each scan; these pulse gaps constitute about 20% of the overall time.

To compensate for the interruptions in the timing pulses F1 the phase-controlled oscillator circuit illustrated in Fig. 2 is used in place of that illustrated in Fig. 1. The circuit illustrated in Fig. 2 comprises a phase comparator 1, a low-pass filter formed by a resistor R1 and a capacitor C1, an impedance buffer 8, a voltage-controlled oscillator 2, a frequency divider 3)/1, an AND gate 7, a bit pattern generator B, a binary counter 4, a decoder 6, a bistable stage 5, and a differentiator 9. Commencing with the beginning of each scan, the timing pulses F1 supplied by the displacement pick-up are counted by the counter 4. At this time the stage 5 is in a state in which an enabling signal is supplied to the gate 7, so that the timing pulses F3 are synchronised by the timing pulses F1 as in the circuit illustrated in Fig. 1. On the occurrence of the last timing pulse F1 before a gap, the decoder 6 responds to the count in the counter 4 and causes the state of the stage 5 to change so that the gate 7 is blocked. Thus the phase comparaor 1 is no longer supplied with pulses of the timing pulse train F2, the timing pulses F1 also being discontinued. As a result the phase comparator 1 maintains the voltage across the capacitor C1 constant so that during the gap in the timing pulses F1 the frequency of the timing pulses F3 is also maintained substantially constant. Discharge of the capacitor C1 into the oscillator 2 during the gap in the pulses F1 is reduced by the presence of the impedance buffer 8.

Thus the frequency of the timing pulses F3 is maintained at a steady level during the gap in the pulses F1, and the timing pulses F3 have the requisite frequency when the timing pulses F1 are again emitter by the displacement pick-up at the end of the gap. The first such pulse F1 causes the stage 4 to return to its original state so that the AND gate 7 is again enabled to conduct the pulses F2 to the phase comparator 1.

In order to avoid disturbing build-up processes which would otherwise occur as a result of the different phase states of the timing pulses F2 and the displacement pick-up pulses F1, and would produce fluctuations in the frequency of the timing pulses F3, the frequency divider 3/1 is a presettable frequency divider such as is commercially available for example under the designation SN 74193 from Texas Instruments. The frequency divider 3/1 is preset, to an empirically determined value supplied by the bit pattern generator B, in response to a pulse being supplied via the differentiator 9 and a lead 10 to a "load" input of the frequency divider 3/1 when the stage 5 returns to the state in which the gate 7 is enabled. The empirically determined value supplied by the generator B is fundamentally dependent upon the dis-

charge of the capacitor C1 during the gap in the timing pulses F1, and is arranged to be such that with the first pulse F1 following the gap in these pulses the frequency divider 3/1 supplies the timing pulses F2 with the same phase state as the pulses F1.

WHAT WE CLAIM IS:—

1. A phaselcontrolled oscillator circuit comprising an oscillator which serves to emit timing pulses, a frequency divider arranged to frequency-divide the timing pulses to produce frequency-divided pulses, a phase comparator arranged to compare the phase of the frequency-divided pulses with the phase of synchronising pulses supplied thereto and to cause the frequency of the timing pulses emitted by the oscillator to be controlled in dependence upon the phase comparison result, and means for interrupting the supply of the frequency-divided pulses to the phase comparator during an interruption in the synchronising pulses.

2. A circuit as claimed in Claim 1 wherein said means comprises a bistable stage, an AND element having an output connected to an input of the phase comparator for the frequency-divided pulses, one input connected to an output of the frequency divider, and another input connected to an output of the bistable stage, and a pulse counter and decoder which are responsive to the synchronising pulses to set the bistable stage to a state in which the AND element is blocked in response to an anticipated interruption in the synchronising pulses and to reset the bistable stage to a state in which the AND element is enabled in response to a recurrence of the synchronising pulses.

3. A circuit as claimed in Claim 1 or Claim 2 wherein the frequency divider is presettable and means are provided to preset the frequency divider in accordance with the phase state of the synchronising pulses relative to the frequency-divided pulses on the recurrence of the synchronising pulses following an interruption.

4. A phase-controlled oscillator circuit substantially as herein described with reference to Fig. 2 of the accompanying drawing.

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1 SHEET This drawing is a reproduction of the Original on a reduced scale

Fig.1

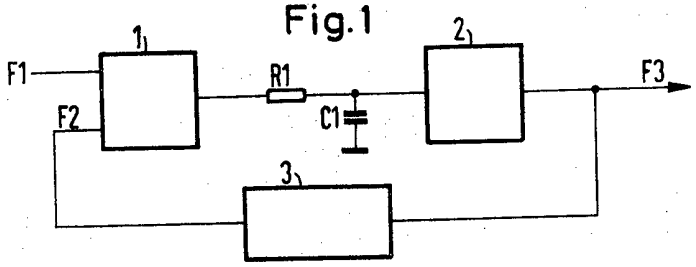

Fig.2