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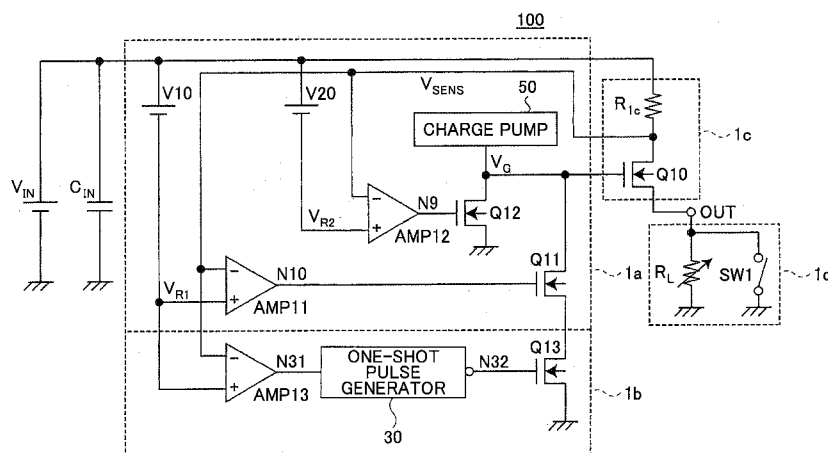
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(54) Title: CURRENT LIMITING CIRCUIT

FIG.3



(57) Abstract: A current limiting circuit includes a limit current setting unit that sets a value of a limit current for limiting an output current from a driver circuit connected to the current limiting circuit, the limit current value including a first acceptable value and a second acceptable value larger than the first acceptable value; an excess current detecting unit that detects when the output current from the driver circuit exceeds the first acceptable value; and a limit current adjusting unit that replaces the first acceptable value with the second acceptable value in a period when the output current detected by the excess current detecting unit exceeds the first acceptable value.

DESCRIPTION

TITLE OF THE INVENTION

CURRENT LIMITING CIRCUIT

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TECHNICAL FIELD

The present invention relates to a current limiting circuit for an apparatus for driving a load.

10 BACKGROUND ART

In a system in which an external apparatus, such as a portable music player or a digital camera, is connected to a host apparatus, such as a personal computer or a car navigation apparatus, the external
15 apparatus may be supplied with electric power from the host apparatus via a connector. Normally, a power switch IC with a protection function is provided immediately upstream of the connector in order to protect a power supply of the host apparatus
20 from any abnormality in the external apparatus. For example, in case the power supply line of the external apparatus connected to the host apparatus is short-circuited to ground (GND), the host apparatus limits the current supply to a constant current of
25 600 mA, using the power switch IC. At the same time,

error information is sent to the host apparatus system. In this case, an average current that can be supplied to a normal external apparatus may be 500 mA at maximum in accordance with a standard
5 specification.

FIG. 1 is a circuit diagram of a driver circuit and a current limiting circuit in a host apparatus according to related art. Specifically, the circuits include a driver circuit 201, an
10 inverter circuit, and an operational amplifier 202. The driver circuit 201 includes a sense resistor and a N-ch (channel) power MOSFET Q0. The operational amplifier 202 includes a charge pump circuit 50 that produces a voltage (such as 8 V) exceeding a power
15 supply voltage and a N-ch transistor Q1.

FIG. 2 illustrates operation waveforms at various parts of the circuits of FIG. 1. V_{R1} is set to limit an output current when it exceeds 600 mA. When a load is connected that requires a current flow
20 of 900 mA from an output OUT in a period between $t1$ and $t4$, an output current I_{OUT} starts increasing at time $t1$ and a sense voltage V_{SENS} decreases. When the output current I_{OUT} reaches 600 mA at $t2$, the sense voltage V_{SENS} decreases to V_{R1} , at which the
25 operational amplifier 202 is operated, so that an

output V_{N2} of the operational amplifier 202 (at node N2) rises. While V_G decreases when V_{N2} rises, the fall of V_G is gradual because of a large transistor width and a large gate capacity of the power MOSFET Q0. In the period of decrease of V_G , the output current I_{OUT} of 900 mA flows, and the sense voltage V_{SENS} is lower than V_{R1} .

As V_G further decreases, the output current I_{OUT} approaches 600 mA and the sense voltage V_{SENS} approaches V_{R1} at which V_{N2} decreases. At $t3$, V_G is constant at a voltage (=6 V in the illustrated example of FIG. 2) such that the output current I_{OUT} becomes constant (600 mA). At the same time, V_{N2} is constant (at 1 V in the illustrated example) so that $V_G=6V$. At $t4$, the output current I_{OUT} becomes zero, when the sense voltage V_{SENS} returns to 5 V and V_{N2} reaches zero. Thereafter, V_G rises slowly depending on the capacity of the charge pump 50.

In the waveform chart of FIG. 2, the time between $t1$ and $t3$ is a response time of the current limiting circuit. The response time may be on the order of 20 μs . The circuits illustrated in FIGs. 1 and 2 form an over-current protection circuit that supplies a load current of up to 500 mA. The over-current protection circuit is configured to lower V_G

in about 20 μ s when a current limit value (such as 600 mA) is exceeded.

In some external apparatuses, large currents, such as 1 A, may flow during operation in a transient manner. When such an external apparatus is connected, the host apparatus may be required not to limit the current by the power switch IC even if the output current exceeds 500 mA as long as the excess is instantaneous. This is because the external apparatus that requires an instantaneous current flow of 1 A would not be able to operate normally if the load current is limited at 600 mA. Thus, the current limit value of the power switch IC may be set at a higher value, such as 1.2 A. However, in this case, if a current of 900 mA flows in the external apparatus due to abnormality, the host apparatus fails to limit the current and does not even recognize an error. As a result, the large current may keep flowing through the external apparatus, potentially causing the external apparatus to be overheated or even ignited.

JP Patent No. 3589392 discusses an over-current detection/protection circuit in which a current limit value is switched to a higher value for a period immediately after turning on a power MOSFET,

where the current limiting value is brought back to a lower value when an inrush current has subsided. In this over-current detection/protection circuit, the over-current detection value is increased only
5 immediately after the turning-on of the power MOSFET so that the inrush current can be allowed to flow. However, if a large current flows instantaneously due to an operation of the external apparatus after its operation current has stabilized, the large current
10 is detected as an over-current. As a result, the output current is limited and the external apparatus fails to operate normally.

SUMMARY OF INVENTION

15 Thus, it is a general object of the present invention to overcome the disadvantages of the related art. A more specific object of the present invention is provide a current limiting circuit that does not recognize as abnormal a
20 transient current that should be permitted.

In one embodiment, a current limiting circuit includes a limit current setting unit that sets a value of a limit current for limiting an output current from a driver circuit connected to the
25 current limiting circuit, the limit current value

including a first acceptable value and a second acceptable value larger than the first acceptable value; an excess current detecting unit that detects when the output current from the driver circuit exceeds the first acceptable value; and a limit current adjusting unit that replaces the first acceptable value with the second acceptable value in a period when the output current detected by the excess current detecting unit exceeds the first acceptable value.

In another embodiment, a current limiting circuit includes a driver circuit including a power MOSFET and a sense resistor through which a current that flows through the power MOSFET flows; a first current limiting unit that detects an output current of the driver circuit by comparing a sense voltage obtained from one end of the sense resistor with a first reference voltage, and that limits the output current when the output current detected by the first current limiting unit is greater than a first limit current value; a second current limiting unit that detects the output current from the driver circuit by comparing the sense voltage obtained from the one end of the sense resistor with a second reference voltage, and that limits the output current when the output

current detected by the second current limiting unit is greater than a second limit current value which is greater than the first limit current value; and an invalidating unit that invalidates an operation of the first current limiting unit for limiting the output current for a period when the output current detected by the first current limiting unit is greater than the first limit current value.

In another embodiment, a current limiting circuit includes a driver circuit including a power MOSFET and a sense resistor through which a current that flows through the power MOSFET flows; a current limiting unit that detects an output current of the driver circuit by comparing a sense voltage obtained from one end of the sense resistor with a first reference voltage, and that limits the output current when the detected output current is greater than a first limit current value; and a limit current value adjusting unit that changes the first reference voltage compared with the sense voltage to a second reference voltage for a period when the output current detected by the current limiting unit is greater than the first limit current value, in order to change the first limit current value to a second limit current value. The first reference voltage and

the second reference voltage are set such that the second limit current value is greater than the first limit current value.

5 BRIEF DESCRIPTION OF THE DRAWINGS

A complete understanding of the present invention may be obtained by reference to the accompanying drawings, when considered in conjunction with the subsequent, detailed description, in which:

10 FIG. 1 is a circuit diagram of a driver circuit and a current limiting circuit according to related art;

FIG. 2 is a waveform chart for the driver circuit and the current limiting circuit illustrated
15 in FIG. 1;

FIG. 3 is a circuit diagram of a current limiting circuit according to a first embodiment of the present invention;

FIG. 4 is a circuit diagram of a current
20 limiting circuit according to a second embodiment of the present invention;

FIG. 5 is a circuit diagram of a current limiting circuit according to a third embodiment of the present invention;

FIG. 6 is a waveform chart for the current limiting circuits according to the embodiments of the present invention;

FIG. 7A is a circuit diagram of a one-shot pulse generating circuit that may be used in the current limiting circuit illustrated in FIG. 3; and

FIG. 7B is a circuit diagram of another one-shot pulse generating circuit that may be used in the current limiting circuit illustrated in FIG. 5.

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BEST MODE OF CARRYING OUT THE INVENTION

First Embodiment

Referring now to the drawings, wherein like reference numerals designate identical or corresponding parts throughout the several views, FIG. 3 is a circuit diagram of a current limiting circuit 100 according to a first embodiment of the present invention. The current limiting circuit 100 includes a current limiting unit 1a, a one-shot pulse generating unit 1b, and a driver circuit 1c. The driver circuit 1c includes a sense resistor R_{1c} and a power MOSFET Q₁₀ (driver transistor). A power supply voltage V_{IN} is supplied as an input voltage to the driver circuit 1c. An external apparatus (load circuit) 1d is connected to an output OUT. The

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external apparatus 1d includes equivalent circuits of a variable-load resistor R_L and a switch SW 1 that simulates an abnormality in the external apparatus 1d. The driver circuit 1c outputs a sense voltage V_{SENS} with reference to the power supply voltage V_{IN} .

The current limiting unit 1a is configured to limit an output current I_{OUT} at the output OUT based on a comparison of the sense voltage V_{SENS} with reference voltages V_{R1} and V_{R2} . The current limiting unit 1a includes amplifiers AMP 11 and AMP 12 for voltage comparison. The charge pump circuit 50 produces a voltage V_G for driving the power MOSFET Q10. The voltage V_G is set to be greater than the power supply voltage V_{IN} . When the sense voltage V_{SENS} is lower than the reference voltages V_{R1} and V_{R2} , the voltage V_G is lowered by an operation of transistors Q11 and Q12.

The reference voltage V_{R1} determines a first limit current I_{LIM1} , while the reference voltage V_{R2} determines a second limit current I_{LIM2} . V_{R1} and V_{R2} are set such that $V_{IN}-V_{R2}$ is greater than $V_{IN}-V_{R1}$; namely, $I_{LIM2} > I_{LIM1}$. Operation waveforms at various parts of the circuit of FIG. 3 are illustrated in FIG. 6, which also schematically illustrates the

relationship between the first limit current I_{LIM1} and the second limit current I_{LIM2} .

The one-shot pulse generating unit 1b includes a one-shot pulse generating circuit 30. The one-shot pulse generating circuit 30 generates a pulse having a pulse width " T_{ILIM2} " at a rising edge of the output of an amplifier AMP 13 (see FIG. 6). The amplifier AMP 13 is operated to cause the one-shot pulse generating circuit 30 to generate the pulse when the sense voltage V_{SENS} is lower than the reference voltage V_{R1} . The one-shot pulse causes the transistor Q13 to be turned off.

The current limiting circuit 100 of FIG. 1 constantly detects whether the output current I_{OUT} exceeds the first limit current I_{LIM1} . The current limiting circuit 100 also detects constantly whether the second limit current I_{LIM2} , which is greater than the first limit current I_{LIM1} , is exceeded. The current limiting circuit 100 includes a first output current limit unit that limits the output current upon detection of the output current exceeding the first limit current I_{LIM1} , and a second output current limit unit that limits the output current upon detection of the output current exceeding the second limit current I_{LIM2} . The current limiting circuit 100

further includes an invalidating unit configured to invalidate the limitation of the output current by the first output current limit unit for a period immediately after the detection of the first limit current having been exceeded by the output current I_{OUT} . Thus, the output current I_{OUT} is not limited for a period immediately after detection of the output current I_{OUT} exceeding the first limit current value unless the output current I_{OUT} exceeds the second limit current value.

An operation of the current limiting circuit 100 is described with reference to the waveform chart of FIG. 6. At time t_0 , the current limiting unit 1a is enabled by an enable signal (not shown), whereby the power MOSFET Q10 is turned on. The switch SW 1 in the external apparatus 1d connected to the output terminal OUT is in an off-state.

The output voltage V_{OUT} then increases and is stabilized at time t_1 . The increase in the output voltage V_{OUT} is accompanied by an increase in the output current I_{OUT} , which is stabilized (I_1) at time t_1 . The sense voltage V_{SENS} is also stabilized at time t_1 after decreasing from V_{IN} .

When the variable-load resistor R_L of the external apparatus 1d is sharply decreased at time t_2 , the output current I_{OUT} increases to a value I_2 and the sense voltage V_{SENS} sharply decreases. If I_2 is greater than the first limit current I_{LIM1} , i.e., if the sense voltage V_{SENS} is lower than V_{R1} , the outputs of the amplifiers AMP 11 and AMP 13 simultaneously assume a high ("H") level, so that the nodes N10 and N31 simultaneously assume "H" levels for a short period. However, the fall of the voltage V_G is gradual because of a large transistor width and a large gate capacity of the power MOSFET Q10. As the voltage V_G starts to change (decrease), the transistor Q13 is soon turned off, so that the voltage V_G hardly changes. In a period " T_{ILIM2} " where the transistor Q13 is off, the limit current of the current limiting circuit 100 is set to be equal to the second limit current I_{LIM2} due to the operation of the amplifier AMP 12.

If the output current I_{OUT} decreases from I_2 to I_1 before the period T_{ILIM2} (pulse width) elapses, the voltage V_G does not change and is maintained at "H" level. When I_{OUT} is at I_2 , the output voltage V_{OUT} is decreased to V_2 due to a voltage drop corresponding to a sum of the on-resistance of the

power MOSFET Q10 and the sense resistance times the increase in the output current I_{OUT} , as illustrated in FIG. 6.

While not illustrated in FIG. 6, if the
5 period of T_{ILIM2} elapses with the output current I_{OUT} maintained at I_2 , the transistor Q13 is turned on, so that the output current I_{OUT} is limited to the first limit current I_{LIM1} . Thus, the period T_{ILIM2} may be set appropriately depending on the characteristics of the
10 connected external apparatus 1d.

When the switch SW 1 of the external
apparatus 1d is turned on at time t_4 , the output OUT is short-circuited to ground. This short-circuiting of the switch SW 1 simulates a failure in the
15 external apparatus 1d.

When the output current I_{OUT} exceeds the first limit current I_{LIM1} , the output of the amplifier AMP 13 assumes "H" level and the limit current is set to the second limit current I_{LIM2} . When the output
20 current I_{OUT} exceeds the second limit current I_{LIM2} , the output V_{N9} of the amplifier AMP 12 assumes "H" level and the transistor Q12 is turned on, so that the power MOSFET Q10 is feedback-controlled and the output current I_{OUT} is limited to the second limit
25 current I_{LIM2} . Simultaneously, error information is

sent to the host apparatus system. A transient current I_{TRANS} in excess of the second limit current I_{LIM2} flows for a very short period before the feedback control of the current limiting unit 1a is
5 stabilized.

At time t_5 , the enable signal to the current limiting unit 1a is disabled by the operation of the host apparatus system in response to the error information. As a result, the power MOSFET Q10 is
10 turned off and the output current I_{OUT} becomes zero. Thereafter, when the switch SW 1 is turned off before time t_6 and the current limiting unit 1a is again enabled at time t_6 , the transistor Q10 is turned on after time t_6 , so that the output voltage V_{OUT} rises
15 in the same manner as after t_0 .

Second Embodiment

FIG. 4 is a circuit diagram of a current limiting circuit 200 according to a second embodiment
20 of the present invention. The current limiting circuit 200 is generally similar to the current limiting circuit 100 illustrated in FIG. 1. Specifically, the current limiting circuit 200 includes a driver circuit 2c, a current limiting unit
25 2a, and a one-shot pulse generating unit 2b which are

configured to provide substantially identical functions to those of the driver circuit 1c, the current limiting unit 1a, and the one-shot pulse generating unit 1b, respectively, of the current limiting circuit 100.

In the current limiting circuit 200, an output of the one-shot pulse generating unit 2b is supplied to an enable terminal EN of the amplifier AMP 21 of the current limiting unit 2a. In the case of the one-shot pulse generating unit 1c of the foregoing embodiment illustrated in FIG. 3, the one-shot pulse generating circuit 30 generates a one-shot pulse in order to turn off the transistor Q13, thus invalidating the turning-on of the transistor Q11. Similarly, in the current limiting unit 2a illustrated in FIG. 4, the amplifier AMP 21 is disabled by a one-shot pulse generated by the one-shot pulse generating circuit 30 so that the output of the amplifier AMP 21 is maintained at "L" level, thereby preventing (invalidating) the turning-on of the transistor Q21.

The operation waveforms of the current limiting circuit 200 are similar to the waveforms for the current limiting circuit 100 illustrated in FIG. 6. The driver circuit 2c includes a power MOSFET Q20,

a power MOSFET Q200 having a smaller transistor width than the power MOSFET Q20, and a sense resistor R2c. A current corresponding to a size ratio of the power MOSFET Q20 and the power MOSFET Q200 flows through
5 the sense resistor R2c, producing a sense voltage V_{SENS} . Thus, the voltage drop by the sense resistor R2c in the driver circuit 2c can be reduced. The driver circuit 2c may be replaced with the driver circuit 1c illustrated in FIG. 3.

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Third Embodiment

FIG. 5 is a circuit block diagram of a current limiting circuit 300 according to a third embodiment. The current limiting circuit 300 is also
15 generally similar to the current limiting circuit 100 illustrated in FIG. 3. In FIG. 5, V_{REF} designates a reference voltage at ground (GND) potential, which may be realized by a bandgap reference circuit. V_{REF} is applied to the resistor R2 by the operation of the
20 amplifier AMP 32, so that $V_{\text{IN}} - V_{\text{R3}}$ is $V_{\text{REF}} \times R1/R2$. The value of V_{R1} (i.e., the value of V_{I0}) is set such that V_{R1} is equal to V_{R3} with reference to ground (GND) when the transistor Q33 is turned off.

When the transistor Q33 is turned on (such
25 as by the one-shot pulse from the one-shot pulse

generating circuit 130), $V_{IN} - V_{R3}$ becomes $V_{REF} \times R1/(R2//R3)$. This corresponds to the reference voltage that determines the second limit current I_{LIM2} in the First and the Second Embodiments. $(R2//R3)$ indicates the resistance when the resistors $R2$ and $R3$ are connected in parallel, whose value is $(R2 \times R3)/(R2 + R3)$. The output voltage V_{OUT} and the output current I_{OUT} transition as illustrated in FIG. 6. The waveforms are identical to those of the First Embodiment between time $t0$ and time $t2$.

When the variable-load resistor R_L of the external apparatus 3d sharply decreases at time $t2$, the output current I_{OUT} increases to a value $I2$ and the sense voltage V_{SENS} sharply drops. If $I2$ is greater than the first limit current I_{LIM1} , i.e., if the sense voltage V_{SENS} is lower than V_{R1} , the output of the amplifier AMP 33 assumes "H" level. In response, the output of the one-shot pulse generating circuit 130 rises and the transistor Q33 is turned on, whereby V_{R3} is changed from a voltage corresponding to the reference voltage that determines the first limit current I_{LIM1} to a voltage corresponding to the reference voltage that determines the second limit current I_{LIM2} .

While the output of the amplifier AMP 31 also rises simultaneously with the increase in the output current I_{OUT} and the sharp decrease in the sense voltage V_{SENS} , V_{R3} is changed (sharply decreased) to a voltage corresponding to the reference voltage that determines the second limit current I_{LIM2} immediately after the start of change in the voltage V_G . Thus, the output of the amplifier AMP 31 falls, so that the voltage V_G is hardly changed substantially.

If the output current I_{OUT} decreases from I_2 to I_1 before the period T_{ILIM2} (pulse width of one-shot pulse) elapses, the voltage V_G is not changed and maintained at "H" level. When I_{OUT} is at I_2 , the output voltage V_{OUT} decreases to V_2 due to a voltage drop corresponding to a sum of the on-resistance of the power MOSFET Q10 and the sense resistance times the increase in the output current I_{OUT} , as illustrated in FIG. 6.

Thereafter, when the switch SW 1 of the external apparatus 1d is turned on at time t_4 and the output OUT is short-circuited to ground (GND), the output current I_{OUT} exceeds the first limit current I_{LIM1} and the output of the amplifier AMP 33 assumes "H" level, so that the limit current is set to the second limit current I_{LIM2} . While the output current

I_{OUT} may tend to exceed the second limit current I_{LIM2} , the output of the amplifier AMP 31 assumes "H" level and the transistor Q31 is turned on. Thus, the power MOSFET Q10 is feedback-controlled such that the
5 output current I_{OUT} is limited to the second limit current I_{LIM2} . Simultaneously, error information is sent to the host apparatus system, and a transient current I_{TRANS} in excess of the second limit current I_{LIM2} flows for a very short period after time $t4$, as
10 in the case of the First and the Second Embodiments.

The enable signal to the current limiting unit 3a is disabled at time $t5$ by the operation of the host apparatus system in response to the error information. As a result, the power MOSFET Q10 is
15 turned off, and the output current I_{OUT} becomes zero. Thereafter, when the switch SW 1 is turned off before time $t6$ and the current limiting unit 3a is again enabled at time $t6$, the transistor Q10 is turned on after time $t6$, so that the output voltage V_{OUT} rises
20 in the same way as after $t0$.

Thus, in a system where an external apparatus is supplied with electric power from a host apparatus, when the external apparatus temporarily requires a large transient current (such as $I2$), the
25 current limiting circuits 100, 200, and 300 according

to the foregoing embodiments of the present invention allow such transient current to flow for the period T_{ILIM2} . If the current (I_2) flows even after the period, the output current I_{OUT} is compulsorily limited to I_{LIM1} , thus ensuring safety. The period T_{ILIM2} may be appropriately designed depending on the characteristics of the external apparatus.

One-shot Pulse Generating Circuit

The one-shot pulse generating circuit 30 or 130 may be based on conventional technologies. FIG. 7A is a circuit diagram of the one-shot pulse generating circuit 30. The one-shot pulse generating circuit 30 includes plural N-ch MOSFETs, plural P-ch MOSFETs, an inverter, a NAND circuit, a capacitor, and a power supply. A capacitor C2 is charged with a constant current determined by a bias input BIASP1. Thus, the rise time of the one-shot pulse is determined by the constant current determined by BIASP1.

Similarly, FIG. 7B is a circuit diagram of the one-shot pulse generating circuit 130. The one-shot pulse generating circuit 130 includes plural N-ch MOSFETs, plural P-ch MOSFETs, an inverter, a NAND circuit, a capacitor, and a power supply. A

capacitor C4 is discharged by a constant current determined by a bias input BIASN1. Thus, the fall time of the one-shot pulse is determined by the constant current determined by BIASN1.

5 An embodiment of the present invention may be utilized in an over-current protection apparatus for a power MOSFET, a power switch IC, or an over-current protection circuit for an IC having a power switch. In accordance with an embodiment of the
10 present invention, when a supply current that slightly exceeds a maximum rated current is detected in a load drive apparatus, such as a regulator or a driver circuit, that supplies a voltage to a load, the current supply is permitted if the excess current
15 is transient and required by the external apparatus for normal operation.

 Although this invention has been described in detail with reference to certain embodiments, variations and modifications exist within the scope
20 and spirit of the invention as described and defined in the following claims.

 The present application is based on Japanese Priority Application No. 2010-032631 filed February 17, 2010, the entire contents of which are
25 hereby incorporated by reference.

CLAIMS

Claim 1. A current limiting circuit comprising:

- 5 a limit current setting unit that sets a value of a limit current for limiting an output current from a driver circuit connected to the current limiting circuit; the limit current value including a first acceptable value and a second
- 10 acceptable value larger than the first acceptable value;
- an excess current detecting unit that detects when the output current from the driver circuit exceeds the first acceptable value; and
- 15 a limit current adjusting unit that replaces the first acceptable value with the second acceptable value in a period when the output current detected by the excess current detecting unit exceeds the first acceptable value.

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Claim 2. A current limiting circuit comprising:

- a driver circuit including a power MOSFET and a sense resistor through which a current that
- 25 flows through the power MOSFET flows;

a first current limiting unit that detects an output current of the driver circuit by comparing a sense voltage obtained from one end of the sense resistor with a first reference voltage, and that
5 limits the output current when the output current detected by the first current limiting unit is greater than a first limit current value;

a second current limiting unit that detects the output current from the driver circuit by
10 comparing the sense voltage obtained from the one end of the sense resistor with a second reference voltage, and that limits the output current when the output current detected by the second current limiting unit is greater than a second limit current value which is
15 greater than the first limit current value; and

an invalidating unit that invalidates an operation of the first current limiting unit for limiting the output current for a period when the output current detected by the first current limiting
20 unit is greater than the first limit current value.

Claim 3. A current limiting circuit comprising:

a driver circuit including a power MOSFET and a sense resistor through which a current that flows through the power MOSFET flows;

a current limiting unit that detects an
5 output current of the driver circuit by comparing a sense voltage obtained from one end of the sense resistor with a first reference voltage, and that limits the output current when the detected output current is greater than a first limit current value;
10 and

a limit current value adjusting unit that changes the first reference voltage compared with the sense voltage to a second reference voltage for a period when the output current detected by the
15 current limiting unit is greater than the first limit current value, in order to change the first limit current value to a second limit current value,

wherein the first reference voltage and the second reference voltage are set such that the
20 second limit current value is greater than the first limit current value.

FIG.1

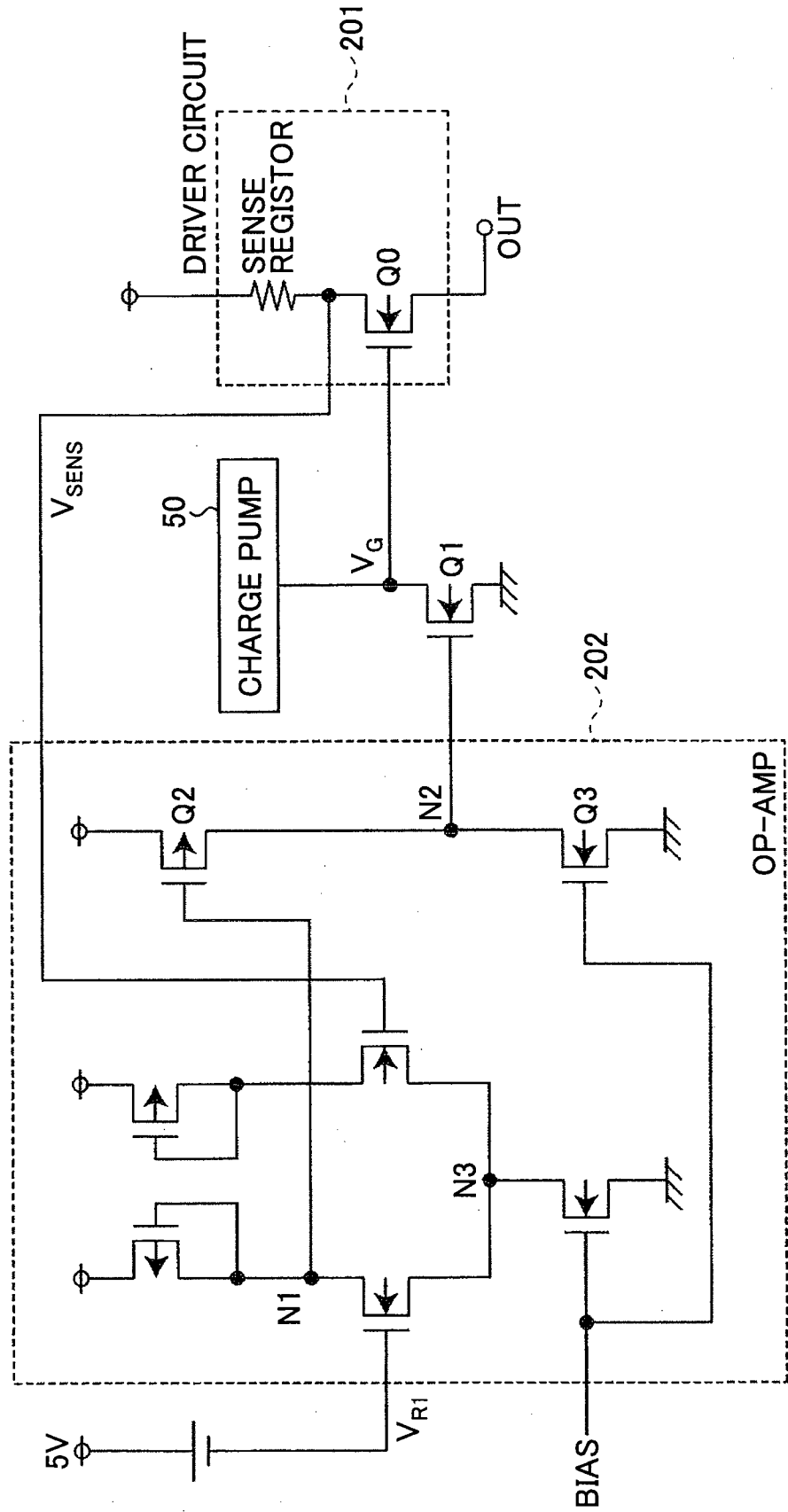


FIG.2

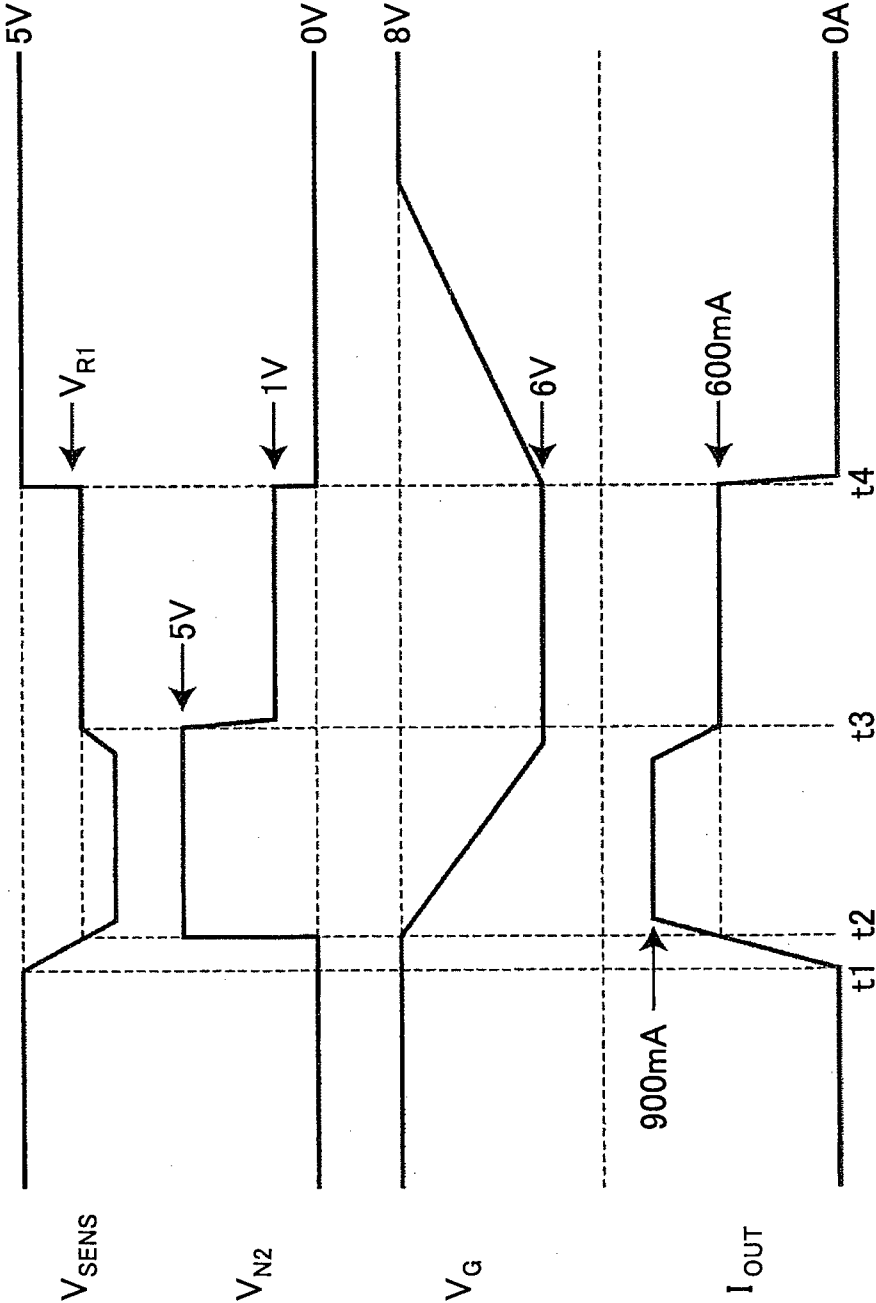


FIG.3

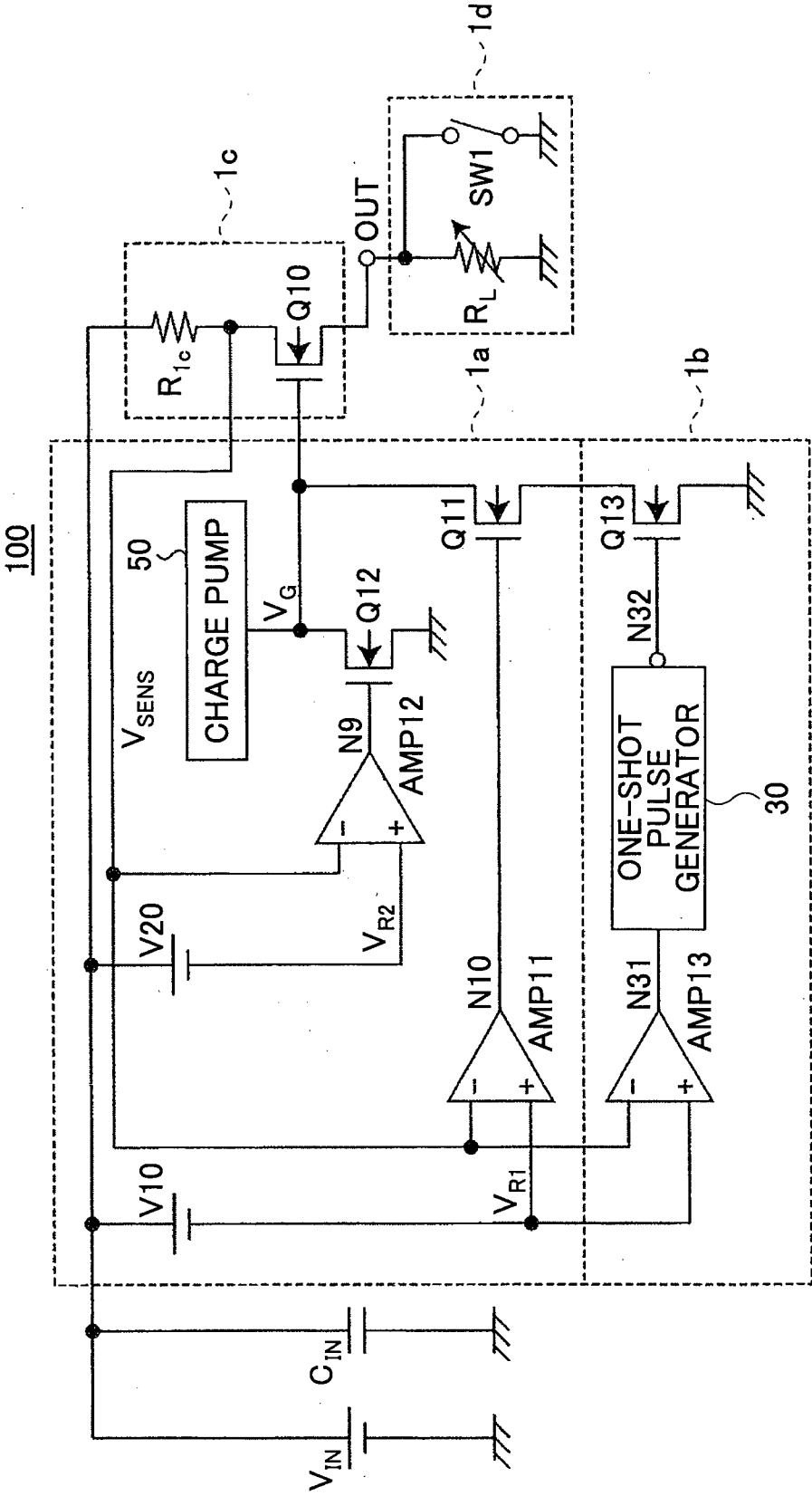


FIG. 4

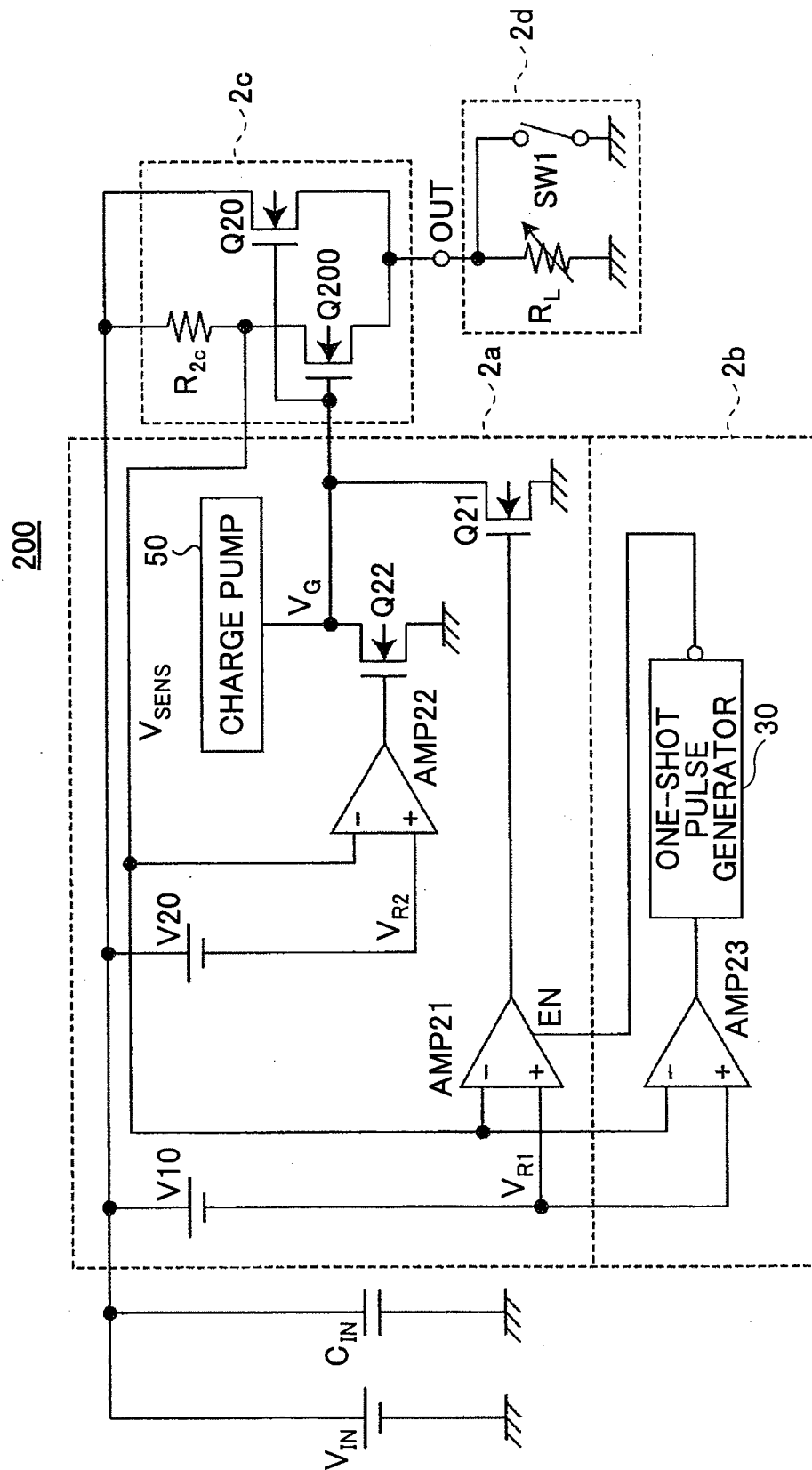
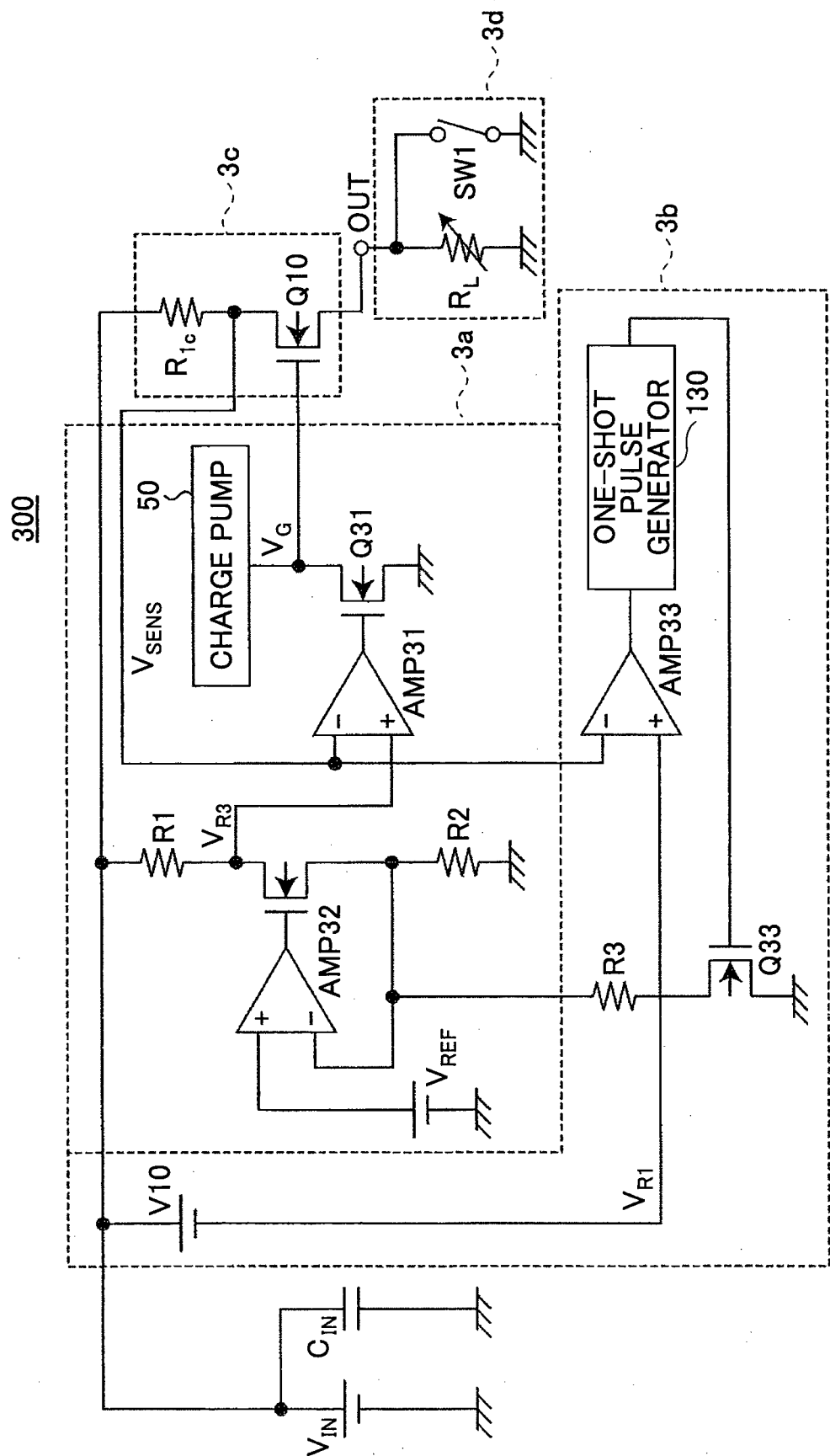
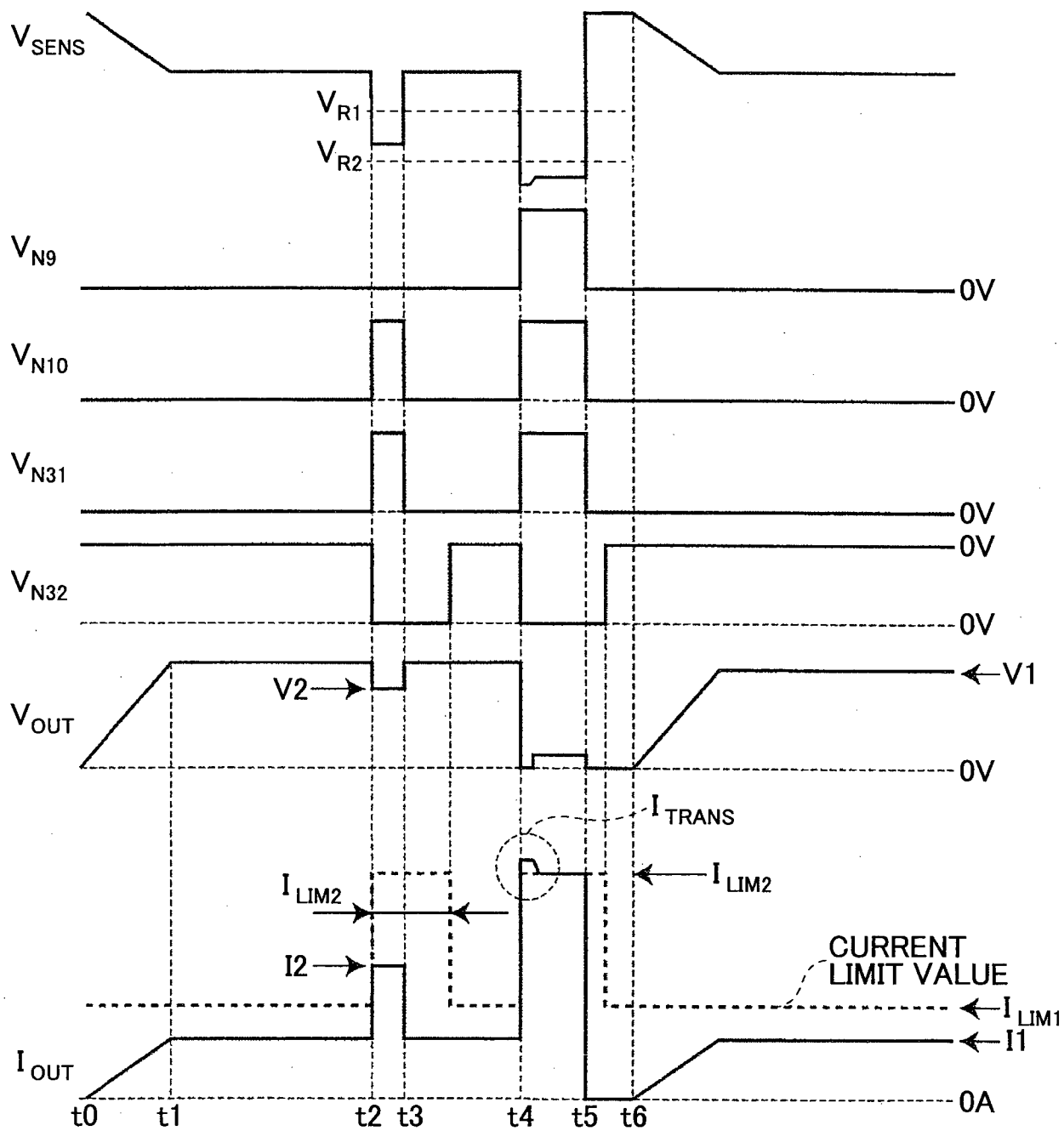


FIG. 5



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FIG.6



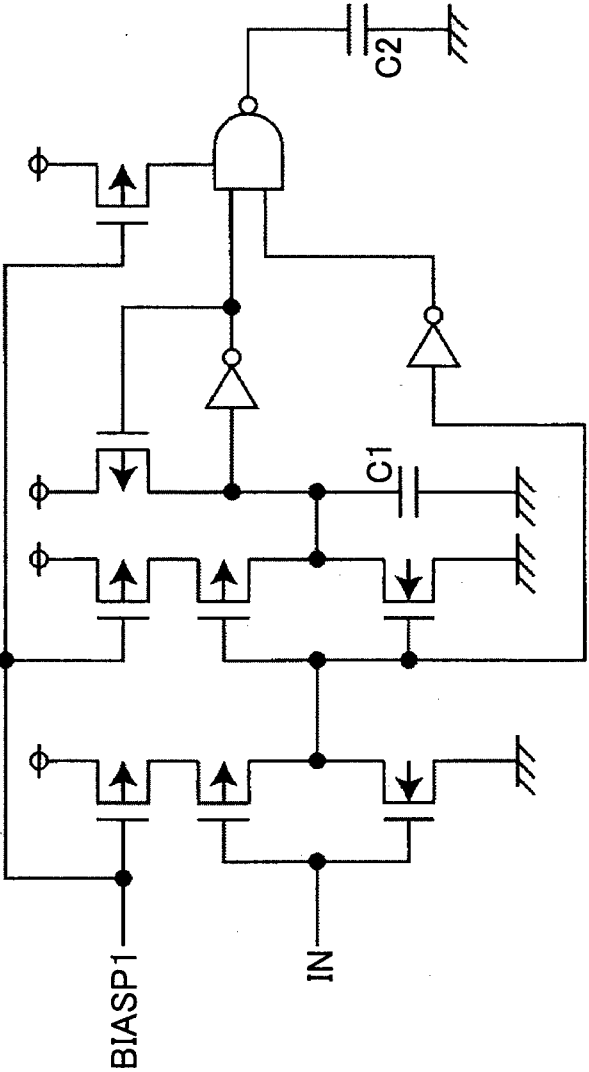


FIG. 7A

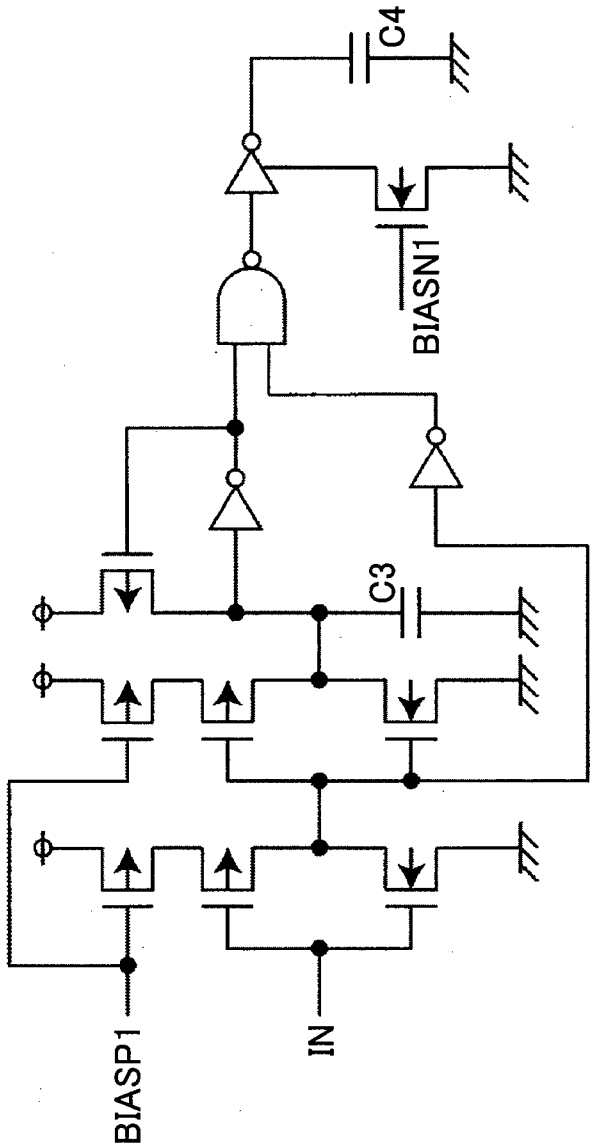


FIG. 7B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/051376

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. G05F1/10 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. G05F1/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
 Published unexamined utility model applications of Japan 1971-2011
 Registered utility model specifications of Japan 1996-2011
 Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 3589392 B2 (Yazaki Corporation) 2004.11.17, [0065]-[0070], Figs 1-3 (Family : none)	1-3
A	JP 2005-339355 A (Sony Corporation) 2005.12.08, [0071]-[0079], Figs 7-10 & US 2005/0264970 A1	1-3
PA	JP 2010-074874 A (FUJITSU TELECOM NETWORKS LIMITED) 2010.04.02, [0035]-[0040], Figs 7-9 (Family : none)	1-3
PA	JP 2010-200550 A (NEC Corporation, NEC Tohoku, Ltd.) 2010.09.09, [0033]-[0035], Figs 3-5 (Family : none)	1-3



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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“&” document member of the same patent family

Date of the actual completion of the international search

25.02.2011

Date of mailing of the international search report

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