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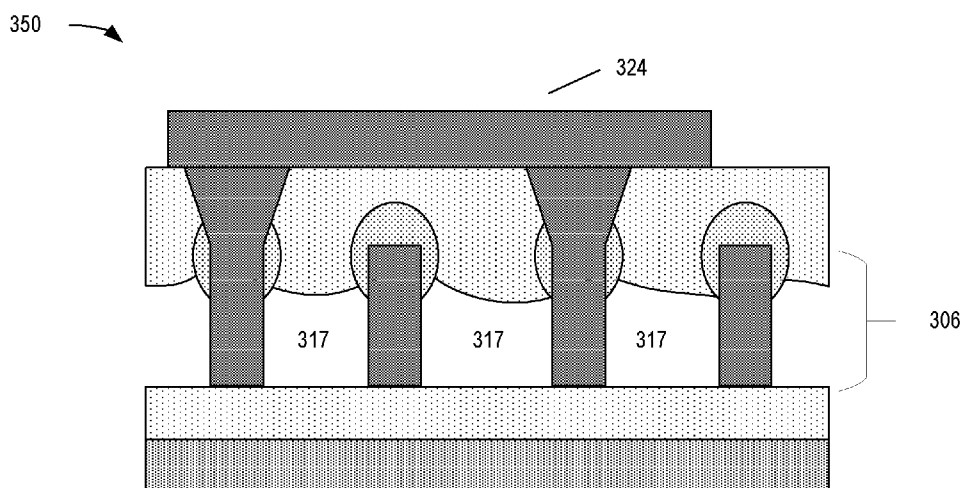


Fig. 3F

(57) Abstract: An apparatus is provided which comprises: a semiconductor circuit substrate, a plurality of interconnect layers on different planes on the substrate, a plurality of metal traces in a first of the plurality of interconnect layers, a helmet dielectric film on the metal traces, wherein the helmet dielectric film comprises a first thickness on a top portion of the metal traces and a second thickness on sidewalls of the metal traces, the first thickness being greater than the second thickness, and interlayer dielectric material adjacent the helmet dielectric film. Other embodiments are also disclosed and claimed.



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CREATING DIELECTRIC HELMET FILMS USING PULSED GAS DEPOSITION

BACKGROUND

[0001] As integrated circuit devices continue to scale down in feature sizes and spacing, it becomes more challenging from a manufacturing perspective to be able to deposit materials in certain locations and not others, for example there may be a need to deposit a film on top of a feature with little or no deposition on the side wall or on the bottom. In many cases additional steps, such as depositing a sacrificial fill to keep subsequent dielectric deposition out of the feature, are currently utilized.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The embodiments of the disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the disclosure, which, however, should not be taken to limit the disclosure to the specific embodiments, but are for explanation and understanding only.

[0003] **Fig. 1** illustrates a cross-sectional view of an integrated circuit device suitable for implementing dielectric helmet films formed using pulsed gas deposition, according to some embodiments,

[0004] **Figs. 2A-2F** illustrate cross-sectional views of manufacturing steps of dielectric helmet films using pulsed gas deposition, according to some embodiments,

[0005] **Figs. 3A-3F** illustrate cross-sectional views of manufacturing steps of dielectric helmet films using pulsed gas deposition, according to some embodiments,

[0006] **Fig. 4** illustrates a diagram of an example semiconductor manufacturing equipment, according to some embodiments,

[0007] **Fig. 5** illustrates a flowchart of a method of forming an integrated circuit device with dielectric helmet films using pulsed gas deposition, according to some embodiments, and

[0008] **Fig. 6** illustrates a smart device or a computer system or a SoC (System-on-Chip) which includes an integrated circuit device with dielectric helmet films using pulsed gas deposition, according to some embodiments.

DETAILED DESCRIPTION

[0009] Creating dielectric helmet films using pulsed gas deposition is generally presented. In this regard, embodiments of the present invention enable highly non-conformal

(in the range of about 15% to 20% or less conformality) dielectric thin films to be deposited on interconnect traces. One skilled in the art would appreciate that these depositions may enable greater ease of manufacturing by removing the need for additional patterning steps. Additionally, gas pulsing may allow multiple process options in a single chamber and the option of doing graded films in a single chamber.

[0010] In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present disclosure. It will be apparent, however, to one skilled in the art, that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present disclosure.

[0011] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0012] Throughout the specification, and in the claims, the term "connected" means a direct connection, such as electrical, mechanical, or magnetic connection between the things that are connected, without any intermediary devices. The term "coupled" means a direct or indirect connection, such as a direct electrical, mechanical, or magnetic connection between the things that are connected or an indirect connection, through one or more passive or active intermediary devices. The term "circuit" or "module" may refer to one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function. The term "signal" may refer to at least one current signal, voltage signal, magnetic signal, or data/clock signal. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0013] Unless otherwise specified the use of the ordinal adjectives "first," "second," and "third," etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0014] For the purposes of the present disclosure, phrases “A and/or B” and “A or B” mean (A), (B), or (A and B). For the purposes of the present disclosure, the phrase “A, B, and/or C” means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C). The terms “left,” “right,” “front,” “back,” “top,” “bottom,” “over,” “under,” and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions.

[0015] **Fig. 1** illustrates a cross-sectional view of an integrated circuit device suitable for implementing dielectric helmet films formed using pulsed gas deposition, according to some embodiments. As shown, device 100 includes interconnect layers 102, circuit substrate 104, metal 106, dielectric 108, metal traces 110, substrate 112, circuits 114, and contacts 116.

[0016] Interconnect layers 102 may provide electrical connections between components of circuit substrate 104 and contacts 116, which may be lands, bumps, pins, etc., to couple device 100 with external substrates, interposers, packages, sockets, etc. Interconnect layers 102 may be formed iteratively on separate planes above circuit substrate 104. In some embodiments, interconnect layers 102 includes metal 106, such as copper, that may be plated into etched trenches and vias, then polished back to create metal trenches (such as metal traces 110), planes, and vias, for example to communicate power and signals to and from circuit substrate 104. Metal 106 in interconnect layers 102 may be interspersed with dielectric 108, which has insulative properties. In some embodiments, dielectric 108 represents an interlayer dielectric (ILD) material, such as carbon doped oxide (CDO), deposited across metal 106 structures to a thickness at least equivalent to a thickness of an interconnect structure including wiring lines and subsequent level conductive vias. Metal traces 110 may have fine feature sizes and spacing and may benefit from having a highly non-conformal thin film helmet dielectric as described in more detail hereinafter.

[0017] Circuit substrate 104 may include integrated circuits in a circuits 114 layer on a substrate 112. In some embodiments, circuits 114 include semiconductor transistors, switches, gates, relays, and/or memory components. Circuits 114 may include millions of circuit devices or components that each include an input, an output, and/or a power signal communicated through interconnect layers 102. Substrate 112 may be made of silicon, other semiconductor material, and/or other non-semiconductor material.

[0018] **Figs. 2A-2F** illustrate cross-sectional views of manufacturing steps of dielectric helmet films using pulsed gas deposition, according to some embodiments. As shown in Fig. 2A, assembly 200 includes circuit substrate 202, dielectric layer 204, and patterning material 206. Dielectric layer 204 may represent one or more layers of dielectric,

for example dielectric 108, that have been built up on circuit substrate 202. Patterning material 206 may have been etched from a metal or other material to form a backbone for patterning dielectric layer 204 as part of a damascene process for patterning copper interconnects. While shown as having straight sides, patterning material 206 may have curved and/or irregular sides.

[0019] Fig. 2B shows assembly 210, which may include dielectric helmets 208 deposited on a (top) surface of adjacent patterning material 206. Dielectric helmets 208 may be deposited by atomic layer deposition (ALD), chemical vapour deposition (CVD), plasma enhanced CVD (PECVD), or by other means, utilizing the methods described in more detail hereinafter. In some embodiments, dielectric helmets 208 are highly non-conformal in that helmet sidewall thickness may be 20% or less of helmet top thickness. In some embodiments, helmet sidewall thickness may be around 2 nm, while helmet top thickness may be around 12 nm. In some embodiments, dielectric helmets 208 are a silicon nitride or oxide, such as silicon nitride or silicon dioxide, for example.

[0020] As shown in Fig. 2C, assembly 220 has had trenches 222 formed in dielectric layer 204. In some embodiments, trenches 222 are formed by chemical or mechanical etching. In some embodiments, the width of trenches 222 may be defined by a spacing between dielectric helmets 208.

[0021] Turning now to Fig. 2D, assembly 230 may have had patterning material 206 and dielectric helmets 208 removed. In some embodiments, mechanical and/or chemical processes are used to remove patterning material 206 and dielectric helmets 208.

[0022] Fig. 2E shows assembly 240, which may have had copper 242 plated in and over trenches 222. In some embodiments, copper 242 may be formed in multiple steps, for example an electroplating step after a seed layer deposition step.

[0023] As shown in Fig. 2F, assembly 250 may have had copper 242 planarized, by chemical and/or mechanical processes, down to a junction with dielectric layer 204. In some embodiments, the planarization of copper 242 may result in the formation of copper traces 252. In some embodiments copper traces 252 may form the basis of an interconnect layer, such as an interconnect layer 102.

[0024] **Figs. 3A-3F** illustrate cross-sectional views of manufacturing steps of dielectric helmet films using pulsed gas deposition, according to some embodiments. As shown in Fig. 3A, assembly 300 includes circuit substrate 302, interconnect layers 304, and metal traces 306. Interconnect layers 304 may represent any number of layers, for example interconnect layers 102, that have been built up on circuit substrate 302. Metal traces 306

may have been formed from a damascene process as described in relation to Figs. 2A-2F. Metal traces 306 may be electrically coupled with structures in interconnect layers 304 and circuit substrate 302 through vias, not shown. While shown as having straight sides, metal traces 306 may have curved and/or irregular sides.

[0025] Fig. 3B shows assembly 310, which may include dielectric helmets 308 deposited on a (top) surface of adjacent metal traces 306. Dielectric helmets 308 may be deposited by atomic layer deposition (ALD), chemical vapour deposition (CVD), plasma enhanced CVD (PECVD), or by other means, utilizing the methods described in more detail hereinafter. In some embodiments, dielectric helmets 308 are highly non-conformal in that helmet sidewall thickness 314 may be 20% or less of helmet top thickness 312. In some embodiments, helmet sidewall thickness 314 may be around 2 nm, while helmet top thickness 312 may be around 12 nm. In some embodiments, dielectric helmets 308 are a silicon nitride or oxide, such as silicon nitride or silicon dioxide, for example.

[0026] As shown in Fig. 3C, assembly 320 has had dielectric 316 deposited over metal traces 306 and dielectric helmets 308. In some embodiments, dielectric 316 is a low k interlayer dielectric (ILD) material, such as carbon doped oxide (CDO). While shown as covering dielectric helmets 308, dielectric 316 may not cover dielectric helmets 308 in other embodiments. In some embodiments, dielectric 316 is removed from, or prevented from being deposited in, spaces between metal traces 306 to form air gaps 317.

[0027] Turning now to Fig. 3D, assembly 330 may include openings 318 formed through dielectric 316 and dielectric helmets 308 to expose metal traces 306. In some embodiments, an etch process is utilized perhaps after additional patterning steps.

[0028] Fig. 3E shows assembly 340, which may have had interconnect material 322 deposited in openings 318. In some embodiments, interconnect material 322 represents copper plating that may have been planarized.

[0029] As shown in Fig. 3F, assembly 350 may include interconnect 324 on a surface of dielectric 316. In some embodiments, interconnect 324 may conductively couple two or more of metal traces 306.

[0030] **Fig. 4** illustrates a diagram of an example semiconductor manufacturing equipment, according to some embodiments. As shown, equipment 400 includes deposition chamber 402, pedestal 404, substrate 406, precursor control 408, diluent control 410, plasma 412, plasma control 414, electrodes 416 and pump control 418. Substrate 406 may represent intermediary assemblies of an integrated circuit device, such as any of the assemblies depicted in Figs. 3A-3F. Pedestal 404 may support substrate 406 and may be used to

transport substrate 406 into and out of deposition chamber 402. In some embodiments, equipment 400 is used to form dielectric helmets 308 on metal traces 306.

[0031] Deposition chamber 402 may deposit dielectric thin films by performing PECVD, however, other types of deposition may be utilized that take advantage of benefits of embodiments of the present invention. In some embodiments, deposition chamber 402 provides a temperature and pressure, which may vary depending upon the desired reactions, for a chemical vapor deposition.

[0032] In some embodiments, precursor control 408 controls the deposition process by controlling the supply of precursor molecules necessary for deposition to occur. In some embodiments, precursor control 408 may pulse the supply of a precursor gas proximate to substrate 406 to create lean conditions that may tend to lead to deposition mainly on a closest surface, resulting in non-conformal thin films, such as dielectric helmets 208 or 308. In some embodiments, the precursor gas may include silane, dichlorosilane, or tetraethylorthosilicate, for example.

[0033] In some embodiments, precursor control 408 utilizes a step function, sine function, ramp function or other periodic or aperiodic function to adjust a supply of a precursor gas. In some embodiments, precursor control 408 adjusts a supply of a precursor gas between on and off, however, in other embodiments, the adjustment may be in a range between a regular supply level and a lowered (non-zero) supply level. In some embodiments, the durations of intervals of regular precursor gas supply level and intervals of lowered precursor gas supply level are disparate, while in other embodiments they may be similar. Additionally, the durations of intervals of regular precursor gas supply level and intervals of lowered precursor gas supply level may be consistent or may vary.

[0034] Diluent control 410 may provide one or more gases proximate to substrate 406 to enable deposition. In some embodiments, diluent control maintains a constant supply of diluent gas while precursor control 408 regulates the supply of a precursor gas.

[0035] Plasma control 414 may control the electrodes 416 to ionize precursor and diluent gases to form plasma 412. In some embodiments, plasma control 414 maintains plasma 412 while precursor control 408 regulates the supply of a precursor gas. Plasma control 414 may provide electrodes 416 with DC, AC, or RF energy in various embodiments.

[0036] Pump control 418 may remove gases, for example byproducts of deposition reactions, from deposition chamber 402. In some embodiments, pump control 418 may vary a pump setting to further create lean conditions at a surface of substrate 406 in conjunction with precursor control 408.

[0037] **Fig. 5** illustrates a flowchart of a method of forming an integrated circuit device with dielectric helmet films using pulsed gas deposition, in accordance with some embodiments. Although the blocks in the flowchart with reference to **Fig. 5** are shown in a particular order, the order of the actions can be modified. Thus, the illustrated embodiments can be performed in a different order, and some actions/blocks may be performed in parallel. Some of the blocks and/or operations listed in **Fig. 5** are optional in accordance with certain embodiments. The numbering of the blocks presented is for the sake of clarity and is not intended to prescribe an order of operations in which the various blocks must occur.

Additionally, operations from the various flows may be utilized in a variety of combinations.

[0038] Method 500 begins with forming (502) interconnects, for example in a plane on a dielectric layer on a substrate, such as metal traces 306. Next, deposition is prepared (504). For example substrate 406 may be placed in deposition chamber 402 with an appropriate temperature and pressure provided.

[0039] Then, precursor and diluent gases may be provided (506) proximate to substrate 406. In some embodiments, plasma 412 is formed adjacent to metal traces 306. Next, to create non-conformal deposition of dielectric helmets 308, precursor control 408 may regulate (508) the supply of precursor gas in deposition chamber 402, for example by pulsing or other techniques previously mentioned in reference to precursor control 408.

[0040] The method continues with depositing (510) interlayer dielectric 316. In some embodiments, dielectric 316 may be removed from, or prevented from being deposited, between metal traces 306 leaving air gaps 317. Next, openings 318 may be formed (512) through dielectric helmets 308 to expose metal traces 306. Finally, interconnect material 322 may be added (514) to fill openings 318. Further processing steps may be taken to add additional interconnect layers and contacts, for example, to complete the integrated circuit device.

[0041] **Fig. 6** illustrates a smart device or a computer system or a SoC (System-on-Chip) 600 which an integrated circuit device with dielectric helmet films using pulsed gas deposition, according to some embodiments. In some embodiments, computing device 600 represents a mobile computing device, such as a computing tablet, a mobile phone or smart-phone, a wireless-enabled e-reader, or other wireless mobile device. It will be understood that certain components are shown generally, and not all components of such a device are shown in computing device 600. In some embodiments, one or more components of computing device 600, for example processor 610 and/or memory subsystem 660, include an

integrated circuit device with dielectric helmet thin films on interconnects as described above.

[0042] For purposes of the embodiments, the transistors in various circuits and logic blocks described here are metal oxide semiconductor (MOS) transistors or their derivatives, where the MOS transistors include drain, source, gate, and bulk terminals. The transistors and/or the MOS transistor derivatives also include Tri-Gate and FinFET transistors, Gate All Around Cylindrical Transistors, Tunneling FET (TFET), Square Wire, or Rectangular Ribbon Transistors, ferroelectric FET (FeFETs), or other devices implementing transistor functionality like carbon nanotubes or spintronic devices. MOSFET symmetrical source and drain terminals i.e., are identical terminals and are interchangeably used here. A TFET device, on the other hand, has asymmetric Source and Drain terminals. Those skilled in the art will appreciate that other transistors, for example, Bi-polar junction transistors—BJT PNP/NPN, BiCMOS, CMOS, etc., may be used without departing from the scope of the disclosure.

[0043] In some embodiments, computing device 600 includes a first processor 610. The various embodiments of the present disclosure may also comprise a network interface within 670 such as a wireless interface so that a system embodiment may be incorporated into a wireless device, for example, cell phone or personal digital assistant.

[0044] In one embodiment, processor 610 can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 610 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting the computing device 600 to another device. The processing operations may also include operations related to audio I/O and/or display I/O.

[0045] In one embodiment, computing device 600 includes audio subsystem 620, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker and/or headphone output, as well as microphone input. Devices for such functions can be integrated into computing device 600, or connected to the computing device 600. In one embodiment, a user interacts with the computing device 600 by providing audio commands that are received and processed by processor 610.

[0046] Display subsystem 630 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device 600. Display subsystem 630 includes display interface 632, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 632 includes logic separate from processor 610 to perform at least some processing related to the display. In one embodiment, display subsystem 630 includes a touch screen (or touch pad) device that provides both output and input to a user.

[0047] I/O controller 640 represents hardware devices and software components related to interaction with a user. I/O controller 640 is operable to manage hardware that is part of audio subsystem 620 and/or display subsystem 630. Additionally, I/O controller 640 illustrates a connection point for additional devices that connect to computing device 600 through which a user might interact with the system. For example, devices that can be attached to the computing device 600 might include microphone devices, speaker or stereo systems, video systems or other display devices, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[0048] As mentioned above, I/O controller 640 can interact with audio subsystem 620 and/or display subsystem 630. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of the computing device 600. Additionally, audio output can be provided instead of, or in addition to display output. In another example, if display subsystem 630 includes a touch screen, the display device also acts as an input device, which can be at least partially managed by I/O controller 640. There can also be additional buttons or switches on the computing device 600 to provide I/O functions managed by I/O controller 640.

[0049] In one embodiment, I/O controller 640 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in the computing device 600. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[0050] In one embodiment, computing device 600 includes power management 650 that manages battery power usage, charging of the battery, and features related to power saving operation. Memory subsystem 660 includes memory devices for storing information in computing device 600. Memory can include nonvolatile (state does not change if power to

the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory subsystem 660 can store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of the computing device 600.

[0051] Elements of embodiments are also provided as a machine-readable medium (e.g., memory 660) for storing the computer-executable instructions. The machine-readable medium (e.g., memory 660) may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, phase change memory (PCM), or other types of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the disclosure may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[0052] Connectivity 670 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable the computing device 600 to communicate with external devices. The computing device 600 could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[0053] Connectivity 670 can include multiple different types of connectivity. To generalize, the computing device 600 is illustrated with cellular connectivity 672 and wireless connectivity 674. Cellular connectivity 672 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless connectivity (or wireless interface) 674 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc.), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), or other wireless communication.

[0054] Peripheral connections 680 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that the computing device 600 could both be a peripheral device ("to" 682) to other computing devices, as well as have peripheral devices ("from" 684) connected

to it. The computing device 600 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on computing device 600. Additionally, a docking connector can allow computing device 600 to connect to certain peripherals that allow the computing device 600 to control content output, for example, to audiovisual or other systems.

[0055] In addition to a proprietary docking connector or other proprietary connection hardware, the computing device 600 can make peripheral connections 680 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other types.

[0056] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[0057] Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive

[0058] While the disclosure has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. The embodiments of the disclosure are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

[0059] In addition, well known power/ground connections to integrated circuit (IC) chips and other components may or may not be shown within the presented figures, for

simplicity of illustration and discussion, and so as not to obscure the disclosure. Further, arrangements may be shown in block diagram form in order to avoid obscuring the disclosure, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present disclosure is to be implemented (i.e., such specifics should be well within purview of one skilled in the art). Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the disclosure, it should be apparent to one skilled in the art that the disclosure can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

[0060] The following examples pertain to further embodiments. Specifics in the examples may be used anywhere in one or more embodiments. All optional features of the apparatus described herein may also be implemented with respect to a method or process.

[0061] In one example, an apparatus is provided comprising: a semiconductor circuit substrate; a plurality of interconnect layers on different planes on the substrate; a plurality of metal traces in a first of the plurality of interconnect layers; a helmet dielectric film on the metal traces, wherein the helmet dielectric film comprises a first thickness on a top portion of the metal traces and a second thickness on sidewalls of the metal traces, the first thickness being greater than the second thickness; and interlayer dielectric material adjacent the helmet dielectric films.

[0062] In some embodiments, the helmet dielectric film comprises a conformality of between about 15% and 20%. Some embodiments also include openings in the helmet dielectric film filled with interconnect material. In some embodiments, the interconnect material conductively couples two or more of the metal traces. In some embodiments, the helmet dielectric film comprises a silicon nitride. In some embodiments, the helmet dielectric film comprises silicon dioxide.

[0063] In another example, a system is provided comprising: a display subsystem; a wireless communication interface; and an integrated circuit device, the integrated circuit device comprising: a semiconductor circuit substrate; a plurality of interconnect layers on different planes on the substrate; a plurality of metal traces in a first of the plurality of interconnect layers; a helmet dielectric film on the metal traces, wherein the helmet dielectric film comprises a first thickness on a top portion of the metal traces and a second thickness on sidewalls of the metal traces, the second thickness being between about 15% and 20% of the first thickness; and interlayer dielectric material adjacent the helmet dielectric films.

[0064] In some embodiments, the helmet dielectric film comprises a sidewall thickness of about 2 nm and a top thickness of about 12 nm. Some embodiments also include openings in the helmet dielectric film filled with interconnect material. In some embodiments, the interconnect material conductively couples two or more of the metal traces. In some embodiments, the helmet dielectric film comprises a silicon nitride. In some embodiments, the helmet dielectric film comprises silicon dioxide.

[0065] In another example, a method is provided comprising: providing a temperature and a pressure for a chemical vapor deposition of dielectric material; introducing a precursor gas and a diluent gas proximate to an interconnect surface; and pulsing a supply of the precursor gas to form a non-conformal helmet film on the interconnect surface.

[0066] Some embodiments also include the helmet film having a conformality of about 15-20%. In some embodiments, the precursor gas comprises a gas chosen from the group consisting of: silane, dichlorosilane, and tetraethylorthosilicate. In some embodiments, the helmet film comprises a dielectric chosen from the group consisting of: a silicon nitride and a silicon dioxide. In some embodiments, the precursor and diluent gases are ionized to form a plasma. Some embodiments also include forming an opening in the helmet film and depositing interconnect material in the opening.

[0067] In another example, a method of performing a plasma enhanced chemical vapor deposition (PECVD) is provided comprising: providing a diluent gas; providing a precursor gas; ionizing the diluent and precursor gases to form a plasma; and adjusting a supply of the precursor gas during a dielectric deposition on one or more metal traces on a circuit substrate to form non-conformal helmet films.

[0068] In some embodiments adjusting the supply of the precursor gas comprises alternating between intervals of a low supply of the precursor gas and intervals of a regular supply of the precursor gas. In some embodiments, the low supply of the precursor gas comprises substantially turning off the supply of the precursor gas. In some embodiments, the intervals of the low supply of the precursor gas and the intervals of the regular supply of the precursor gas comprise disparate durations. In some embodiments, the intervals of the low supply of the precursor gas comprise varying durations. In some embodiments, the intervals of the regular supply of the precursor gas comprise varying durations. In some embodiments, the precursor gas comprises a gas chosen from the group consisting of: silane, dichlorosilane, and tetraethylorthosilicate.

[0069] In another example, a reaction chamber for performing chemical vapour deposition (CVD) is provided comprising: means for providing a diluent gas; means for

providing a precursor gas; means for ionizing the diluent and precursor gases to form a plasma; and means for adjusting a supply of the precursor gas during a dielectric deposition on one or more metal traces on a circuit substrate to form non-conformal helmet films.

[0070] In some embodiments, the means for adjusting the supply of the precursor gas comprises means for alternating between intervals of a low supply of the precursor gas and intervals of a regular supply of the precursor gas. In some embodiments, the low supply of the precursor gas comprises substantially turning off the supply of the precursor gas. In some embodiments, the intervals of the low supply of the precursor gas and the intervals of the regular supply of the precursor gas comprise disparate durations.

[0071] In some embodiments, the intervals of the low supply of the precursor gas comprise varying durations. In some embodiments, the intervals of the regular supply of the precursor gas comprise varying durations. Some embodiments also include means to provide a pressure of about 100 to 700 Torr. Some embodiments also include means to provide a temperature of about 350 to 1300 degrees C.

[0072] In another example, a method of patterning copper is provided comprising: providing a diluent gas; providing a precursor gas; ionizing the diluent and precursor gases to form a plasma; adjusting a supply of the precursor gas during a dielectric deposition on a patterning material over a dielectric layer to form non-conformal helmets; etching the dielectric layer through gaps between non-conformal helmets to form trenches; and electroplating the trenches with copper.

[0073] In some embodiments adjusting the supply of the precursor gas comprises alternating between intervals of a low supply of the precursor gas and intervals of a regular supply of the precursor gas. In some embodiments, the low supply of the precursor gas comprises substantially turning off the supply of the precursor gas. In some embodiments, the intervals of the low supply of the precursor gas and the intervals of the regular supply of the precursor gas comprise disparate durations. In some embodiments, the intervals of the low supply of the precursor gas comprise varying durations. In some embodiments, the intervals of the regular supply of the precursor gas comprise varying durations. In some embodiments, the precursor gas comprises a gas chosen from the group consisting of: silane, dichlorosilane, and tetraethylorthosilicate.

[0074] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby

incorporated into the detailed description, with each claim standing on its own as a separate embodiment.

CLAIMS

We claim:

1. An apparatus comprising:
 - a semiconductor circuit substrate;
 - a plurality of interconnect layers on different planes on the substrate;
 - a plurality of metal traces in a first of the plurality of interconnect layers;
 - a helmet dielectric film on the metal traces, wherein the helmet dielectric film comprises a first thickness on a top portion of the metal traces and a second thickness on sidewalls of the metal traces, the first thickness being greater than the second thickness;
 - and
 - interlayer dielectric material adjacent the helmet dielectric film.
2. The apparatus of claim 1, wherein the helmet dielectric film comprises a conformality of between about 15% and 20%.
3. The apparatus of claim 2, further comprising openings in the helmet dielectric film filled with interconnect material.
4. The apparatus of claim 3, further comprising wherein the interconnect material conductively couples two or more of the metal traces.
5. The apparatus according to any one of claims 1 to 4, wherein the helmet dielectric film comprises a silicon nitride.
6. The apparatus according to any one of claims 1 to 4, wherein the helmet dielectric film comprises silicon dioxide.
7. A system comprising:
 - a display subsystem;
 - a wireless communication interface; and
 - an integrated circuit device, the integrated circuit device comprising:
 - a semiconductor circuit substrate;
 - a plurality of interconnect layers on different planes on the substrate;
 - a plurality of metal traces in a first of the plurality of interconnect layers;

a helmet dielectric film on the metal traces, wherein the helmet dielectric film comprises a first thickness on a top portion of the metal traces and a second thickness on sidewalls of the metal traces, the second thickness being between about 15% and 20% of the first thickness; and interlayer dielectric material adjacent the helmet dielectric films.

8. The system of claim 7, wherein the helmet dielectric film comprises a sidewall thickness of about 2 nm and a top thickness of about 12 nm.
9. The system of claim 8, further comprising openings in the helmet dielectric film filled with interconnect material.
10. The system of claim 9, further comprising wherein the interconnect material conductively couples two or more of the metal traces.
11. The system of any of claims 7 to 10, wherein the helmet dielectric film comprises a silicon nitride.
12. The system of any of claims 7 to 10, wherein the helmet dielectric film comprises silicon dioxide.
13. A method comprising:
 - providing a temperature and a pressure for a chemical vapor deposition of dielectric material;
 - introducing a precursor gas and a diluent gas proximate to an interconnect surface;
 - and
 - pulsing a supply of the precursor gas to form a non-conformal helmet film on the interconnect surface.
14. The method of claim 13, further comprising the helmet film having a conformality of about 15-20%.
15. The method of claim 13, wherein the precursor gas comprises a gas chosen from the group consisting of: silane, dichlorosilane, and tetraethylorthosilicate.

16. The method of claim 13, wherein the helmet film comprises a dielectric chosen from the group consisting of: a silicon nitride and a silicon dioxide.
17. The method according to any one of claims 13 to 16, wherein the precursor and diluent gases are ionized to form a plasma.
18. The method according to any one of claims 13 to 16, further comprising forming an opening in the helmet film and depositing interconnect material in the opening.
19. A method of performing a plasma enhanced chemical vapor deposition (PECVD) comprising:
 - providing a diluent gas;
 - providing a precursor gas;
 - ionizing the diluent and precursor gases to form a plasma; and
 - adjusting a supply of the precursor gas during a dielectric deposition on one or more metal traces on a circuit substrate to form non-conformal helmet films.
20. The method of claim 19, wherein adjusting the supply of the precursor gas comprises alternating between intervals of a low supply of the precursor gas and intervals of a regular supply of the precursor gas.
21. The method of claim 20, wherein the low supply of the precursor gas comprises substantially turning off the supply of the precursor gas.
22. The method of claim 20, wherein the intervals of the low supply of the precursor gas and the intervals of the regular supply of the precursor gas comprise disparate durations.
23. The method of any of claims 20 to 22, wherein the intervals of the low supply of the precursor gas comprise varying durations.
24. The method of any of claims 20 to 22, wherein the intervals of the regular supply of the precursor gas comprise varying durations.

25. The method of any of claims 19 to 22, wherein the precursor gas comprises a gas chosen from the group consisting of: silane, dichlorosilane, and tetraethylorthosilicate.

AMENDED CLAIMS**received by the International Bureau on 01 May 2018 (01.05.2018)**

26. An apparatus comprising:
- a substrate comprising semiconductor material;
 - two or more interconnect layers on different planes on the substrate;
 - one or more traces comprising metal in a first of the two or more interconnect layers;
 - a helmet film comprising dielectric material on the traces, wherein the helmet film comprises a first thickness on a top portion of the traces and a second thickness on sidewalls of the traces, the first thickness being greater than the second thickness; and
 - interlayer dielectric material adjacent the helmet film.
27. The apparatus of claim 26, wherein the helmet film comprises a conformality of between about 15% and 20%.
28. The apparatus of claim 27, further comprising openings in the helmet film filled with interconnect material.
29. The apparatus of claim 28, wherein the interconnect material conductively couples two or more of the traces.
30. The apparatus according to any one of claims 26 to 29, wherein the helmet film comprises a silicon nitride.
31. The apparatus according to any one of claims 26 to 29, wherein the helmet film comprises silicon dioxide.
32. A system comprising:
- a display subsystem;
 - a wireless communication interface; and
 - an integrated circuit device, the integrated circuit device comprising:

a substrate comprising dielectric material;
two or more interconnect layers on different planes on the substrate;
one or more traces comprising metal in a first of the two or more interconnect layers;
a helmet film comprising dielectric material on the traces, wherein the helmet film comprises a first thickness on a top portion of the traces and a second thickness on sidewalls of the traces, the second thickness being between about 15% and 20% of the first thickness; and
interlayer dielectric material adjacent the helmet film.

33. The system of claim 32, wherein the helmet film comprises a sidewall thickness of about 2 nm and a top thickness of about 12 nm.
34. The system of claim 33, further comprising openings in the helmet film filled with interconnect material.
35. The system of claim 34, wherein the interconnect material conductively couples two or more of the traces.
36. The system of any of claims 32 to 35, wherein the helmet film comprises a silicon nitride.
37. The system of any of claims 32 to 35, wherein the helmet film comprises silicon dioxide.
38. A method comprising:
 providing a temperature and a pressure for a chemical vapor deposition of dielectric material;
 introducing a precursor gas and a diluent gas proximate to an interconnect surface;
 and
 pulsing a supply of the precursor gas to form a non-conformal helmet film on the interconnect surface.

39. The method of claim 38, further comprising the helmet film having a conformality of about 15-20%.
40. The method of claim 38, wherein the precursor gas includes a gas comprising silane, dichlorosilane, or tetraethylorthosilicate.
41. The method of claim 38, wherein the helmet film comprises a dielectric chosen from the group consisting of: a silicon nitride and a silicon dioxide.
42. The method according to any one of claims 38 to 41, wherein the precursor and diluent gases are ionized to form a plasma.
43. The method according to any one of claims 38 to 41, further comprising forming an opening in the helmet film and depositing interconnect material in the opening.
44. A method of performing a plasma enhanced chemical vapor deposition (PECVD) comprising:
 providing a diluent gas;
 providing a precursor gas;
 ionizing the diluent and precursor gases to form a plasma; and
 adjusting a supply of the precursor gas during a dielectric deposition on one or more metal traces on a circuit substrate to form non-conformal helmet films.
45. The method of claim 44, wherein adjusting the supply of the precursor gas comprises alternating between intervals of a low supply of the precursor gas and intervals of a regular supply of the precursor gas.
46. The method of claim 45, wherein the low supply of the precursor gas comprises substantially turning off the supply of the precursor gas.
47. The method of claim 45, wherein the intervals of the low supply of the precursor gas and the intervals of the regular supply of the precursor gas comprise disparate durations.

48. The method of any of claims 45 to 47, wherein the intervals of the low supply of the precursor gas comprise varying durations.
49. The method of any of claims 45 to 47, wherein the intervals of the regular supply of the precursor gas comprise varying durations.
50. The method of any of claims 44 to 47, wherein the precursor gas includes a gas comprising silane, dichlorosilane, or tetraethylorthosilicate.

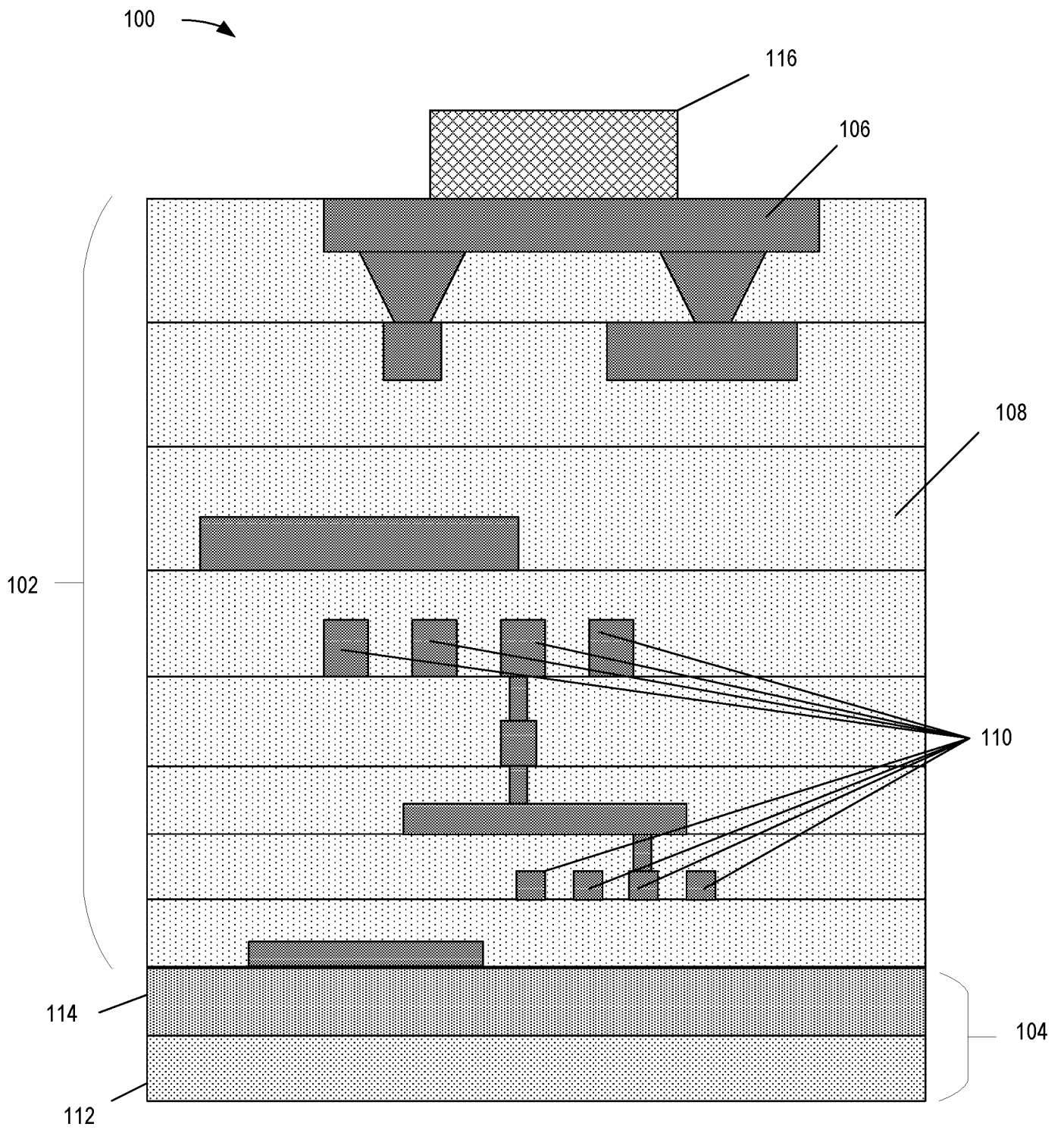


Fig. 1

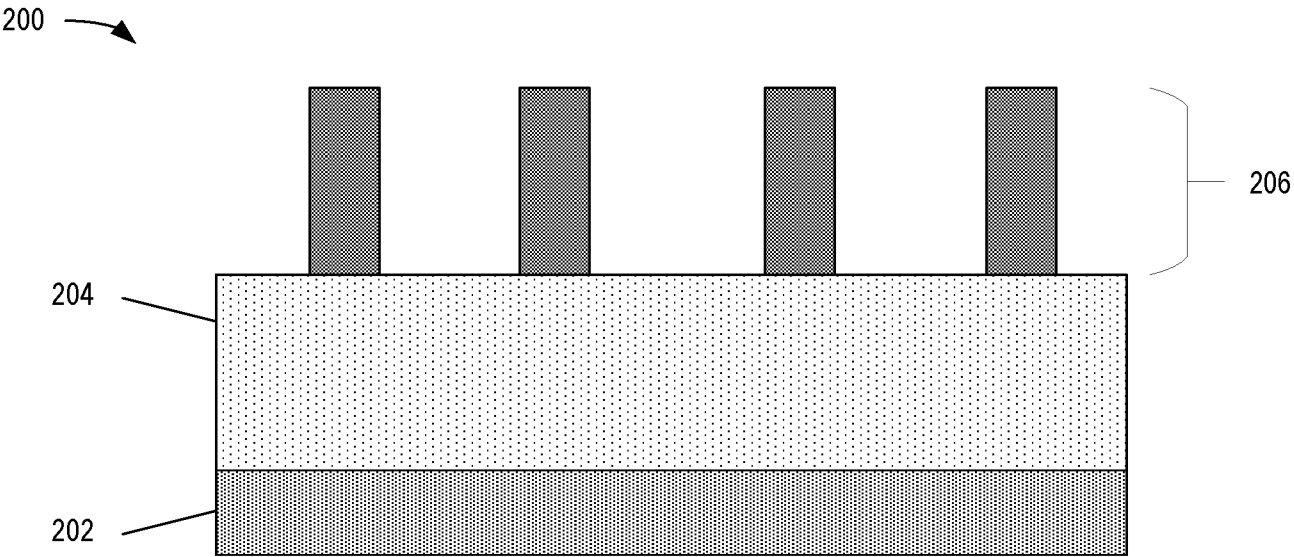


Fig. 2A

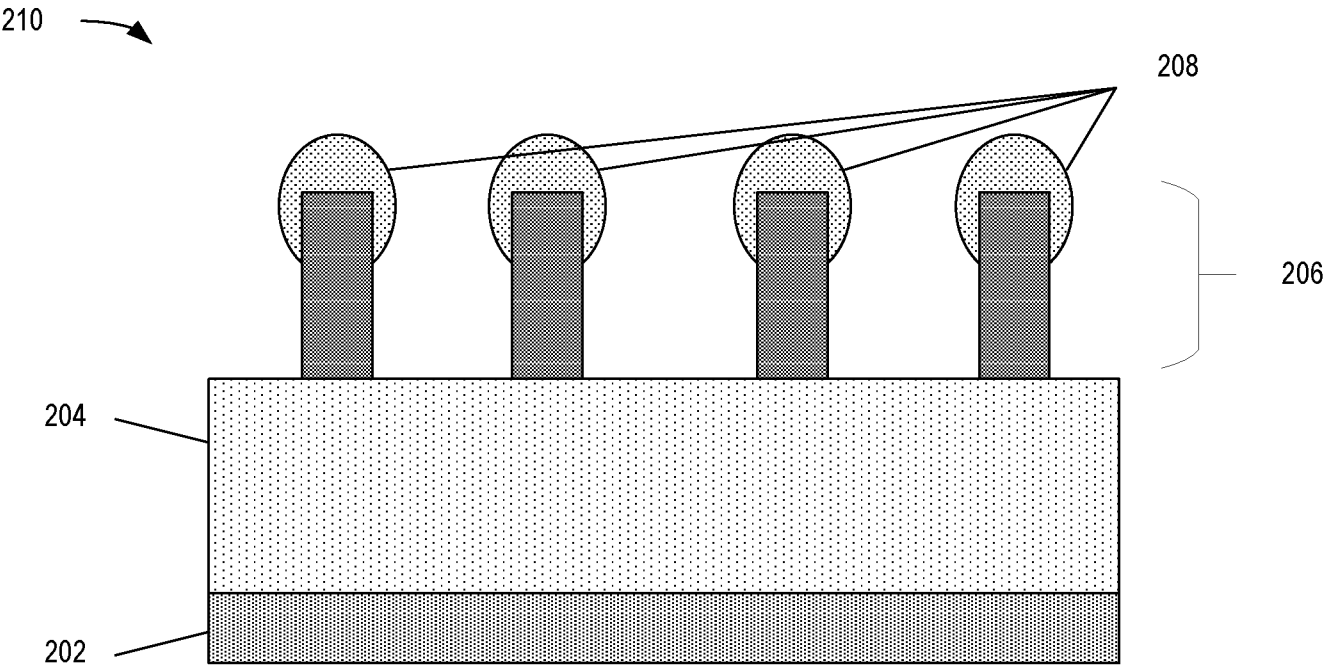


Fig. 2B

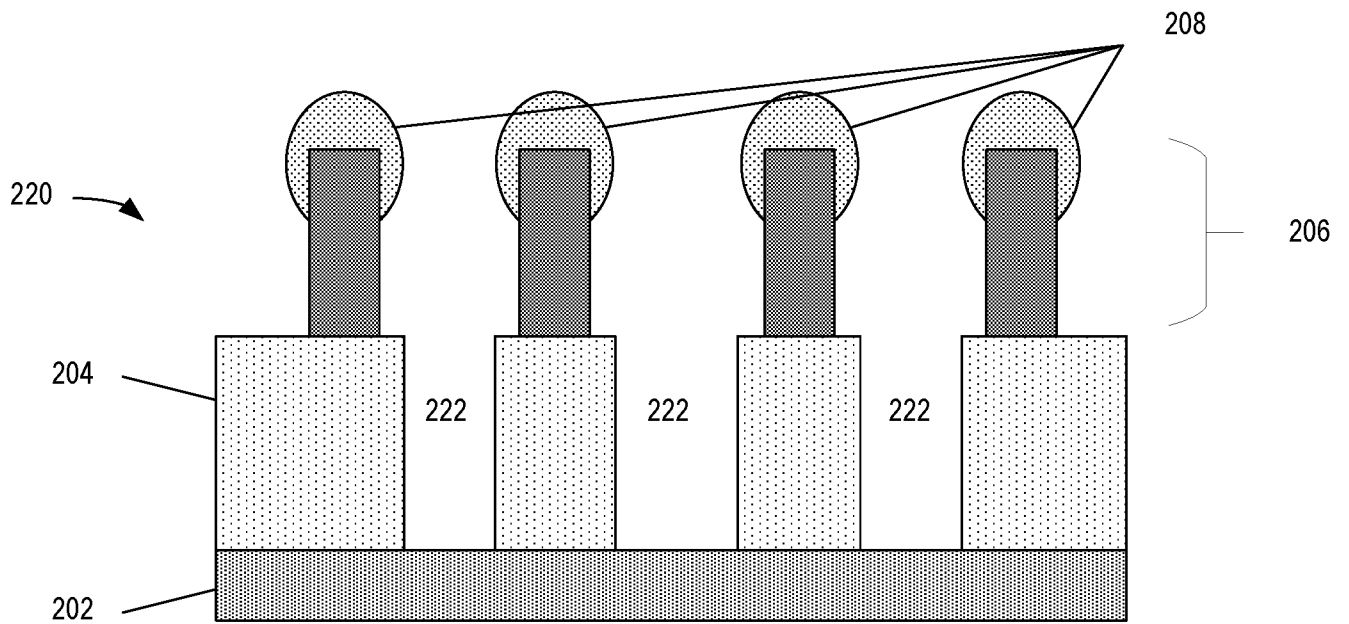


Fig. 2C

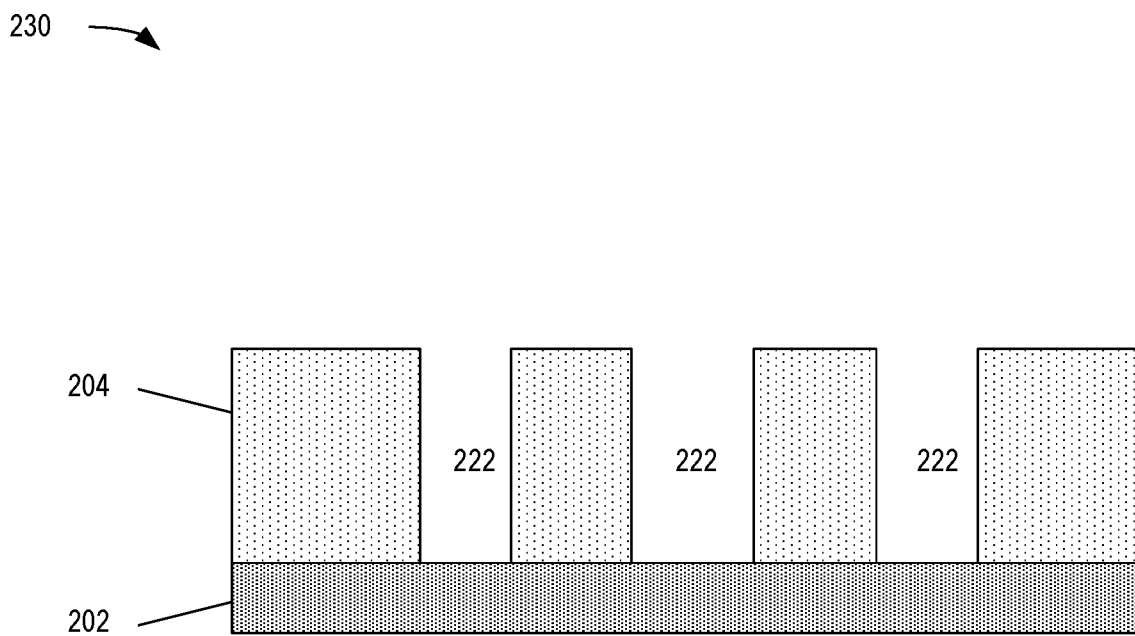


Fig. 2D

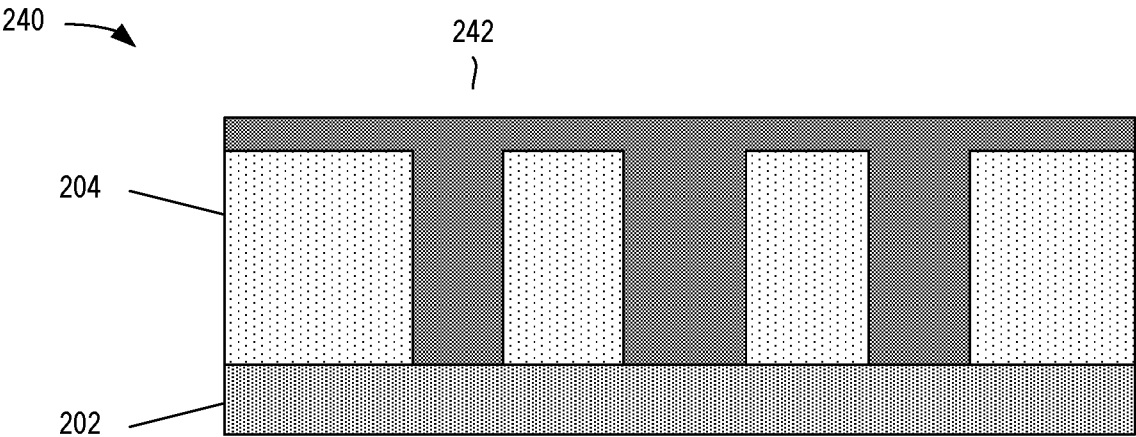


Fig. 2E

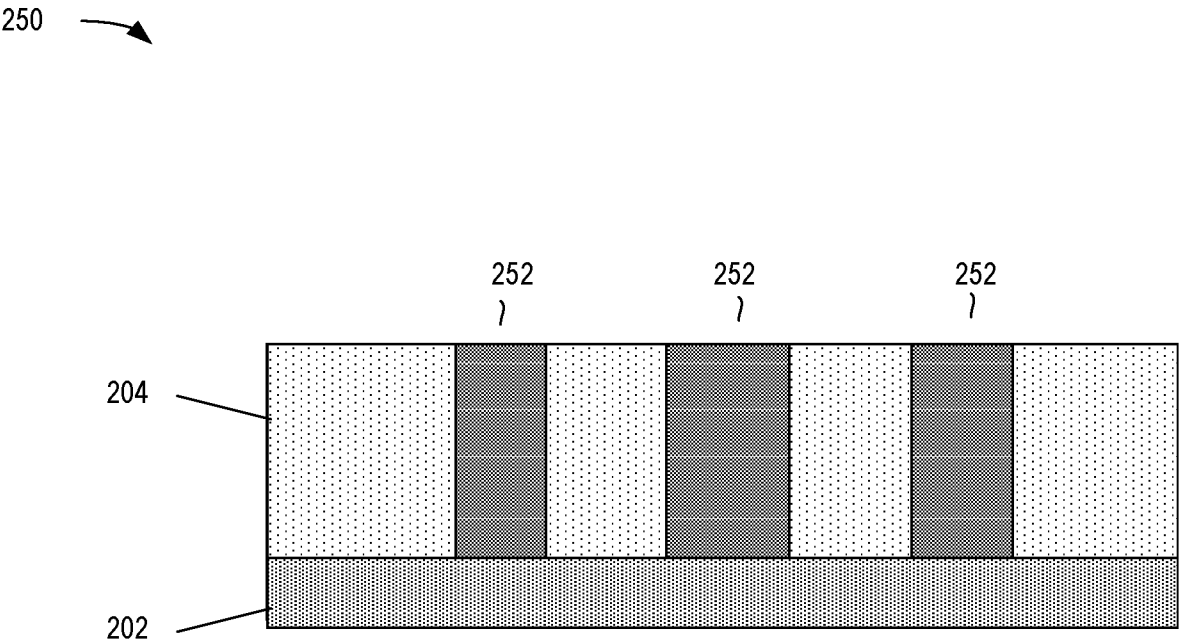


Fig. 2F

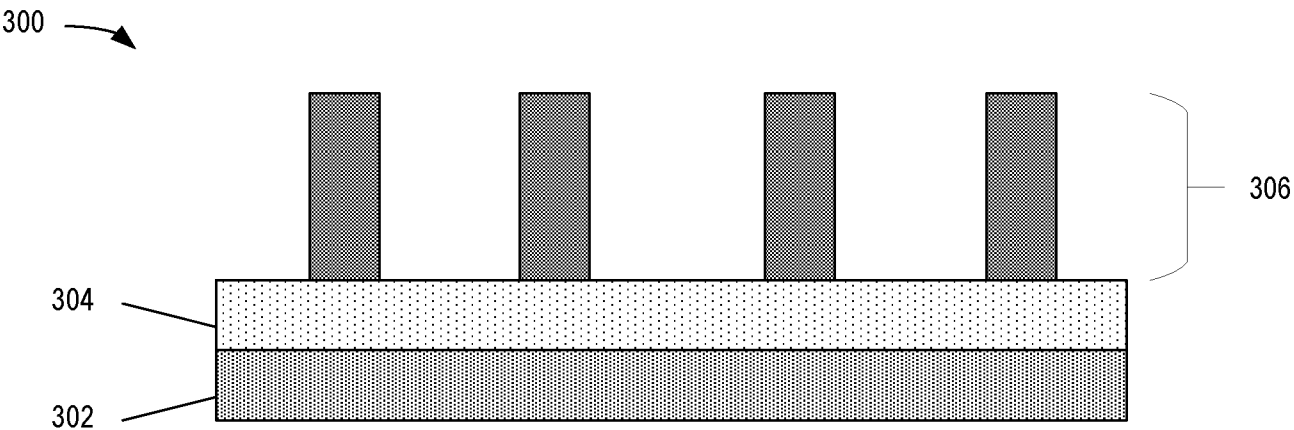


Fig. 3A

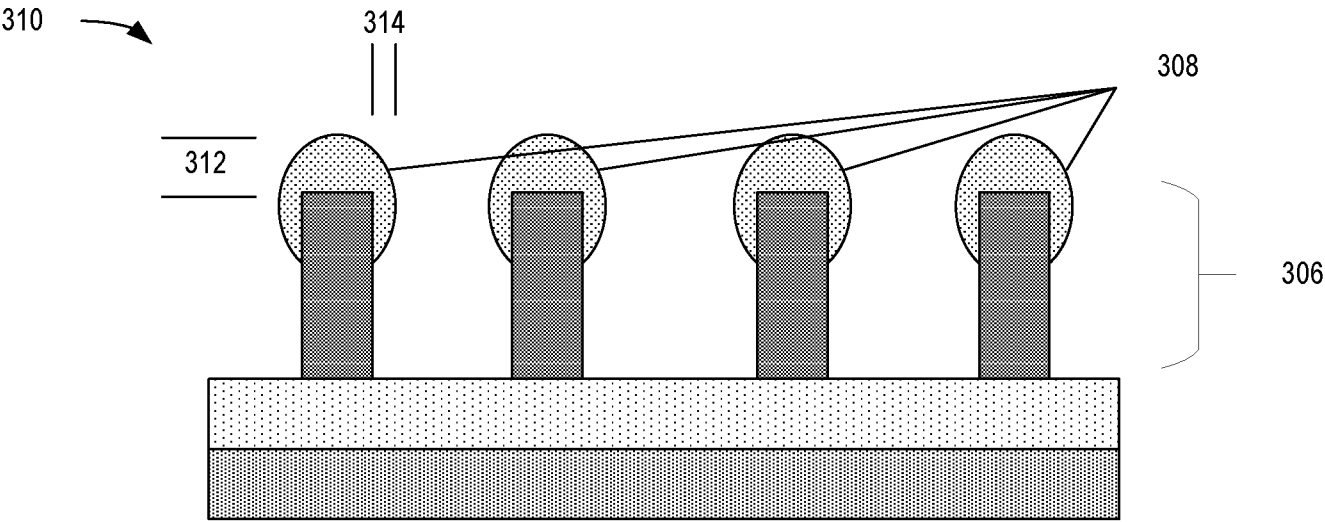
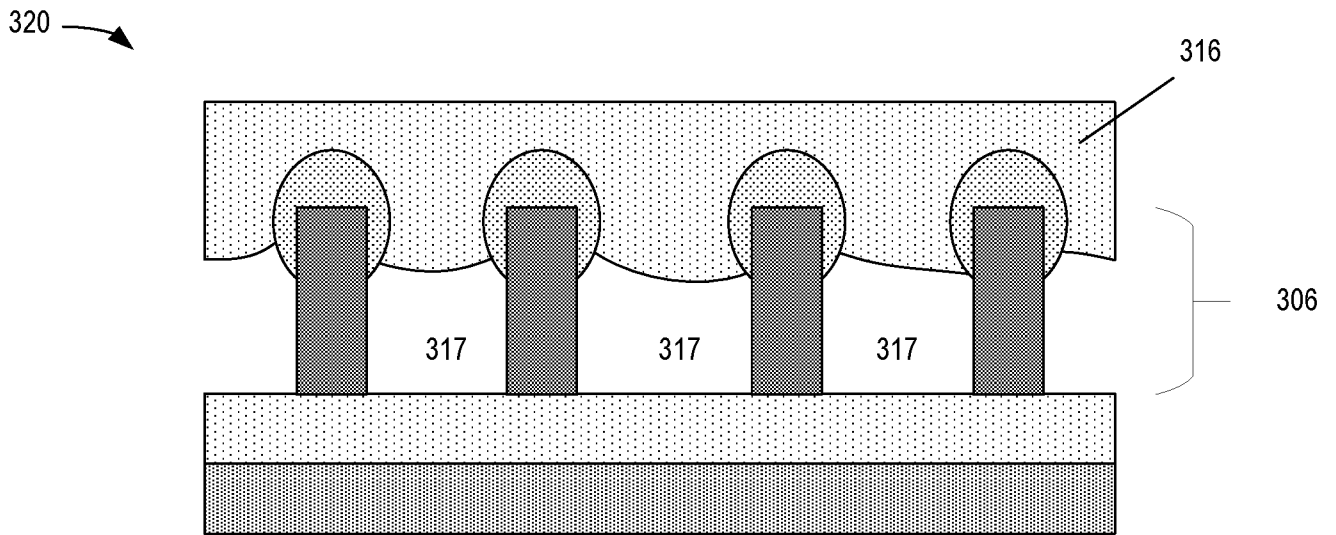
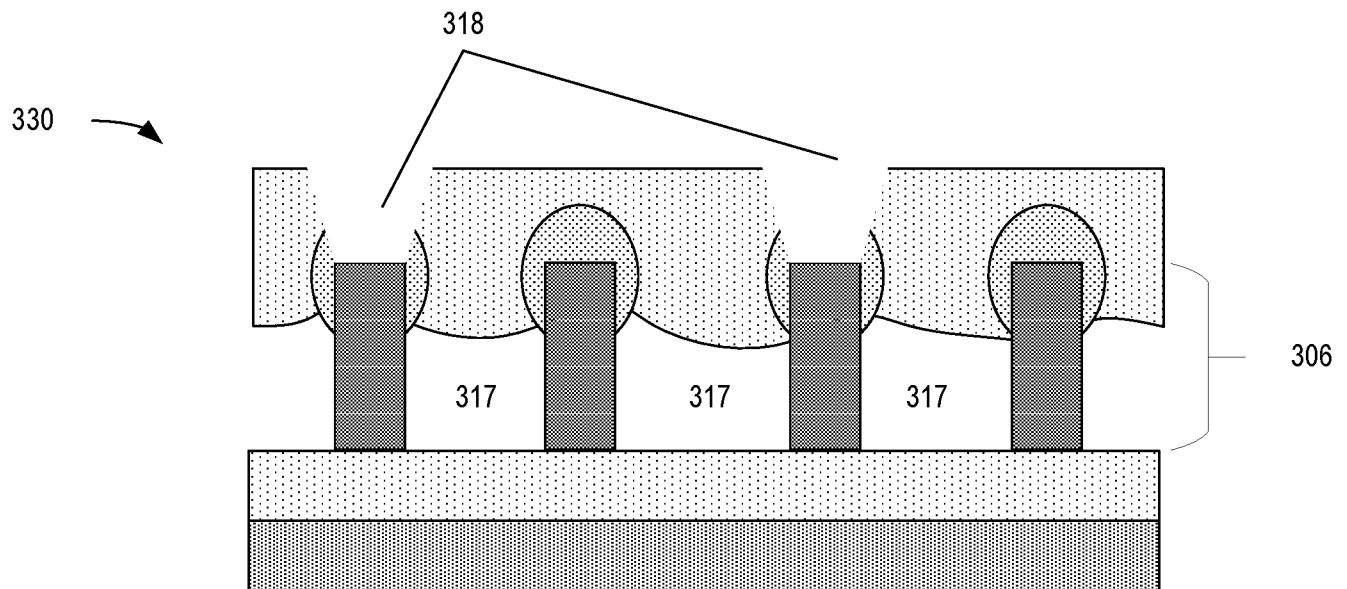


Fig. 3B

**Fig. 3C****Fig. 3D**

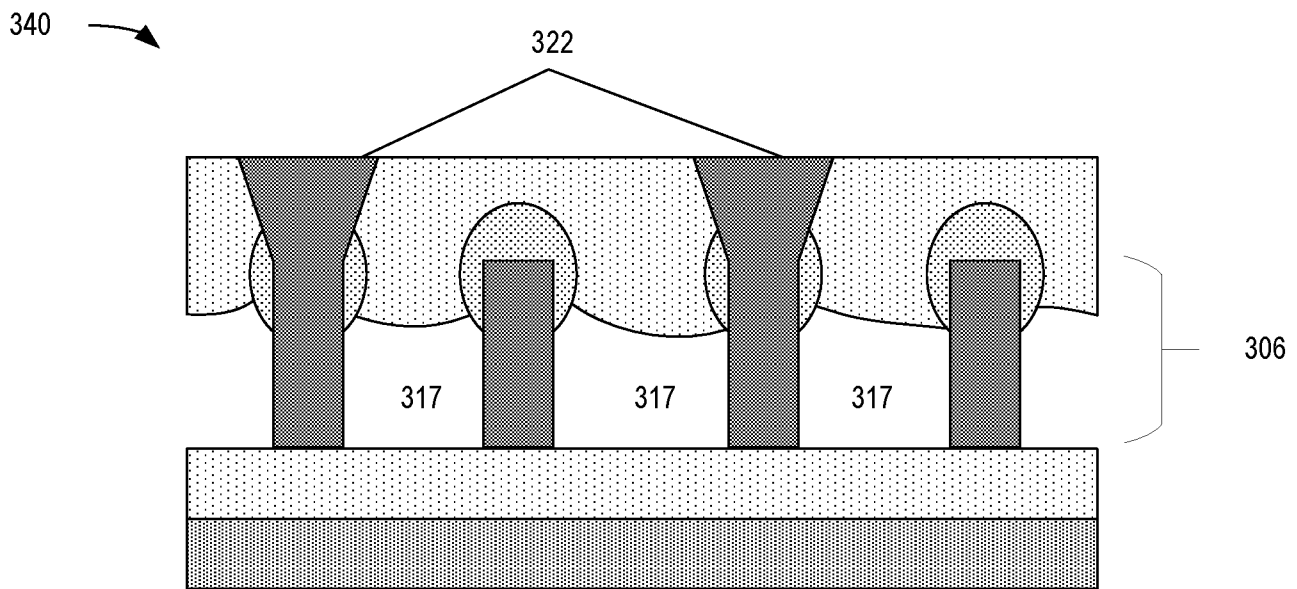


Fig. 3E

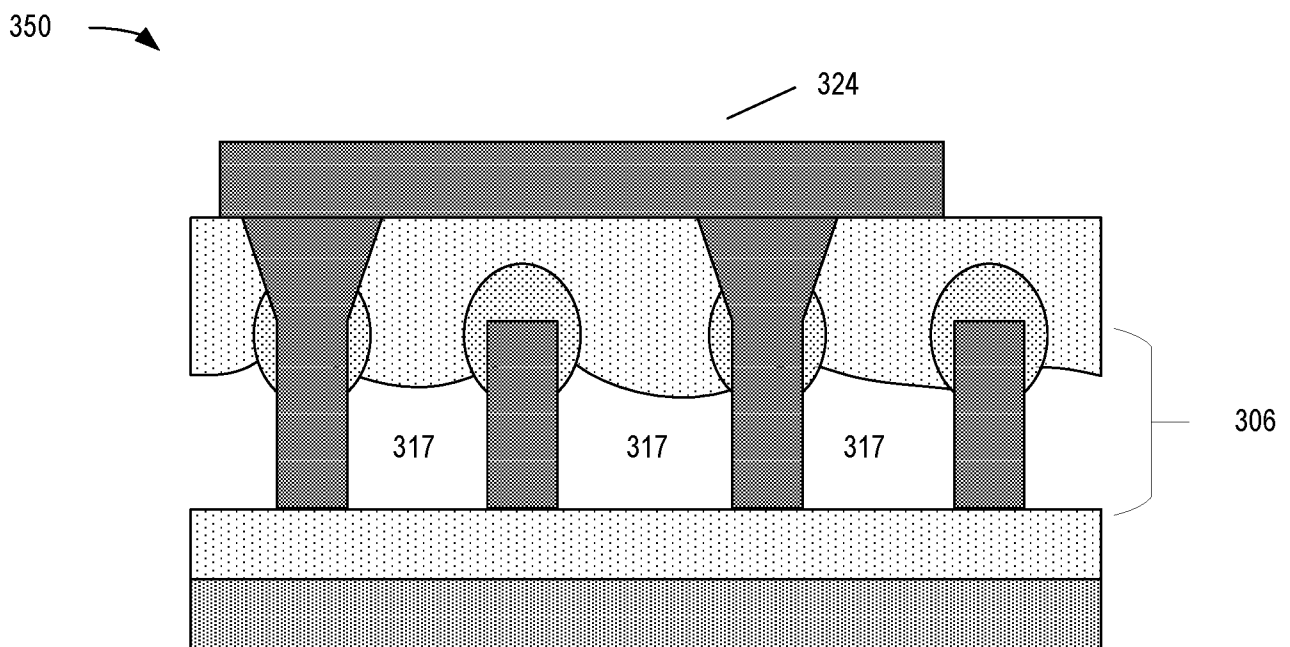


Fig. 3F

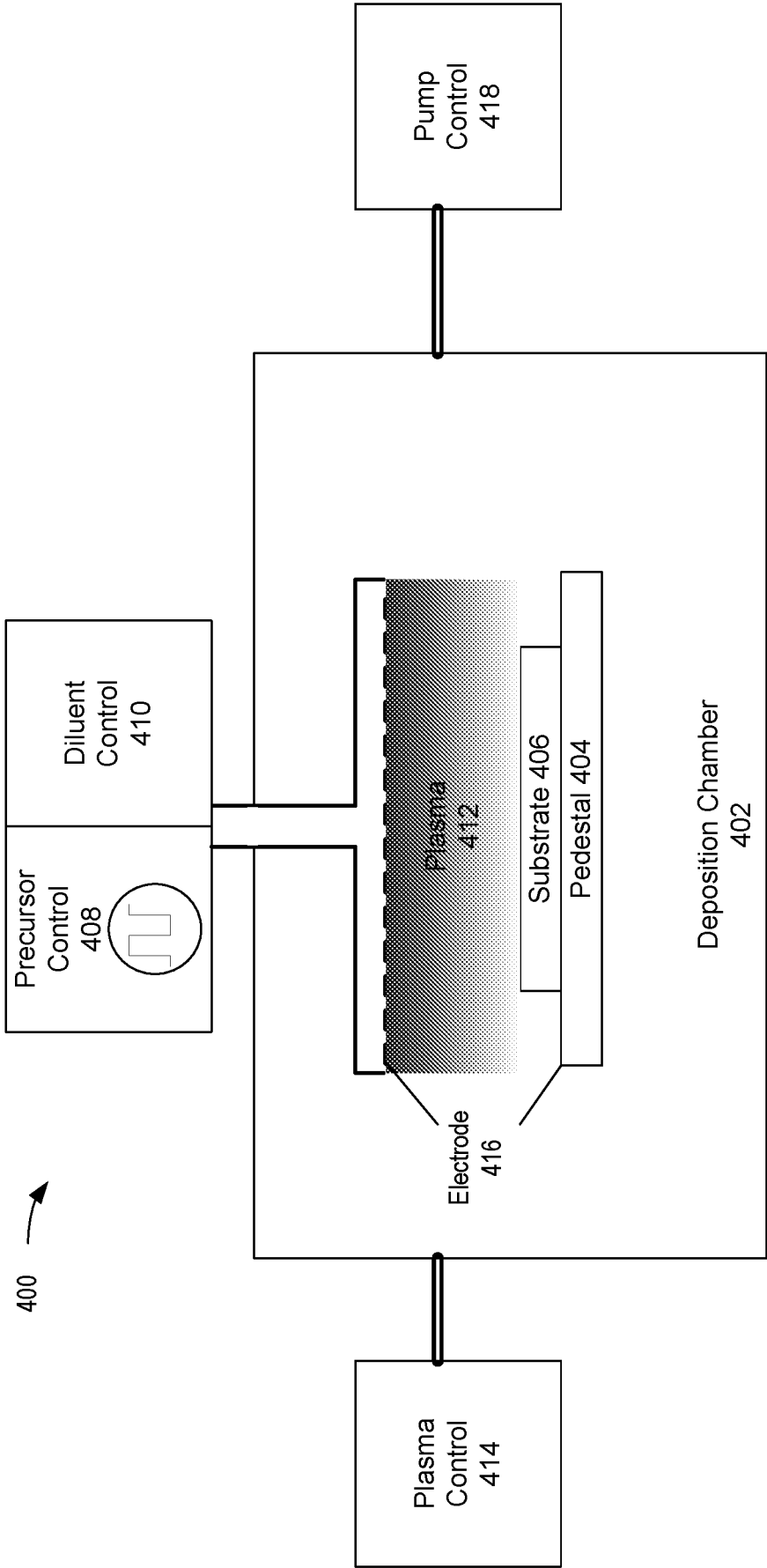
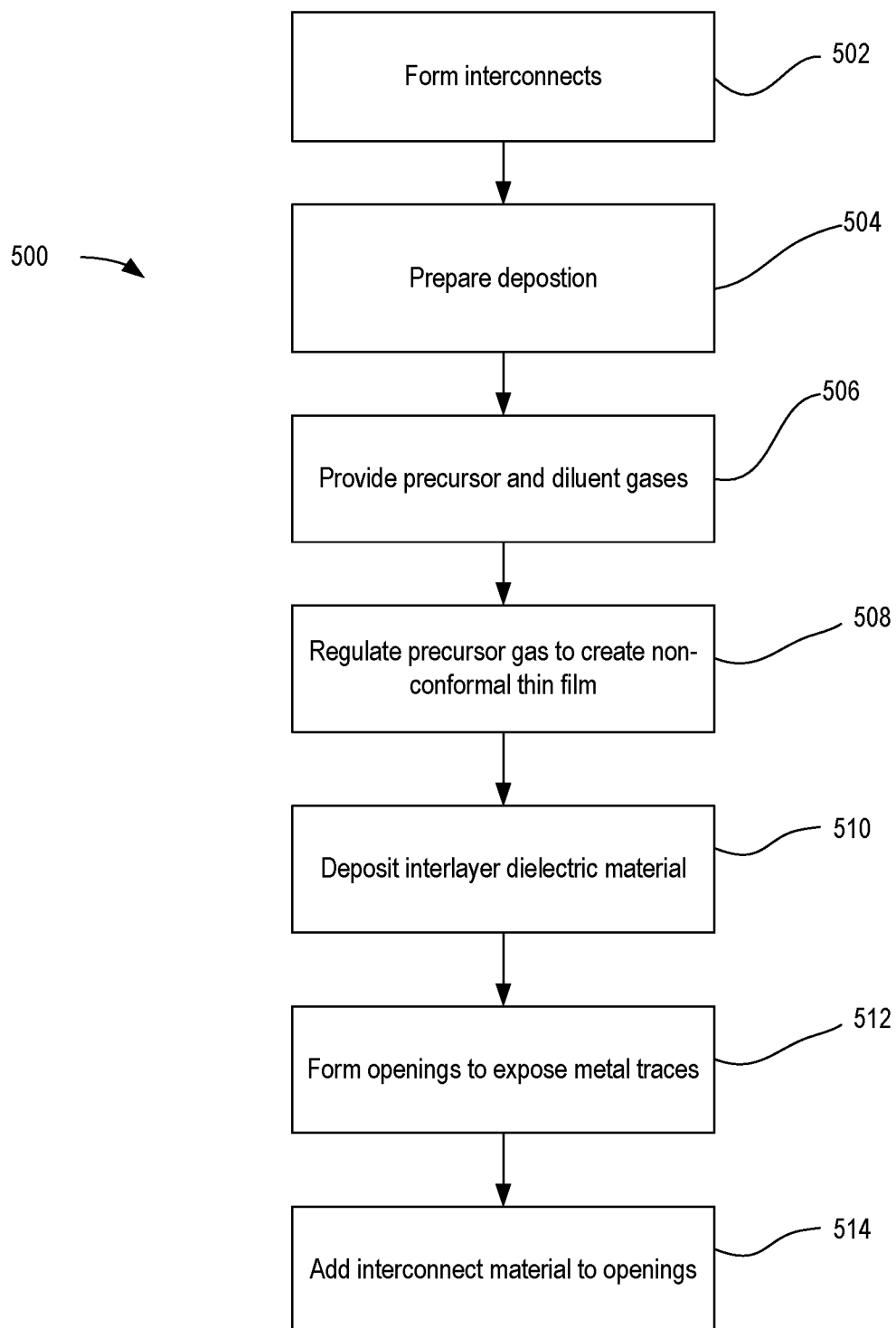


Fig. 4

**Fig. 5**

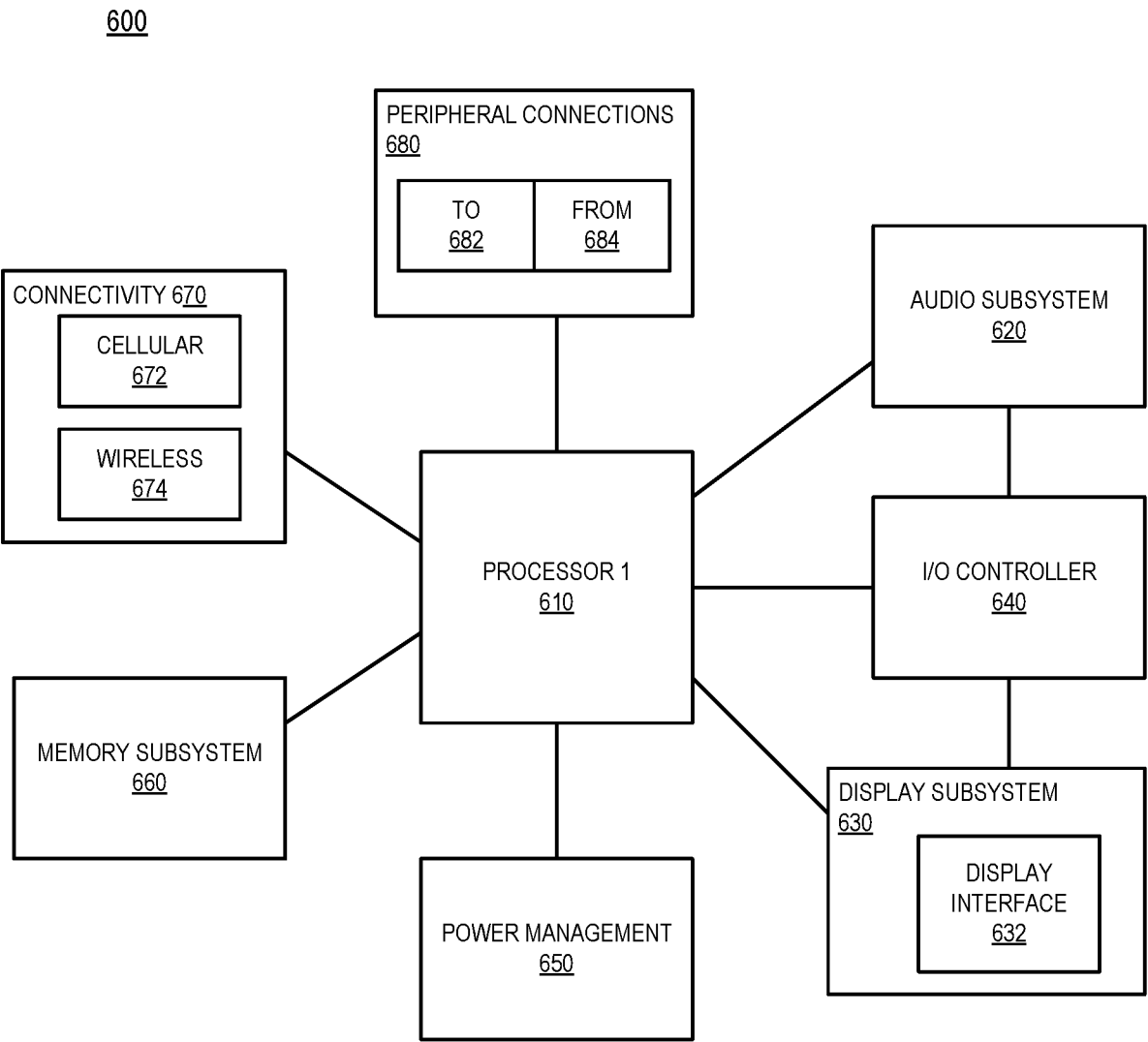


Fig. 6

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/768(2006.01)i, H01L 21/02(2006.01)i, H01L 21/205(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/768; H01L 23/52; H01L 21/764; H01L 21/02; H01L 21/31; H01L 23/532; H01L 21/205

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: substrate, trace, helmet dielectric, precursor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007-0246831 A1 (ZVONIMIR GABRIC et al.) 25 October 2007 See paragraphs [0081]-[0090] and figures 1-7.	1-12
A		13-25
Y	US 2009-0263951 A1 (JUNICHI SHIBATA et al.) 22 October 2009 See paragraphs [0105]-[0128] and figures 1-6.	1-12
Y	US 2016-0013133 A1 (QUALCOMM INCORPORATED) 14 January 2016 See paragraphs [0032]-[0040] and figures 1A-1G.	3-4, 9-10
A	US 2015-0214092 A1 (APPLIED MATERIALS, INC.) 30 July 2015 See paragraphs [0022]-[0066] and figures 1-4.	1-25
A	US 2012-0129356 A1 (JIN-GYUN KIM et al.) 24 May 2012 See paragraphs [0026]-[0031] and figures 1A-1C.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 September 2017 (28.09.2017)

Date of mailing of the international search report

28 September 2017 (28.09.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/069145

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