A display comprising a plurality of microdisplay tiles, each microdisplay tile comprising a plurality of emitters, wherein each emitter comprises at least one LED in particular an OLED or ILED. Control electronics are mounted to the back of each tile. Plural tiles can be connected together to create a larger display. The pixel pitch is maintained across adjacent tiles. The substrate upon which the LEDs are formed is the display surface and may be configured to manipulate the emitted light.

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.
Tile = ILED MicroDisplay consisting of an 4 x 4 array of ILED devices

ILED Devices (single and 3 way cluster device shown)

ILED Display consisting of a 3 x 3 array of ILED Tiles (microdisplays)

Figure 1
**Figure 2 (prior art)**

**Figure 3**

- Micro LEDs (bottom emitting through substrate)
- Sapphire Substrate / Screen
- GaN epimaterial
- IC (TFT) electrical chip mounted to back of microLED array for control circuitry
- Metal Contact (Anode)
- Planar Interdielectric Layer + Passivation
- Metal Contact (Cathode)
- Multilayer Metals
Display

TECHNICAL FIELD
The invention is related to a display and in particular to a display made from a plurality of smaller tiles.

BACKGROUND
ILED (Inorganic Light Emitting Diode) displays provide an alternative to the better known LCD (Liquid Crystal Display) and the OLED (Organic Light Emitting Diode) displays.

An ILED display does not have any of the drawbacks of LCD or OLED displays. Benefits of ILED displays include reduced power consumption relative to other available displays, high contrast and long-lifetime operation. The display will be highly uniform, have no dither, predictable colour gamma, ultra-fast response rates and negligible flicker.

A microdisplay is a display which typically has a diagonal dimension of < 2" (however, it can be any size as long as the yield and economic cost to manufacture are viable). These microdisplay sizes have niche applications for example in wearable and pico projection market segments.

Micro-arrays of ILEDs in microdisplays can be manufactured by hybrid or monolithic methods. For large area ILED displays, hybrid methods are considered as the preferred platform approach because of the scaling challenge in achieving high yields and uniformity across a large display area. This typically involves the preparation, disposition, handling and fine pitch placement of millions of R, G and B chips to form pixel of the ILED display. Recently, microprintheads have emerged as credible assembly method for high throughput low cost manufacture of large area ILED displays, as described for example in US 2011/0266561 A1.

SUMMARY
In monolithic architectures, a N x M ILED array or microdisplay is formed on a single transparent substrate without the need for individual packaging and assembly.
Each tile can then be further arrayed out to form a Display Module consist of N x M tiles (N = 4, M = 4 in example). The tiles may be four side tileable which allows tiles to be positioned together with minimal deadspace such that the μLED emitter pitch intra tile is preserved.

One key limitation of the monolithic tile is the ability to process R, G and B chips to create the pixel of a color display. Monolithic displays are typically monochrome. Methods however for generating color displays by monolithic means include near-UV ILED's optimised for coupling to light converting materials such as nano quantum dots materials to generate Red, Blue and Green light emission.

Hybrid display assembly is generally the preferred manufacturing approach for displays. This is because monolithic methods require high yield manufacturing methods and uniform material performance over the area of the microdisplay.

Monolithic displays are therefore best suited for niche microdisplays as they dispense with the need for placing and packaging individual chips.

It is recognised by the inventors, that there are certain situations where monolithic assembly of displays can be preferred both from a performance (high light extraction), form factor (display thickness and size) and economic reason. The economic viewpoint is on the basis that substrate material costs associated with sapphire and more recently silicon LED substrate materials is declining.

This coupled with the removal of the ILED chip preparation for microprint, complicated die pick and place assembly tooling and processes and key layers (i.e. the glass screen as disclosed in this invention) means that there is a need for monolithic microdisplay heads.

For the LED based microdisplay systems, high resolution monolithic array chip is known in the prior art. US2014/0008667 A1 discloses a method for fabricating a high resolution active matrix monolithic display by combining an LED micro-array and an Active Matrix (AM) panel using flip-chip methods. The array being fabrication on sapphire substrate with the active matrix panel using Silicon CMOS processes. The
microdisplay was realised in this invention by integrating the LED microarray and electronic CMOS processing by flip-chip methods.

The LED manufactured in this invention are top emitters whereby the light generated is emitted on the same side as the contacts upwards and away from the sapphire substrate. This design is limited in both the area of the microdisplay and its thickness. Specifically the micro-LED array and AM layers do not overlap directly (i.e. light cannot transmit through the AM substrate layer) and result in microdisplay head which is larger than the area of the micro-LED array area. In addition, the thickness of the display is governed by several factors most noticeably the thickness of the screen which is typically less than 800microns using gorilla glass. A solution therefore which can reduce or eliminate the glass screen thickness is desirable.

The display in US2014/0008667 invention does not facilitate the tiling to create a large display head. This is because of the deadspace afforded to wirebonding on the perimeter of the display. This invention discloses a method for minimising the perimeter deadspace in order to allow the tile together of several microdisplay parts to create a large area display head.

It should be recognised that while the focus of this IDF is on a monolithic tile the concept of tiling microdisplays manufactured by hybrid methods equally applies.

It is an object to minimise the perimeter deadspace of tiles in order to allow the tiling together of several microdisplay parts to create a large area display head. A small form factor ILED microdisplay tile which can be integrated directly to control electronics is proposed. The microdisplay tile consists of a monolithic piece of LED material where ILED devices are configured in an Nxm format.

The control electronics can be integrated directly underneath the microdisplay tile such that the tiles can be assembled in a N x M array of tiles to form a larger area module for a larger display head. The microdisplay is 4 side tileable which means that the further tiles can be butted to them on all four sides of the tile. The display head with this configuration can be planar or mounted on a flexible substrate to achieve a non rigid flexible display. An embodiment of this invention is that transparent substrate upon
which the ILEDs are grown and fabricated on the tile act as the primary screen for the microdisplay.

According to a first aspect, there is provided a display comprising a plurality of microdisplay tiles, each microdisplay tile comprising a plurality of emitters, each emitter comprising at least one LED.

Optionally, each LED is selected from any of an OLED and an ILED.

The display optionally comprises control electronics mounted to an underside of each tile. As an option, the control electronics have a surface area no greater than the tile. As a further option, the display further comprises a ball grid array mounted to the control electronics.

Optionally, each microdisplay tile is two r-sided and configured to be disposed to adjacent microdisplay tiles on each side. Alternatively, each microdisplay tile is three-sided and configured to be disposed to adjacent microdisplay tiles on each side. Alternatively, each microdisplay tile is four-sided and configured to be disposed to adjacent microdisplay tiles on two sides.

As an option, each microdisplay tile comprises a connector arranged to connect the microdisplay tile to an adjacent microdisplay tile.

As an option, each microdisplay tile is formed on a substrate, the substrate forming a screen of the microdisplay. The screen is optionally configured to manipulate emitted light. As a further option, the screen comprises quantum dots configured to post-process emitted light.

Optionally, a pitch of the emitters is maintained across adjacent microdisplay tiles.

According to a second aspect, there is provided a microdisplay tile comprising a plurality of emitters, each emitter comprising at least one LED, the microdisplay tile further comprising means to connect to the microdisplay tile to at least one adjacent microdisplay tile.
Optionally, each LED is selected from any of an OLED and an ILED.

The microdisplay tile optionally comprises control electronics mounted to an underside of each tile. As a further option the control electronics have a surface area no greater than the tile. As a further option the microdisplay tile further comprises a ball grid array mounted to the control electronics.

As an option the microdisplay tile is four-sided and configured to be disposed to adjacent microdisplay tiles on each side. As an alternative, the microdisplay tile is three-sided and configured to be disposed to adjacent microdisplay tiles on each side. Alternatively, the microdisplay tile is four-sided and configured to be disposed to adjacent microdisplay tiles on two sides.

As an option, each microdisplay tile is formed on a substrate, the substrate forming a screen of the microdisplay. The screen is optionally configured to manipulate emitted light. As an option, the screen comprises quantum dots configured to post-process emitted light.

According to a third aspect, there is provided a method of manufacturing a display, the method comprising connecting an array of a plurality of microdisplay tiles, each microdisplay tile comprising a plurality of emitters, each emitter comprising at least one LED.

The method optionally comprises manufacturing each microdisplay tile using either monolithic fabrication or hybrid assembly.

The method optionally further comprises growing each of the plurality of emitters epitaxially on a common substrate.

The method optionally further comprises providing a mesa at each emitter of the plurality of emitters.

The method optionally further comprises providing an active layer within each mesa.
BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates schematically a plan view of how ILED displays, tiles and devices relate to one another;

Figure 2 illustrates schematically in a side elevation cross-section view a ‘bottom emitting’ ILED;

Figure 3 illustrates a side elevation cross section view of an exemplary ILED Tile or MicroDisplay with IC chips mounted directly to a backside of a MicroLED array; and

Figure 4 illustrates a side elevation cross section view of an exemplary BGA Style ILED microdisplay for mounting to a control electronics motherboard.

DETAILED DESCRIPTION

The following definitions and abbreviations are used herein:

<table>
<thead>
<tr>
<th>Emitter</th>
<th>The smallest unit cell of the display. This includes a single or cluster of μLED diodes</th>
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<tbody>
<tr>
<td>MicroDisplay tile</td>
<td>A tile consisting of an array of ILED devices grown/fabricated on a common transparent substrate</td>
</tr>
<tr>
<td>Display Module</td>
<td>An array of MicroDisplay tiles arranged in a mosaic format to create a large area display module</td>
</tr>
<tr>
<td>Single Emitter Chip (SEC)</td>
<td>An LED chips with only 1 emitting region. Generally the whole chip will illuminate</td>
</tr>
<tr>
<td>Addressable Array Chip (AAC)</td>
<td>An LED chip which has more than 1 distinct light generating region that can be independently addressed. This is equivalent to the definition of tile or microdisplay above</td>
</tr>
<tr>
<td>Addressable Array Element (AAE)</td>
<td>An independently addressable emitting area in an Addressable Array Chip</td>
</tr>
</tbody>
</table>

The inventors have appreciated that there is a substantial need to reduce the overall thickness and overall form factor for microdisplays.

This inventors have also recognised the need to manufacture a small area microdisplay module where the total area of the module is equivalent in area to the area of the ILED array itself.
There is described a method which replaces the glass screen of the display with the sapphire substrate of the MicroDisplay. The solution is only viable whereby the light emission from the ILED is through the substrate and the ILED contacts are on the opposite face away from the sapphire substrate.

Figure 1 shows an exemplary μLED Display. The display consists of individual or cluster emitters which are configured into a tile consisting of N x M array of emitters (N=4, M =4 in example). The emitters are manufactured by monolithic manufacturing methods, although hybrid methods may also be used. Each tile can then be further arrayed out to form a Display Module consist of N x M tiles (N = 3, M = 3 in example). The tiles are four side tileable which allows tiles to be positioned together with minimal deadspace such that the μLED emitter pitch intra tile is preserved.

A micro-LED structure is proposed in WO 2004/097947 (US 7,518,149) with a high EE because of its shape. Such a micro-LED 100 is shown in Figure 2, wherein a substrate 102 has a semiconductor epitaxial layer 104 located on it. The epitaxial layer 104 is shaped into a mesa 106. An active (or light emitting) layer 108 is enclosed in the mesa structure 106. The mesa 106 has a truncated top, on a side opposed to a light transmitting or emitting face 110. The mesa 106 also has a near-parabolic shape to form a reflective enclosure for light generated or detected within the device. The arrows 112 show how light emitted from the active layer 108 is reflected off the walls of the mesa 106 toward the light exiting surface 110 at an angle sufficient for it to escape the LED device 100 (i.e. within the angle of total internal reflection).

The term "quasi-collimated" is used herein to define the light confined within the critical escape angle of an LED device. Light generated in the active layer must exit either: (a) directly through an exit face without reflection on the mesa sidewall; (b) via a single reflection on the mesa sidewall resulting in an incident angle to the exit face within the critical angle range; or (c) following multiple reflections within the mesa structure. This is shown in Figure 1.

The inventors have identified that a monolithic Addressable Array Chip microdisplay or tile using an array of ILED devices has the following advantages:
1. In this configuration the control chips are mounted directly underneath the MicroDisplay to form an integrated 3D packaged display.

2. The glass screen on the display is removed and replaced by the sapphire substrate of the MicroDisplay itself.

3. The total thickness of the display is determined by the sapphire substrate (200μm by way of example) and the thickness of the IC chips

4. A monolithic method like this allows for the production of larger microdisplays heads by tiling them together on all four sides of the tile.

5. Additional post processing is carried out on the backside of the microLED array via spin coating, multilevel metal and dielectric planarisation layering in order to integrate IC components directly on the backside of the display. The backside interconnects metal tracks for cathode and anode of each chip are processed and planarised for mounting discrete IC chips for active drive circuitry using for example low temperature conductive adhesive bonding.

6. Alternatively the electronics can be connected to the micodisplay by flip-chip mounting directly the microLED array to control circuitry using a suitable bonding process. Figure 4 illustrates a micro-BGA type package.

7. The top sapphire surface of the display (the screen) can be further processed with additive layers such as finger sensors or machined in order to manipulate and control the light generated.

8. The top surface of the display (the screen) can be further processed with nanocrystal materials ink /dot dispensed to change the light emission wavelength of ILED emitters of the display.

9. The display eliminates complex ILED chip preparation and assembly by Hybrid assembly methods.
A module is described which combines ILED Display Head formed by monolithic LED display fabrication.

Figure 3 shows a side elevation cross section view of an exemplary ILED Tile or MicroDisplay with IC chips mounted directly to a backside of a MicroLED array. Ribbon cable for external connection is not shown.

Figure 4 illustrates a side elevation cross section view of an exemplary BGA Style ILED microdisplay for mounting to a large control electronics motherboard.

Whilst specific embodiments of the invention are described above, it will be appreciated that a number of modifications and alterations may be made thereto without departing from the scope of the invention as defined in the appended claims.

Numbered clauses
1. A method of forming a display head arrangement for use in display applications, the method comprising a microdisplay and tiling a plurality of microdisplays on a carrier to form a larger Display Module.
2. An inorganic LED, ILED, microdisplay device comprising: a monolithic block of ILED emitters designed in a predefined matrix in X and Y to form a 2 dimensional ILED microdisplay. each ILED chip comprising of transparent substrate; an epitaxial layer grown on the substrate wherein at least a portion of the substrate and the LED epitaxial layers define a mesa;
3. Where the electronics are designed such that they are of similar dimensions or less than the microdisplay area.
4. The microdisplay and electronics are four side tileable with minimal deadspace between tiles.
5. The microdisplay and electronics are two side tileable with minimal deadspace between tiles.
6. The microdisplay and electronics are three side tileable with minimal deadspace between tiles.
7. An active layer within the mesa and configured, on application of an electrical current, to generate light for emission through a light emitting surface of the substrate opposite the mesa.
8. The substrate of the monolithic ILED block serves as the glass screen of the microdisplay.
9. The control electronics are mounted directly to the monolithic ILED Microdisplay.
10. The microdisplay is four side tileable with minimal deadspace between tiles.
11. The microdisplay is two side tileable with minimal deadspace between tiles. The microdisplay is three side tileable with minimal deadspace between tiles.
12. The tiling of the microdisplay preserves the pitch of the ILED to create an infinite display.
13. The monolithic ILED block is a BGA or similar package for direct mounting to a electronics controlling substrate.
14. The ILED screen or sapphire substrate is postprocessed for light control and manipulation.
15. The ILED screen or sapphire substrate is postprocessed for ILED wavelegnth emission.
CLAIMS:

1. A display comprising a plurality of microdisplay tiles, each microdisplay tile comprising a plurality of emitters, each emitter comprising at least one LED.

2. The display according to claim 1, wherein each LED is selected from any of an OLED and an ILED.

3. The display according to claim 1 or 2, further comprising control electronics mounted to an underside of each tile.

4. The display according to claim 3, wherein the control electronics have a surface area no greater than the tile.

5. The display according to claim 3 or 4, further comprising a ball grid array mounted to the control electronics.

6. The display according to any one of claims 1 to 5, wherein each microdisplay tile is two-sided and configured to be disposed to adjacent microdisplay tiles on each side.

7. The display according to any one of claims 1 to 5, wherein each microdisplay tile is three-sided and configured to be disposed to adjacent microdisplay tiles on each side.

8. The display according to any one of claims 1 to 5, wherein each microdisplay tile is four-sided and configured to be disposed to adjacent microdisplay tiles on two side.

9. The display according to any one of the preceding claims, wherein each microdisplay tile comprises a connector arranged to connect the microdisplay tile to an adjacent microdisplay tile.
10. The display according to any one of the preceding claims, wherein each microdisplay tile is formed on a substrate, the substrate forming a screen of the microdisplay.

11. The display according to claim 10, wherein the screen is configured to manipulate emitted light.

12. The display according to claim 10 or 12, wherein the screen comprising quantum dots configured to post-process emitted light.

13. The display according to any one of the preceding claims, wherein a pitch of the emitters is maintained across adjacent microdisplay tiles.

14. A microdisplay tile comprising a plurality of emitters, each emitter comprising at least one LED, the microdisplay tile further comprising means to connect to the microdisplay tile to at least one adjacent microdisplay tile.

15. The microdisplay tile according to claim 14, wherein each LED is selected from any of an OLED and an ILED.

16. The microdisplay tile according to claim 14 or 15, further comprising control electronics mounted to an underside of each tile.

17. The microdisplay tile according to claim 16, wherein the control electronics have a surface area no greater than the tile.

18. The microdisplay tile according to claim 16 or 17, further comprising a ball grid array mounted to the control electronics.

19. The microdisplay tile according to any one of claims 14 to 18, wherein the microdisplay tile is four-sided and configured to be disposed to adjacent microdisplay tiles on each side.
20. The microdisplay tile according to any one of claims 14 to 18, wherein the microdisplay tile is three-sided and configured to be disposed to adjacent microdisplay tiles on each side.

21. The microdisplay tile according to any one of claims 14 to 18, wherein the microdisplay tile is four-sided and configured to be disposed to adjacent microdisplay tiles on two side.

22. The microdisplay tile according to any one of claims 14 to 21, wherein each microdisplay tile is formed on a substrate, the substrate forming a screen of the microdisplay.

23. The microdisplay tile according to claim 22, wherein the screen is configured to manipulate emitted light.

24. The microdisplay tile according to claim 22 or 23, wherein the screen comprising quantum dots configured to post-process emitted light.

25. A method of manufacturing a display, the method comprising connecting an array of a plurality of microdisplay tiles, each microdisplay tile comprising a plurality of emitters, each emitter comprising at least one LED.

26. The method according to claim 25, further comprising manufacturing each microdisplay tile using monolithic fabrication.

27. The method according to claim 25, further comprising manufacturing each microdisplay tile using hybrid assembly.

28. The method according to claim 25, 26 or 27, further comprising growing each of the plurality of emitters epitaxially on a common substrate.

29. The method according to any one of claims 25 to 28, further comprising providing a mesa at each emitter of the plurality of emitters.
30. The method according to claim 29, further comprising providing an active layer within each mesa.
Application No: GB1418769.4  
Examiner: Helen Edwards  
Claims searched: All  
Date of search: 17 April 2015

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

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<td>US7091927 B1 (ROCKWELL COLLINS INC) See figure 5 and paragraphs 0054-0059</td>
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<td>X</td>
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<td>WO02/47310 A2 (SARNOFF CORP) See figures and page 5 lines 18-24, page 6, page 19 lines 12-18, page 20 lines 22-31</td>
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<td>GB2240686 A (HILLEN) See figure 6 and pages 14-15</td>
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| A | Document indicating technological background and/or state of the art. |
| P | Document published on or after the declared priority date but before the filing date of this invention. |
| E | Patent document published on or after, but with priority date earlier than, the filing date of this application. |

Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC:

Worldwide search of patent documents classified in the following areas of the IPC

G09G

The following online and other databases have been used in the preparation of this search report

WPI, EPODOC
### International Classification:

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