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(54) ATOMIC LAYER DEPOSITION OF CAPACITOR DIELECTRIC

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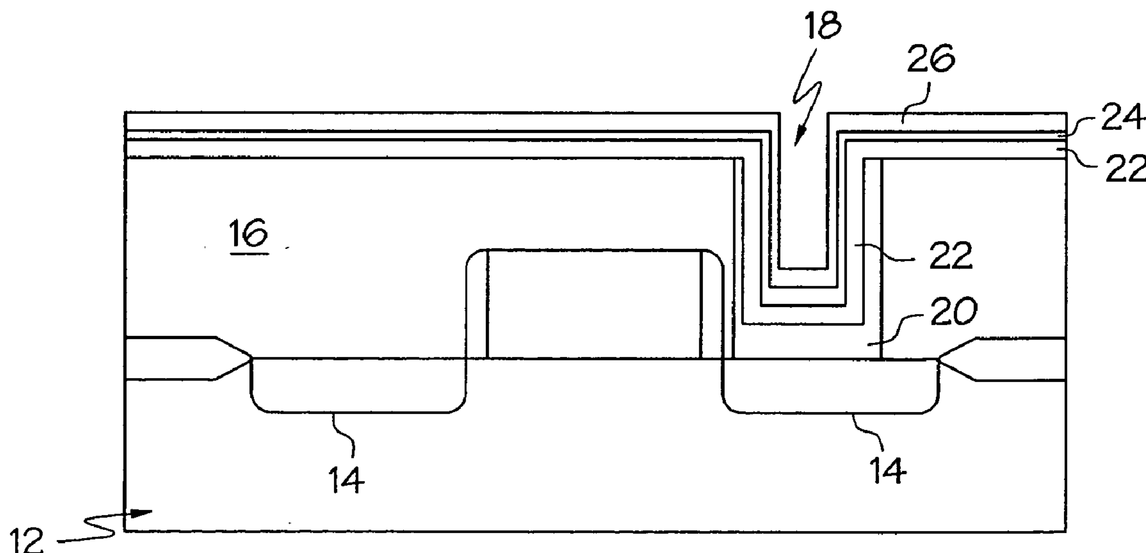
(57) **ABSTRACT**

A capacitor structure is formed over a semiconductor substrate by atomic layer deposition to achieve uniform thickness in memory cell dielectric layers, particularly where the dielectric layer is formed in a container-type capacitor structure. In accordance with several embodiments of the present invention, a process for forming a capacitor structure over a semiconductor substrate is provided. Other embodiments of the present invention relate to processes for forming memory cell capacitor structures, memory cells, and memory cell arrays. Capacitor structures, memory cells, and memory cell arrays are also provided.



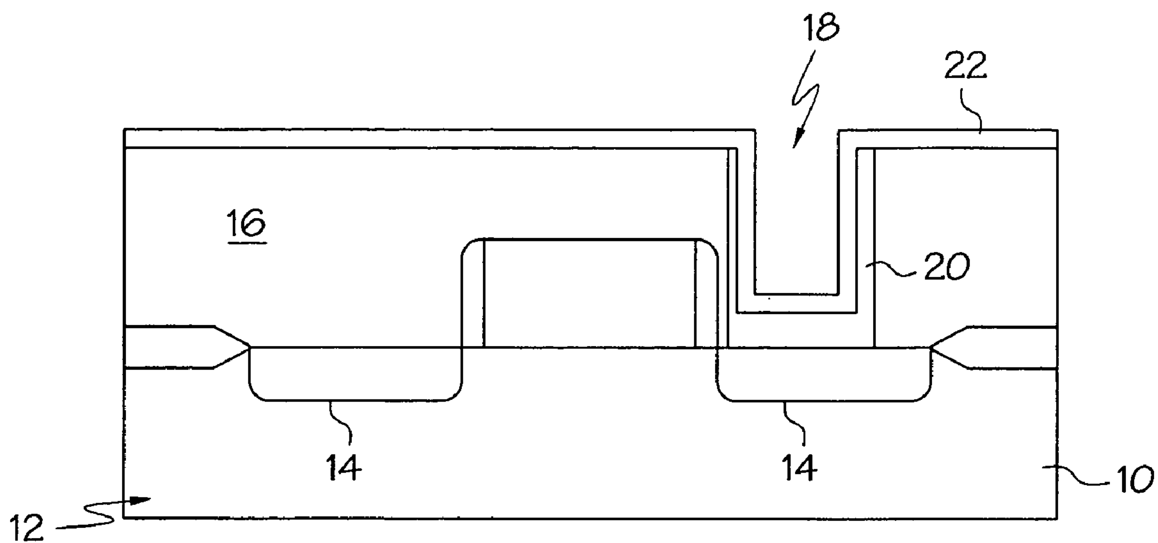


FIG. 1

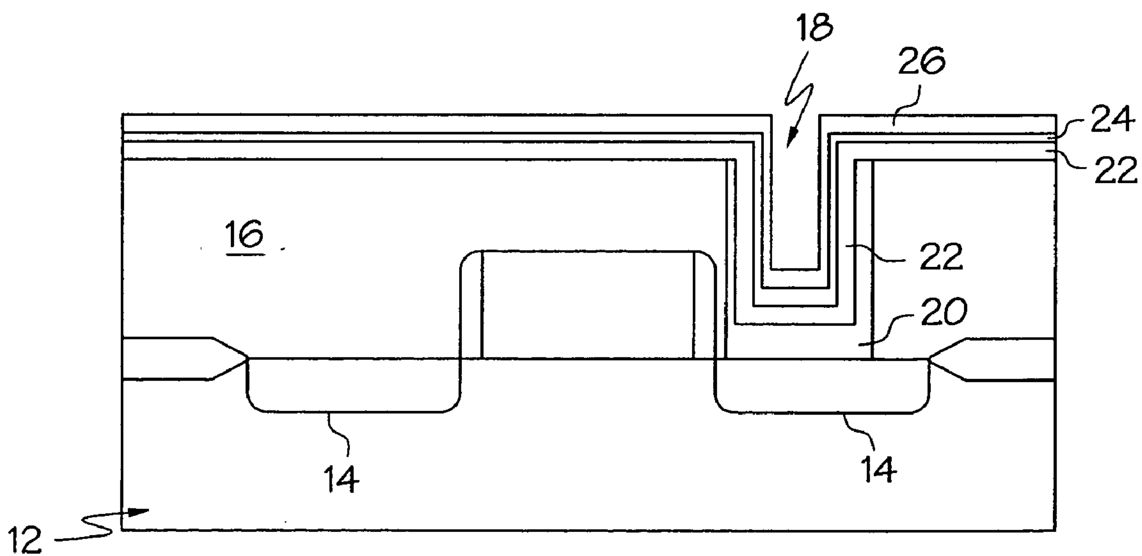


FIG. 2

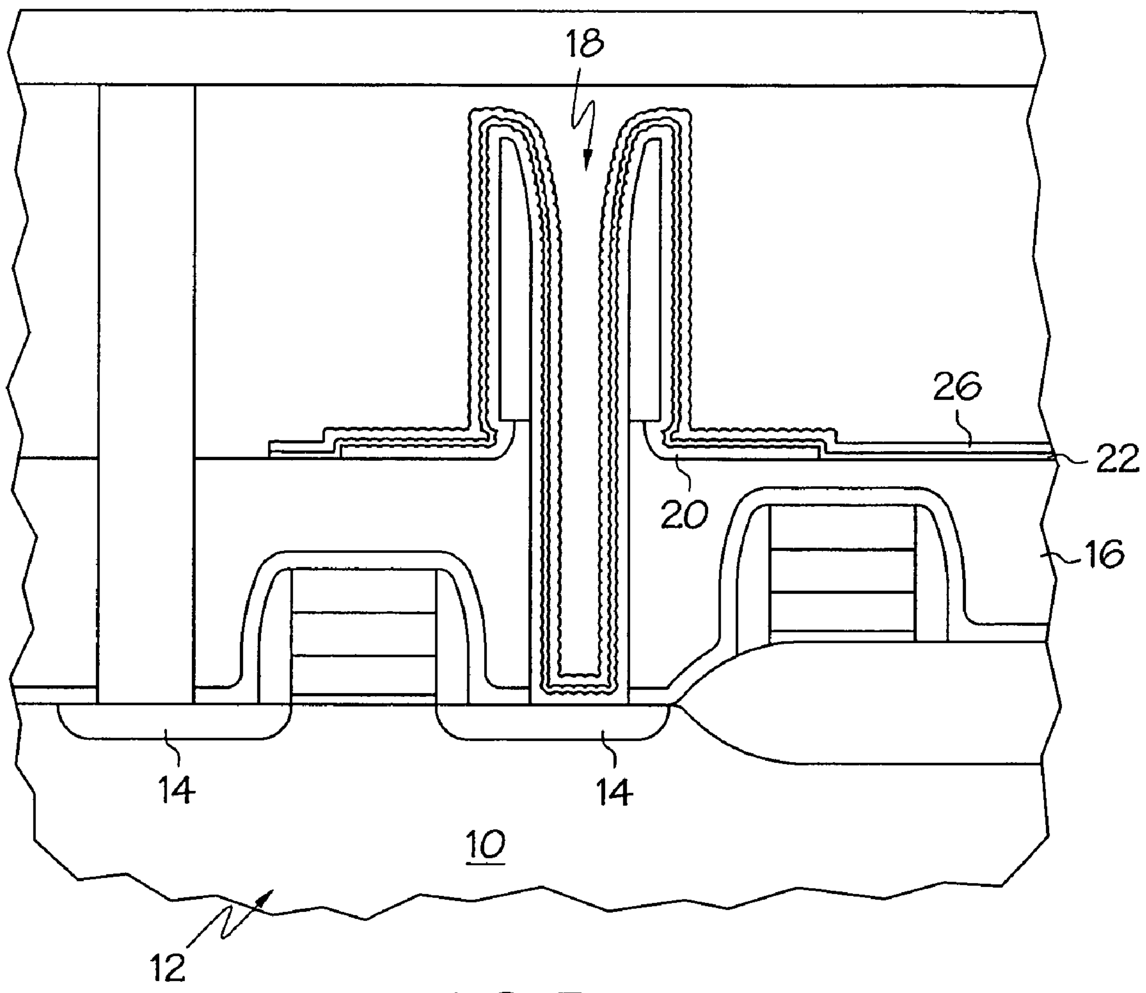


FIG. 3

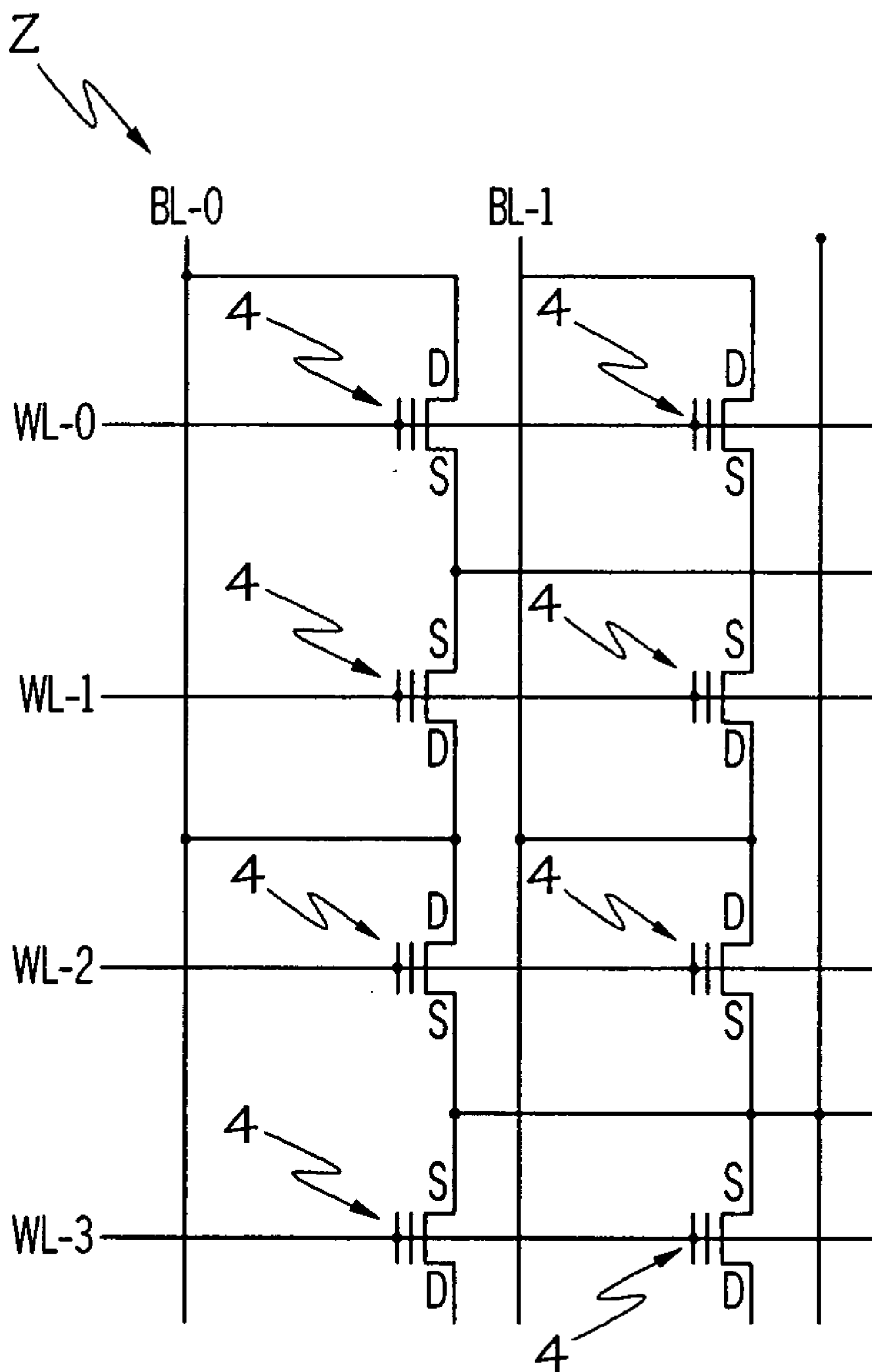


FIG. 4

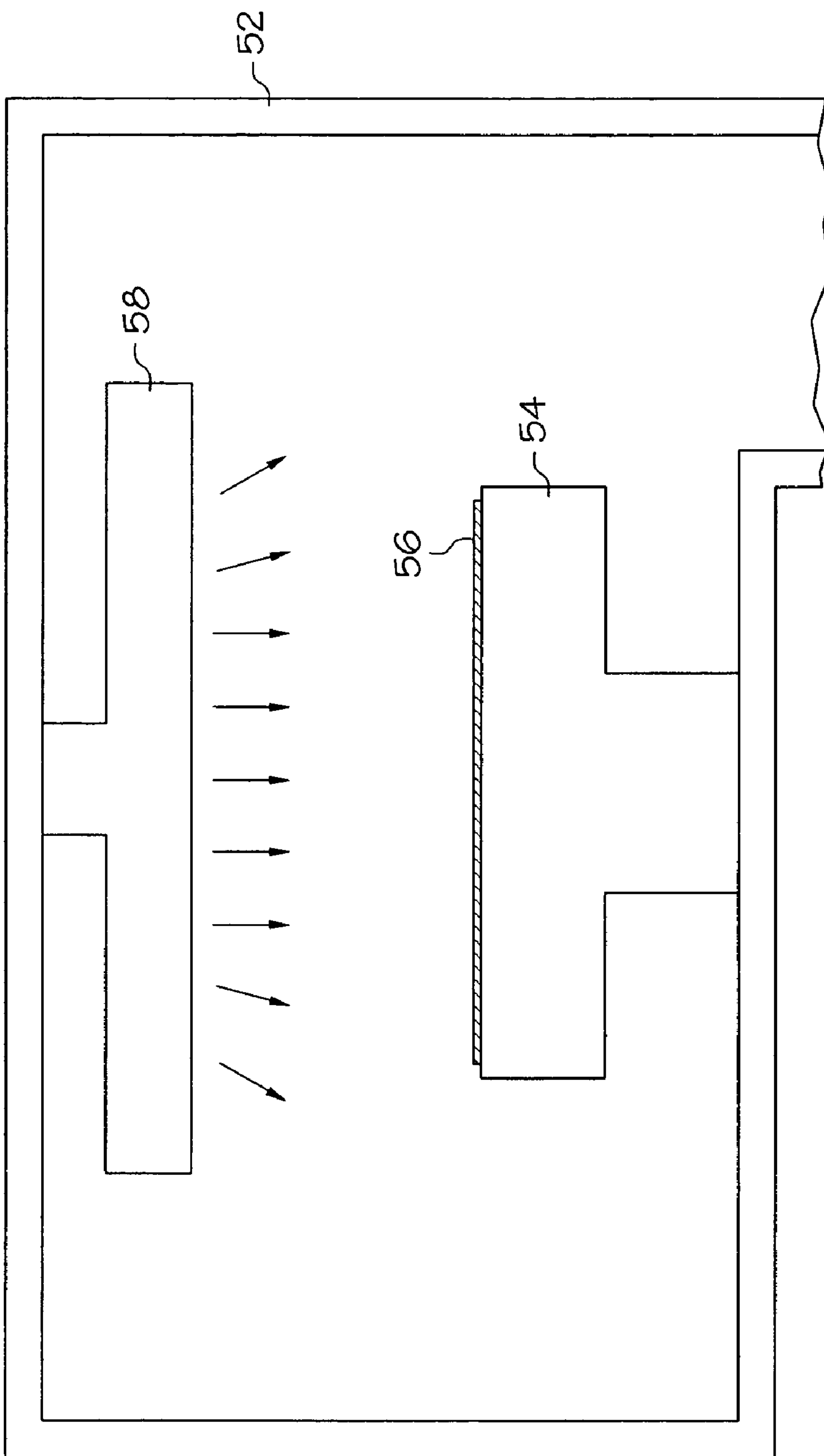


FIG. 5

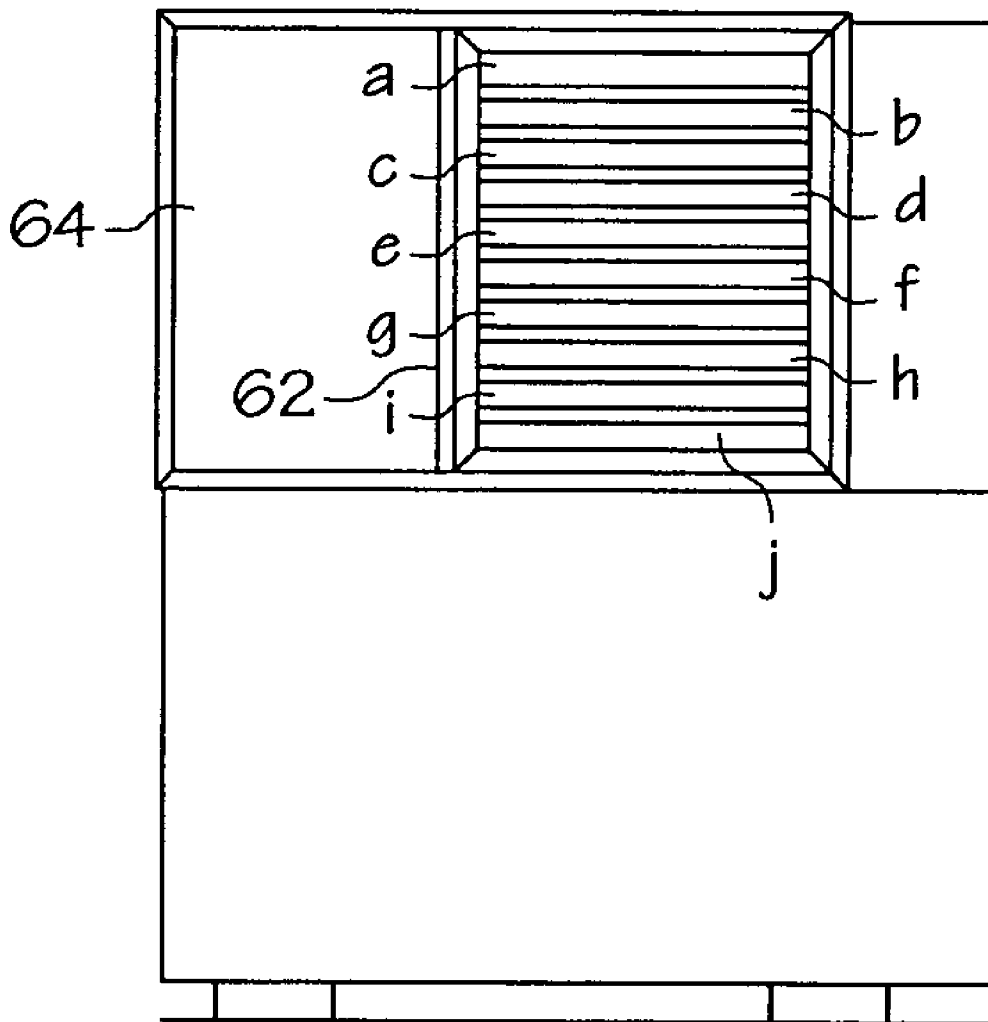


FIG. 6

ATOMIC LAYER DEPOSITION OF CAPACITOR DIELECTRIC

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. patent application Ser. No. 10/228,911 (MIO 0082 VA), which is divisional of U.S. patent application Ser. No. 09/994,547 (MIO 0082 PA), filed Nov. 27, 2001, now U.S. Pat. No. 6,551,893. This application is also related to U.S. patent application Ser. No. 10/228,911 (MIO 0082 NA), filed Aug. 27, 2002, which is a continuation of U.S. patent application Ser. No. 09/994,547 (MIO 0082 PA), filed Nov. 27, 2001, now U.S. Pat. No. 6,551,893.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to memory cell capacitor structures and, more particularly, to a fabrication process where a capacitor dielectric is formed by atomic layer deposition.

[0003] Silicon nitride is commonly employed as the dielectric in memory cell capacitor structures. Unfortunately, conventional process technology is limited in its ability to manufacture suitable reduced-thickness dielectric layers with good uniformity. Accordingly, there is a need for an improved memory cell capacitor dielectric layer manufacturing process.

BRIEF SUMMARY OF THE INVENTION

[0004] This need is met by the present invention wherein a capacitor dielectric is formed by atomic layer deposition. The present inventors have recognized that it is difficult to achieve uniform thickness in memory cell dielectric layers, particularly where the dielectric layer is formed in a container-type capacitor structure. The present invention is also applicable to trench-type capacitor structures. Generally, as device size shrinks, thinner dielectric layers are needed to ensure adequate memory cell capacitance. As dielectric layer thickness decreases, non-uniformity leads to reoxidation punch-through and corresponding device degradation. Also, as the dielectric layer thickness decreases, the leakage current attributable to the dielectric layer tends to increase dramatically, deteriorating device performance.

[0005] The present invention addresses these problems by providing a manufacturing process where the dielectric layer is formed through atomic layer deposition (ALD). In accordance with several embodiments of the present invention, a process for forming a capacitor structure over a semiconductor substrate is provided. Other embodiments of the present invention relate to processes for forming memory cell capacitor structures, memory cells, and memory cell arrays. Capacitor structures, memory cells, and memory cell arrays are also provided. Accordingly, it is an object of the present invention to provide an improved memory cell capacitor dielectric layer manufacturing process. Other objects of the present invention will be apparent in light of the description of the invention embodied herein.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0006] The following detailed description of the preferred embodiments of the present invention can be best understood when read in conjunction with the following drawings, where like structure is indicated with like reference numerals and in which:

[0007] **FIGS. 1 and 2** illustrate a memory cell capacitor structure fabrication scheme according to one embodiment of the present invention;

[0008] **FIG. 3** illustrates a memory cell capacitor structure fabrication scheme according to an alternative embodiment of the present invention;

[0009] **FIG. 4** illustrates a memory cell array;

[0010] **FIG. 5** is a schematic diagram of an ALD apparatus according to the present invention; and

[0011] **FIG. 6** is an elevation view of an ALD apparatus for a large-scale production system according to present invention.

DETAILED DESCRIPTION

[0012] Referring to **FIGS. 1 and 2**, according to one embodiment of the present invention, a capacitor structure of a memory cell may be formed by providing a semiconductor substrate **10** including a semiconductor structure defining a transistor **12** and a pair of transistor node locations **14**. An insulating layer **16**, e.g. a BPSG layer, is formed over the semiconductor substrate **10**. A container **18** is formed in the insulating layer **16** over one of the transistor node locations **14**. A lower electrode layer **20**, typically a HSG polysilicon layer, is formed along an inner surface of the container **18**. A dielectric layer **22** is formed on the lower electrode layer **20** and over a portion of an upper surface of the insulating layer **16**. A reoxidized layer **24** is formed over the dielectric layer **22** by subjecting the dielectric layer **22** to a reoxidation process. Finally, an upper electrode layer **26**, typically a polysilicon layer, is formed over the reoxidized layer **24**, typically covering the entire dielectric layer **22**.

[0013] The lower electrode layer **20** typically covers the entire inner surface of the container **18**. The dielectric layer **22**, which is typically formed directly on the lower electrode layer **20**, completely covering the lower electrode layer **20**, exhibits uniform thickness across the lower electrode layer **20** and the upper surface of the insulating layer **16**. The dielectric layer **22** is formed such that the uniform thickness is sufficient to prevent punch-thru oxidation, i.e., incidental oxidation of the lower electrode layer **20** during reoxidation of the dielectric layer and other device components. As will be appreciated by those practicing the present invention and familiar with semiconductor device fabrication, a reoxidation step is commonly incorporated in semiconductor device fabrication schemes.

[0014] The dielectric layer **22** is formed through an atomic layer deposition (ALD) process. The thickness of a silicon nitride dielectric layer is typically 50 angstroms or less. Conventional process technology, such as low pressure chemical vapor deposition (LPCVD) is not well-suited for fabrication of silicon nitride dielectric layers of such thicknesses because dielectric quality deterioration and oxidation punch-through become problems at layer thicknesses of 50 angstroms or less. Oxidation punch-through of LPCVD silicon nitride dielectric layers occurs because the silicon nitride on the underlying BPSG insulating layer is thinner than that on the HSG lower electrode. The difference in

thickness is attributable to the difference in LPCVD nucleation incubation times for silicon nitride over BPSG and HSG, respectively. Specifically, the nucleation incubation time is longer for silicon nitride on BPSG than for silicon nitride on HSG. Data has also shown that the quality of the silicon nitride layer formed according to the present invention is superior to that of the silicon nitride layer formed by the LPCVD method. Therefore, according to the present invention, capacitor performance is maintained even as the dielectric thickness goes below 50 angstroms.

[**0015**] According to the deposition process of the present invention, a first precursor, e.g., a silicon-containing precursor, is chemisorbed over a surface of the lower electrode layer **20** and the upper surface of the insulating layer **16**. A second precursor, e.g., a nitrogen-containing precursor, is then reacted with the chemisorbed precursor to form the dielectric layer **22**, e.g., a silicon nitride dielectric layer. The specific processing steps utilized to introduce the first and second precursors and cause their chemisorption/reaction are beyond the scope of the present invention and may be gleaned from any one of a number of teachings related to atomic layer deposition. For the purposes of describing and defining the present invention, it is noted that the precise mechanism by which the molecules of the first precursor adhere to the surface of the semiconductor substrate is not the subject of the present invention. The mechanism is merely described herein as chemisorption—a term intended to cover absorption, adsorption, and any other similar mechanisms by which the precursor may form a monolayer upon the surface of the semiconductor substrate **10**.

[**0016**] Generally, in atomic layer deposition, assuming that two precursor gases A and B are used, precursor gas A is introduced into a reaction chamber of an ALD device and atoms of the precursor gas A are chemisorbed on a substrate in the chamber. Next, unabsorbed precursor gas A is purged with an inert gas such as Ar or nitrogen N_2 and precursor gas B flows into the chamber. A chemical reaction between the precursor gases A and B occurs only on the surface of the substrate on which the precursor gas A has been adsorbed, resulting in formation of an atomic layer on the substrate. Unreacted precursor gas B and the by-products of the reaction between two gases A and B are purged. The thickness of the film can be increased by repeating these steps to deposit successive atomic layers. In this manner, the thickness of the thin film can be adjusted in atomic layer units according to the number of repetitions. Atomic layer deposition processes according to the present invention are typically characterized by semiconductor substrate temperatures of between about 350° C. to about 700° C. and reactor chamber pressures of about 1 Torr to about 120 Torr. A substantially flat temperature distribution can be maintained across the semiconductor substrate as the first precursor is chemisorbed and the second precursor is reacted with the chemisorbed precursor.

[**0017**] The ALD method, when used for depositing a thin film on a substrate, can ensure near perfect step coverage regardless of the morphology of the substrate. The composition of the atomic layer depends upon the nature of the reaction between the precursor gases A and B. In the present invention, where the object is to form a silicon nitride film in a capacitor structure, the first precursor gas typically comprises a silicon-containing gas and the second precursor gas typically comprises a nitrogen-containing gas. Suitable silicon-containing precursors include, but are not limited to, $SiCl_4$, $SiHCl_3$, SiH_2Cl2, Si_2H_6, $SiCl_6$, and SiH_4. Suitable nitrogen-containing precursors include, but are not limited to, NH_3 and N_2H_2.

[**0018**] In some cases, for example where N_2H_2 is utilized as the precursor, it may be helpful to generate a plasma in the reaction chamber to help break-up the precursor, generating nitrogen radicals encouraging reaction of the two precursors at the surface of the substrate on which the layer is to be formed. Alternatively, a laser source or an infrared radiation source may be employed to help generate nitrogen radicals. Use of the plasma, the laser source, or the infrared radiation source also allows the process to operate at reduced chamber and substrate temperatures.

[**0019**] **FIG. 5** is a schematic diagram of a single wafer process ALD apparatus **50** according to the present invention. As shown in **FIG. 5**, the ALD apparatus comprises a vacuum chamber **52** and a heater **54** for heating a substrate **56** placed in the vacuum chamber **52** to an appropriate temperature. The substrate **56** is seated on a substrate holder (not shown) placed on top of the heater **54**, and heated evenly by the heater **54**. Also, a showerhead **58** through which a predetermined precursor gas flows into the vacuum chamber **52**, is installed facing the surface of the substrate **56**.

[**0020**] The present invention can be utilized in any standard hot wall batch-type ALD furnace. Batch type furnaces enable processing of multiple wafers in a single batch process, increasing manufacturing throughput. **FIG. 6** is an elevation view of an batch-type ALD apparatus **60** for a large-scale production system according to present invention. In this embodiment, preprocessed substrates a-j are loaded onto a cassette or stacking mechanism **62** in a reaction chamber **64** of the ALD apparatus **60** through a cassette load lock (not shown). Alternatively, an entire cassette of substrates may be introduced into the chamber **64**. Specific structure for accomplishing this sort of loading and interfacing is well-known in the art of production systems. Once loaded the substrates a-j are subject to processing according to the present invention and removed from the chamber **64**. In this manner, respective capacitor structures according to the present invention may be formed over a plurality of semiconductor substrates. Similarly, the present invention relates to fabrication of a memory cell and, on a larger scale, to fabrication to an array of memory cells on a semiconductor die and to respective arrays of memory cells on a plurality of semiconductor die.

[**0021**] Although the present invention has been illustrated with reference to the specific memory cell structure of **FIGS. 1 and 2**, it is contemplated that the present invention is applicable to a variety of memory cell arrangements. For example, **FIG. 3**, where like structure is indicated with like reference numerals, illustrates the process of the present invention as applied to an alternative memory cell structure.

[**0022**] **FIG. 4** illustrates a memory cell array **2**. The memory cell array **2** includes a plurality of memory cells **4**. Each memory cell **4** includes a capacitor structure and a transistor structure, as discussed above with reference to FIGS. **1-3**. Conventional source regions S, drain regions D, bit lines BL, and word lines WL are also illustrated in **FIG. 4**. It is noted that although the present invention is illustrated with reference to the structures of FIGS. **1-4**, the present

invention is applicable to a variety of types of memory cell structures and memory array arrangements.

[0023] For the purposes of describing and defining the present invention, it is noted that a "semiconductor substrate" denotes any construction comprising a semiconductor material. Examples of semiconductor substrates include semiconductor wafers or other bulk semiconductor materials (either alone or in assemblies comprising other materials), and semiconductor material layers (either alone or in assemblies comprising other materials).

[0024] It should be further noted that, for the purposes of defining and describing the present invention, "on" a substrate or layer denotes formation in contact with the surface of the substrate or layer and "over" a substrate or layer denotes formation above or in contact with the surface of the substrate or layer. For the purposes of describing and defining the present invention, it is noted that a layer formed "in" a region or other layer may be formed at a surface of the region/layer or within the region/layer between its upper and lower surfaces. A layer formed "at" a surface of a region/layer may be formed directly on the surface or may be partially embedded in the region/layer so as to define a portion of the surface of the region/layer.

[0025] Having described the invention in detail and by reference to preferred embodiments thereof, it will be apparent that modifications and variations are possible without departing from the scope of the invention defined in the appended claims. More specifically, although some aspects of the present invention are identified herein as preferred or particularly advantageous, it is contemplated that the present invention is not necessarily limited to these preferred aspects of the invention.

What is claimed is:

1. A process for forming a capacitor structure comprising:

forming a BPSG insulating layer over a semiconductor substrate;

forming a container in said insulating layer;

forming an HSG polysilicon lower electrode layer along an inner surface of said container;

forming a silicon nitride dielectric layer characterized by a given degree of uniformity over said HSG polysilicon lower electrode layer and an upper surface of said BPSG insulating layer through an atomic layer deposition process where a silicon-containing precursor is chemisorbed over a surface of said HSG lower electrode layer and a nitrogen-containing precursor is reacted with said chemisorbed silicon-containing precursor to form said silicon nitride dielectric layer such that

said given degree of uniformity exceeds a degree of uniformity attributable to LPCVD nucleation incubation of silicon nitride over HSG polysilicon and BPSG, and

said thickness of said silicon nitride dielectric layer is sufficient to prevent oxidation punch-through from a reoxidized layer formed over said dielectric layer to said HSG polysilicon lower electrode layer; and

forming an upper electrode layer over said reoxidized layer.

2. A process for forming a capacitor structure as claimed in claim 1 wherein said lower electrode layer is formed so as to extend beyond said inner surface of said container.

3. A process for forming a capacitor structure as claimed in claim 1 wherein said lower electrode layer is formed so as to extend along an upper surface of said insulating layer.

4. A process for forming a capacitor structure as claimed in claim 1 wherein said lower electrode layer is formed so as to extend from said inner surface in the direction of an upper surface of said insulating layer along an extension of said container.

5. A process for forming a capacitor structure as claimed in claim 1 wherein said lower electrode layer is formed so as to extend along an upper surface of said insulating layer and from said inner surface in the direction of said upper surface of said insulating layer along an extension of said container.

6. A process for forming a capacitor structure as claimed in claim 1 wherein said dielectric layer is formed on said lower electrode layer.

7. A process for forming a capacitor structure comprising:

forming a BPSG insulating layer over a semiconductor substrate;

forming a container in said insulating layer;

forming an HSG polysilicon lower electrode layer along an inner surface of said container;

forming a silicon nitride dielectric layer less than about 50 angstroms in thickness and characterized by a given degree of uiformity over said HSG polysilicon lower electrode layer and an upper surface of said BPSG insulating layer through an atomic layer deposition process where a silicon-containing precursor is chemisorbed over a surface of said HSG lower electrode layer and a nitrogen-containing precursor is reacted with said chemisorbed silicon-containing precursor to form said silicon nitride dielectric layer such that

said given degree of uniformity exceeds a degree of uniformity attributable to LPCVD nucleation incubation of less than 50 angstrom thick silicon nitride over HSG polysilicon and BPSG, and

said thickness of said silicon nitride dielectric layer is sufficient to prevent oxidation punch-through from a reoxidized layer formed over said dielectric layer to said HSG polysilicon lower electrode layer; and

forming an upper electrode layer over said reoxidized layer.

8. A process for forming a capacitor structure comprising:

forming an insulating layer over a semiconductor substrate;

forming a container in said insulating layer;

forming a lower electrode layer along an inner surface of said container;

forming a dielectric layer characterized by a given degree of uiformity over said lower electrode layer and an upper surface of said insulating layer through an atomic layer deposition process where a silicon-containing precursor is chemisorbed over a surface of said lower electrode layer and a nitrogen-containing precursor is

reacted with said chemisorbed silicon-containing precursor to form said dielectric layer such that

said given degree of uniformity exceeds a degree of uniformity attributable to LPCVD nucleation incubation of a dielectric layer over an electrode layer and an insulating layer, and

said thickness of said dielectric layer is sufficient to prevent oxidation punch-through from a reoxidized layer formed over said dielectric layer to said lower electrode layer; and

forming an upper electrode layer over said reoxidized layer.

9. A process for forming a memory cell comprising:

forming a semiconductor structure defining a transistor and a pair of transistor node locations in a semiconductor substrate;

forming a BPSG insulating layer over said semiconductor substrate;

forming a container in said insulating layer over one of said transistor node locations;

forming an HSG polysilicon lower electrode layer along an inner surface of said container;

forming a silicon nitride dielectric layer characterized by a given degree of uniformity over said HSG polysilicon lower electrode layer and an upper surface of said BPSG insulating layer through an atomic layer deposition process where a silicon-containing precursor is chemisorbed over a surface of said HSG lower electrode layer and a nitrogen-containing precursor is reacted with said chemisorbed silicon-containing precursor to form said silicon nitride dielectric layer such that

said given degree of uniformity exceeds a degree of uniformity attributable to LPCVD nucleation incubation of silicon nitride over HSG polysilicon and BPSG, and

said thickness of said silicon nitride dielectric layer is sufficient to prevent oxidation punch-through from a reoxidized layer formed over said dielectric layer to said HSG polysilicon lower electrode layer; and

forming an upper electrode layer over said reoxidized layer.

10. A process for forming a memory cell comprising:

forming a semiconductor structure defining a transistor and a pair of transistor node locations in a semiconductor substrate;

forming a BPSG insulating layer over said semiconductor substrate;

forming a container in said insulating layer over one of said transistor node locations;

forming an HSG polysilicon lower electrode layer along an inner surface of said container;

forming a silicon nitride dielectric layer less than about 50 angstroms in thickness and characterized by a given degree of uiformity over said HSG polysilicon lower electrode layer and an upper surface of said BPSG insulating layer through an atomic layer deposition process where a silicon-containing precursor is chemisorbed over a surface of said HSG lower electrode layer and a nitrogen-containing precursor is reacted with said chemisorbed silicon-containing precursor to form said silicon nitride dielectric layer such that

said given degree of uniformity exceeds a degree of uniformity attributable to LPCVD nucleation incubation of less than 50 angstrom thick silicon nitride over HSG polysilicon and BPSG, and

said thickness of said silicon nitride dielectric layer is sufficient to prevent oxidation punch-through from a reoxidized layer formed over said dielectric layer to said HSG polysilicon lower electrode layer; and

forming an upper electrode layer over said reoxidized layer.

11. A process for forming a memory cell comprising:

forming a semiconductor structure defining a transistor and a pair of transistor node locations in a semiconductor substrate;

forming an insulating layer over said semiconductor substrate;

forming a container in said insulating layer over one of said transistor node locations;

forming a lower electrode layer along an inner surface of said container;

forming a dielectric layer characterized by a given degree of uiformity over said lower electrode layer and an upper surface of said insulating layer through an atomic layer deposition process where a silicon-containing precursor is chemisorbed over a surface of said lower electrode layer and a nitrogen-containing precursor is reacted with said chemisorbed silicon-containing precursor to form said dielectric layer such that

said given degree of uniformity exceeds a degree of uniformity attributable to LPCVD nucleation incubation of a dielectric layer over an electrode layer and an insulating layer, and

said thickness of said dielectric layer is sufficient to prevent oxidation punch-through from a reoxidized layer formed over said dielectric layer to said lower electrode layer; and

forming an upper electrode layer over said reoxidized layer.

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