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WO-A-83/04354
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US-A- 4 429 416

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, vol. NS-29, no. 1, February 1982, pages 160-163, IEEE, New York, US; A. GLASMACHERS et al.: "Electronic system for an impact mass spectrometer with high dynamic range for the giotto probe"

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PATENT ABSTRACTS OF JAPAN, vol. 9, no. 201 (E-336)[1924], 17th August 1985; & JP-A-60 66 511 (NIPPON DENKI K.K.) 16-04-1985

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IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-16, no. 6, December 1981, pages 626-633, IEEE, New York, US; R.A. BLAUSCHILD: "An open loop programmable amplifier with extended frequency range"

Description

Background of the Invention:

This invention relates to an intermediate frequency amplification circuit for use in a mobile radio station (unit), a cordless telephone set, and/or a telemeter system, and, more particularly, to an intermediate frequency amplification circuit which is capable of measuring or detecting a field strength.

A conventional intermediate frequency amplification circuit of the type described comprises an amplification part which is supplied with a circuit input signal to produce a circuit output signal subjected to amplification therein. In addition, a signal strength measuring part is included in the intermediate frequency amplification circuit to measure or detect a field strength of the circuit input signal.

More particularly, the amplification part of such an amplification circuit comprises a plurality of differential stages connected in cascade to one another. Each of the differential stages comprises a first pair of transistors having emitters coupled in common to each other. On the other hand, the signal strength measuring part measures the field strength by detecting a d.c. level of the circuit input signal. For this purpose, the signal strength measuring part comprises a plurality of rectification circuits for rectifying output signals of the differential stages to produce rectified signals, respectively, and capacitors coupled to the respective rectification circuits so as to add the rectified signals to one another. Each of the rectification circuits is implemented by a plurality of transistors to carry out half-wave rectification.

With this structure, each capacitance of the capacitors in the rectification circuits inevitably become large with a reduction of an intermediate frequency necessary in the intermediate frequency amplification circuit. On manufacturing such an intermediate frequency amplification circuit by the use of a semiconductor integration technique, necessity of a large capacitance gives rise to an increase of a chip size. In order to reduce a chip size, it might be considered that the respective capacitors are connected as external capacitors outside of a chip. However, use of the external capacitors results in an increase of terminals derived from the chip and makes it difficult to apply an integration technique to such an amplification circuit. At any rate, the above-mentioned amplification circuit requires the capacitors equal in number to the rectification circuits.

Moreover, each rectification circuit has a bad temperature characteristic. In order to improve the temperature characteristic, complicated compensation must be carried out in each rectification circuit.

In Unexamined Japanese Patent Publication Syo 60-246108, an intermediate frequency amplification circuit is disclosed which comprises first through last full-wave rectification circuits connected in cascade to one another. Each of the full-wave rectification circuits comprises first and second differential amplifiers and third and fourth differential amplifiers connected to the first and the second differential amplifiers in series across a power source, respectively. Each of rectified output signals is sent through a current mirror circuit to a current summation circuit to produce a field strength signal. The current summation circuit may include a single capacitor.

Incidentally, the first differential amplifier of each full-wave rectification circuit serves to supply an amplified signal to a next following one of the full-wave rectification circuits. As a result, a circuit input signal is supplied to the first full-wave rectification circuits and subjected to amplification through each of the full-wave rectification circuits to produce a circuit output signal through the last full-wave rectification circuit.

With this structure, it is possible to improve a temperature characteristic and to produce the field strength signal by the use of a single capacitor.

However, the intermediate frequency amplification circuit is disadvantageous in that a source voltage must comparatively be high because the first and the second differential amplifiers must be connected to the third and the fourth differential amplifiers in series across the power source. In fact, it is difficult to drive the amplification circuit at a voltage lower than 2 volts or so. This shows that power consumption becomes large in the intermediate frequency amplification circuit.

An intermediate frequency amplification circuit which is substantially constructed as described above and which has all features of the preamble of claim 1 is disclosed in US-A-4 429 416.

In IEEE Transactions on Nuclear Science, Vol. NS-29 (1982), February, No. 1, pages 160-163, a logarithmic amplifier is disclosed which comprises a six-stage differential amplifier circuit, a rectifier block and an adder wherein the rectifier block comprises a balanced emitter coupled pair of transistors. In this logarithmic amplifier, the base regions of primary differential circuits are connected to amplifier input terminals of a cascade of amplifiers whereby the collector regions of said primary differential circuits are connected to the logarithmic amplifier output where a summation takes place.

It is an object of the invention to provide an intermediate frequency amplification circuit which can readily be manufactured by use of a semiconductor integration technique even when the intermediate frequency is low.

It is another object of the invention to provide an intermediate frequency amplification circuit of the type described which is stable in temperature characteristic.

It is still another object of this invention to provide an intermediate frequency amplification circuit of the type described which can reduce the power consumption in the circuit.

These objects are achieved by an intermediate frequency amplification circuit as defined in claim 1; the dependent claims are related to further developments of the invention.

An intermediate frequency amplification circuit to which this invention is applicable is operable in response to a circuit input signal to produce a circuit output signal subjected to amplification. The intermediate frequency amplification circuit comprises first through n-th differential amplifiers which have first through n-th amplifier input terminal pairs and first through n-th amplifier output terminal pairs, respectively, and which are connected in cascade from the first to the n-th differential amplifiers by successively connecting the amplifier output terminal pair of each differential amplifier to the amplifier input terminal pair of the next following differential amplifier. The circuit input signal is supplied across the first amplifier input terminal pair while the circuit output signal is produced at the n-th amplifier output terminal pair. The intermediate frequency amplification circuit further comprises a measuring circuit responsive to the circuit input signal for measuring a field strength to produce a field strength signal representative of the field strength.

According to this invention, the measuring circuit comprises first through (n+1)-th differential units which have first through (n+1)-th unit input terminal pairs connected to the first through n-th amplifier input terminal pairs and to the n-th amplifier output terminal pair, respectively, and first through (n+1)-th unit output terminal pairs supplied with first through (n+1)-th unit output signals, respectively, and an adder circuit connected to the first through (n+1)-th unit output terminal pairs for adding the first through (n+1)-th unit output signals to one another to produce the field strength signal. Each of the first through (n+1)-th differential units comprises a primary differential circuit of first and second primary transistors which have first and second base regions, first and second emitter regions, and first and second collector regions, respectively. The first and the second base regions are connected to the amplifier input terminal pair, respectively, while the first and the second emitter regions have an area ratio of l:k, where k is greater than unity, and are coupled in common to each other. The first and the second collector regions are connected to the unit output terminal pair, respectively.

Brief Description of the Drawing:

Fig. 1 is a circuit diagram of an intermediate frequency amplification circuit according to a first embodiment of this invention;

Fig. 2 is a graphical representation for use in describing operation of a single unit included in the amplification circuit illustrated in Fig. 1;

Fig. 3 is another graphical representation for use in describing a combination of a plurality of the units illustrated in Fig. 1;

Fig. 4 is a circuit diagram of an intermediate frequency amplification circuit according to a modification of the first embodiment illustrated in Fig. 1;

Fig. 5 is a circuit diagram of an intermediate frequency amplification circuit according to a second embodiment of this invention;

Fig. 6 is a graphical representation for use in describing a single unit included in the amplification circuit illustrated in Fig. 5;

Fig. 7 is another graphical representation for use in describing a combination of the units included in the amplification circuit illustrated in Fig. 5;

Fig. 8 is a circuit diagram of an intermediate frequency amplification circuit according to a modification of the second embodiment illustrated in Fig. 5;

Fig. 9 is a circuit diagram of an intermediate frequency amplification circuit according to a third embodiment of this invention;

Fig. 10 is a graphical representation for use in describing operation of a single unit included in the amplification illustrated in Fig. 9;

Fig. 11 is another graphical representation for use in describing operation of a combination of the units included in the amplification circuit illustrated in Fig. 9; and

Fig. 12 is a circuit diagram of an intermediate frequency amplification circuit according to a fourth embodiment of this invention.

Description of the Preferred Embodiments:

Referring to Fig. 1, an intermediate frequency amplification circuit according to a first embodiment of this invention comprises an amplification part 21 which is operable in response to a circuit input signal V_{IN} toproduce a circuit output signal V_{OUT} subjected to amplification. The circuit input signal V_{IN} is given across a pair of circuit input terminals while the circuit output signal V_{OUT} is developed across the circuit output terminals. More particularly, the amplification part 21 comprises first through n-th stages of differential amplifiers which comprises first through n-th amplifier input terminal pairs and first through n-th amplifier output terminal pairs. The first through n-th stages of differential amplifiers may simply be called first through n-th amplifiers, respectively, and are connected in cascade to one another by successively connecting the amplifier output terminal pair of each amplifier to the amplifier input terminal pair of the next following stage of the amplifiers. In this case, the first amplifier input terminal pair is connected to the circuit input terminal pair while the n-th amplifier output terminal pair is connected to the circuit output terminal pair.

The first through n-th amplifiers are similar in structure to one another and comprise circuit elements specified by double suffixes first ones of which are indicative of stage numbers and second ones of which are indicative of element numbers. Taking this into consideration, an i-th amplifier alone will be described as a representative of the first through n-th amplifiers, where i is a natural number between unity and n, both inclusive. The i-th amplifier comprises first and second transistors Q_{i1} and Q_{i2} which have bases connected to an i-th amplifier input terminal pair, emitters connected in common to a constant current source I_{i0}, and collectors which are connected to an i-th amplifier output terminal pair. The collectors of the first and the second transistors Q_{i1} and Q_{i2} are connected through first and second resistors R_{i1} and R_{i2} in common to a first source terminal which is supplied with a source voltage V_{cc} which is supplied across a first source terminal and a second source terminal grounded. With this structure, an amplifier output signal V_i is developed across the collectors of the i-th amplifier which may be regarded as the amplifier output terminal pair, as illustrated in Fig. 1. The collectors of the first and the second transistors Q_{i1} and Q_{i2} of the i-th stage are connected to the bases of the second and the first transistors $Q_{(i+1)2}$ and $Q_{(i+1)1}$ of the (i + 1)-th stage. Such connections may be called twisted connections.

The illustrated intermediate frequency amplification circuit further comprises a measuring part 22 for measuring a field strength of a reception signal given to a receiver including the amplification circuit. Such measurement of the field strength is carried out by detecting a d.c. level of the circuit input signal V_{IN}. For this purpose, the illustrated measuring part 22 has a half-wave rectification and saturation characteristic which simulates a logarithmic characteristic.

More particularly, the measuring circuit 22 comprises first through (n + 1)-th differential units as shown downwards of Fig. 1. The first through (n + 1)-th differential units may simply be called first through (n + 1)-th units as depicted in Fig. 1, respectively. The second through (n + 1)-th units have second through (n + 1)-th unit input terminal pairs connected to the first through n-th amplifier output terminal pairs of the first through n-th amplifiers, respectively, while the first unit has a first input terminal pair connected to the first amplifier input terminal pair or to the circuit input terminal pair. In this connection, the first unit is supplied with the circuit input signal V_{IN}. The second through (n + 1)-th units are supplied with the first through n-th amplifier output signals, respectively.

The first through (n + 1)-th units further have first through (n + 1)-th unit output terminal pairs which are connected to an adder circuit 23 in parallel and which are supplied with first through (n + 1)-th unit output signals, respectively. As readily understood from Fig. 1, the first through (n + 1)-th units are similar in structure and operation to one another.

Therefore, a single one of the units alone will be described as a representative of the first through (n + 1)-th units and may be depicted at the same suffix i as the amplifiers, although i is a natural number between unity and (n + 1), both inclusive. The i-th unit comprises first and second transistors Q_{if} and Q_{is} which may be called first and second primary transistors, respectively, for convenience of description and which are specified by the second ones (f and S) of the double suffixes, respectively. The first and the second primary transistors Q_{if} and Q_{is} have first and second emitter regions, first and second base regions, and first and second collector regions when such transistors are manufactured by a semiconductor integration technique. Herein, it is to be noted that the first and the second emitter regions have a first area S_o and a second area kS_o where k is a factor greater than unity. The factor may be called an area factor. In other words, the first and the second emitter regions have different areas from each other. In this connection, the second emitter region is specified by a double line in Fig. 1.

In the i-th unit, the first and the second emitter regions are connected in common to a constant current source I_{i1}. The first and the second base regions are connected to the circuit input terminal pair and the i-th amplifier output terminal pair when the i-th unit is the first unit and either one of the second through (n + 1)-th amplifiers, respectively. More specifically, the first and the second primary transistors Q_{1f} and Q_{1s} of the first unit have the first and the second base regions connected to the bases of the first and the second transistors Q_{11} and Q_{12} of the first amplifier, respectively, while the first and the second primary transistors of each of the second through (n + 1)-th units have the first and the second base regions connected to the collectors of the second and the first transistors Q_{i2} and Q_{i1}, respectively, of the preceding amplifier stage. Thus, the base regions of the second through (n + 1)-th units are connected to the collectors of the first through n-th amplifiers in a twisted manner like the connections between two adjacent ones of the first through n-th amplifiers.

In addition, the first collector regions of the first through (n + 1)-th units are connected in common to a first adder terminal of the adder circuit 23 while the second collector regions of the first through (n + 1)-th units are connected in common to a second adder terminal of the adder circuit 23.

At any rate, first through (n + 1)-th collector currents of a first kind are caused to flow through the first collector regions of the first primary transistors Q_{if} of the first through (n + 1)-th units, respectively, and are depicted at I_{c11} through $I_{c1(n+1)}$, respectively, while first through (n + 1)-th collector currents I_{c21} to $I_{c2(n+1)}$ of a second kind are caused to flow through the second collector regions of the second primary transistors Q_{is} of the first through (n + 1)-th units, respectively. The collector currents I_{c1i} and I_{c2i} might often simply be referred to as first- and second-kind collector currents, respectively. The first collector regions of the first primary transistors Q_{if} form first ones of the unit output terminal pairs and are connected in common to a first adder input terminal of the adder circuit 23 while the second collector regions of the second primary transistors Q_{is} form second ones of the unit output terminal pairs and are connected in common to a second adder input terminal of the adder circuit 23.

The adder circuit 23 comprises a current mirror circuit composed of a first additional transistor Q_{o1} and a second additional transistor Q_{o2}. The first additional transistor Q_{o1} has a collector and an emitter connected to the first and the second adder input terminals, respectively. In other words, the collector of the first additional transistor Q_{o1} is connected to the first collector regions of the first primary transistors Q_{if} of the first through (n + 1)-th units while the emitter of the first additional transistor Q_{o1} is connected to the second collector regions of the second primary transistors Q_{is} of the first through (n + 1)-th units. The collector of the first additional transistor Q_{o1} is connected in common to a base of the first additional transistor Q_{o1} and also to a base of the second additional transistor Q_{o2}.

The second additional transistor Q_{o2} has an emitter which is connected in common to the emitter of the first additional transistor Q_{o1} on one hand and which is connected to the first source terminal (V_{cc}) on the other hand. A collector of the second additional transistor Q_{o2} is connected to a smoothing circuit comprising a resistor R_{o1} and a capacitor C_{o1} which are connected in parallel. As a result, a collector current I_o of the second additional transistor Q_{o2} is sent to the resistor R_{o1} to be converted into an output voltage V_{log} from an adder output terminal 25. The collector current I_o is substantially equal to a sum of the first through (n + 1)-th collector currents I_{c11} to $I_{c1(n+1)}$ of the first kind. In Fig. 1, the sum is represented by I_o'. Therefore, the output voltage V_{log} is representative of the d.c. level of the circuit input signal V_{IN} and may therefore be referred to as a field strength signal.

Now, consideration will be directed to the i-th unit which is operable in cooperation with the (i-1)-th amplifier on the assumption that the (i-1)-th amplifier produces an (i-1)-th amplifier output signal V_{i-1}. As readily understood from Fig. 1, the following equation holds;

$$V_{bef} - V_{bes} + V_{i-1} = 0, \qquad (1)$$

where V_{bef} is representative of a base-emitter voltage of the first primary transistor Q_{i1}; V_{bes}, a base-emitter voltage of the second primary transistor Q_{i1}.

As known in the art, each of the base-emitter voltages can be related to a saturation current of a transistor and to V_T which is generally called the voltage equivalent of temperature and which is given by:

$$V_T = k'T/q,$$

where k' represents the Boltzmann constant; q, an electronic charge; and T, an absolute temperature. It is to be noted here that the above-mentioned area factor k has no direct connection with the Boltzmann constant k'. Taking this into consideration, V_{bef} and V_{bes} are given by:

$$V_{bef} = V_T \, 1n \, (I_{c1i}/I_{sii}) \qquad (2)$$

and

$V_{bes} = V_T \ln (I_{ci2}/I_{si2})$, (3)

where I_{si1} and I_{si2} represent saturation currents of the first and the second primary transistors Q_{if} and Q_{is}, respectively. In addition, suffixes i are also attached to the saturation currents to specify the i-th unit, as are the cases with the first- and the second-kind collector currents I_{ci1} and I_{ci2}.

In order to calculate the first- and the second-kind collector currents I_{ci1} and I_{ci2}, consideration will be made about a current amplification factor of each of the first and the second primary transistors depicted at α_F. In this event, a relationship between a constant current of the constant current source I_{i1} and the first- and the second-kind collector currents I_{ci1} and I_{ci2} is given by:

$I_{ci1} + I_{ci2} = (1/\alpha_F)\, I_{i1}$. (4)

On the other hand, the saturation currents I_{si1} and I_{si2} are proportional to the areas of the emitter regions of the first and the second primary transistors Q_{if} and Q_{is} and a relationship between the above-mentioned saturation currents is therefore given by:

$I_{si1}/I_{si2} = 1/k$. (5)

From Equations 1, 2, 3, 4, and 5, the first-and the second-kind collector currents I_{ci1} and I_{ci2} are represented by:

$I_{ci1} = \alpha_F I_{i1} / (1 + k\exp(-V_{i-1}/V_T))$ (6)

and

$I_{ci2} = \alpha_F I_{i1} / (1 + (1/k)\exp(V_{i-1}/V_T))$ (7)

Referring to Fig. 2, wherein the abscissa and the ordinate represent a ratio of (V_{i-1}/V_T) and I_{ci1}, respectively, a curve 30 represents a relationship expressed by Equation 6 on the assumption that α_F and k are equal to unity and exp 2, respectively. Herein, let exp 2 be approximately equal to 7.389. As readily understood from Fig. 2, the curve 30 exhibits a half-wave rectification and saturation characteristic. This shows that the first-kind collector current I_{ci1} has the half-wave and saturation characteristic with respect to V_{i-1} given from tho (i-1)-th amplifier.

Accordingly, each of the first through (n+1)-th units produces a collector current having a current waveform shown at a curve 31 when a waveform of an input signal varies with time as specified by a curve 32. At any rate, the collector current has a d.c. current level depicted at $\overline{I_{ci1}}$ in Fig. 2.

Referring back to Fig. 1, the amplifier output signal V_i becomes large with an increase of the number i because each amplifier has a gain which is summed up from the first stage to the n-th stage. In other words, the n-th amplifier output signal V_n has a maximum level and the amplifier output signals V_i become successively small with a decrease of the number i.

This shows that saturation at first begins at the first-kind collector current $I_{c1(n+1)}$ of the (n+1)-th unit of the measuring circuit 22 when the circuit input signal V_{IN} is increased. Thereafter, the remaining collector currents I_{c1n} through I_{c11} are successively put into saturated states. As a result, the first-kind collector current I_{c11} of the first unit is finally saturated. Such first-kind collector currents I_{ci1} of the first through (n+1)-th units are summed up by the adder circuit 23 to be smoothed into the output voltage V_{log} by the parallel circuit of the resistor R_{01} and the capacitor C_{01}. The resultant collector current I_o exhibits, with respect to the circuit input signal V_{IN}, a logarithmic characteristic approximated by a straight line.

Consideration will be made about an additional output current I_o' which flows through the collector of the first additional transistor Q_{01} and which is substantially equal to the output current I_o. The additional output current I_o' is equal to a total sum of the first-kind collector currents I_{ci1} of the first primary transistors Q_{if}. Therefore, the additional output current I_o' is given by:

$$I_o' = \sum_{i=1}^{n+1} I_{ci1}.$$

If a d.c. component of the additional output current I_o' is represented by $\overline{I_o}'$, the following equation holds:

$$\overline{I_o}' = \sum_{i=1}^{n+1} \overline{I_{cli}}.$$

Referring to Fig. 3 together with Fig. 1, a characteristic of the d.c. output current $\overline{I_o}$ is illustrated on the assumption that k and the gain of each stage of the amplifiers are equal to 7.389 and G_o dB, respectively.

Under the circumstances, the output voltage V_{log} is given by:

$V_{log} = R_{o1} \times I_o$.

Therefore, the output voltage V_{log} has the logarithmic characteristic with respect to the circuit input signal V_{IN}.

Referring to Fig. 4, an intermediate frequency amplification circuit according to a modification of the first embodiment is similar in structure to that illustrated in Fig. 1 except that the adder circuit 23 comprises a series circuit of a resistor R_{o1} and a capacitor C_{o1} instead of a combination of the parallel circuit of the resistor and the capacitor and the current mirror circuit. As shown in Fig. 4, the resistor R_{o1} is connected between the first source terminal and the output terminal 25 while the capacitor C_{o1} is connected between the output terminal 25 and a second source terminal grounded. The collector regions of the first primary transistors Q_{if} are connected in common to the output terminal 25 while the collector regions of the second primary transistors Q_{is} are connected to the first source terminal (V_{cc}).

In the illustrated circuit, the output voltage V_{log} is given by:

$V_{log} = Vcc - R_{o1} \overline{I_o}$,

where Vcc represents the first source voltage supplied to the first source terminal. With this structure, it is possible to reduce the first source voltage Vcc to 1.0 volt or so. Therefore, the first source voltage V_{cc} becomes low in comparison with that illustrated in Fig. 1.

As readily understood from Fig. 3, it is possible to expand a dynamic range of the logarithmic characteristic by increasing both of the amplifier stages and the units and to improve linearity of the logarithmic characteristic by selecting each gain of the amplifier stages and the units. Thus, only one capacitor may be included in the illustrated circuit and may be connected to the output terminal 25 for V_{log}. This shows that the capacitor C_{o1} may be connected outside of an integrated circuit. It is, therefore, possible to lower an intermediate frequency.

Referring to Fig. 5, an intermediate frequency amplification circuit according to a second embodiment of this invention is similar to that illustrated in Fig. 1 except that each of the first through (n+1)-th differential units illustrated in Fig. 5 comprises an internal circuit different from that of Fig. 1 and is depicted at B_1 through B_{n+1}. In this connection, the first through n-th differential amplifier stages are depicted at A_1 to A_n in Fig. 5. Therefore, description will be mainly directed to an i-th differential unit B_i as a representative of the differential units B_1 to B_{n+1}. Briefly, each of the illustrated differential units B_1 to B_{n+1} has a full-wave rectification characteristic, differing from the units illustrated with reference to Fig. 1. In order to accomplish such a full-wave rectification characteristic, the i-th differential unit B_i comprises a primary differential circuit of first and second primary transistors Q_{if} and Q_{is} similar to those illustrated with reference to Fig. 1. Accordingly, the emitter regions of the first and the second primary transistors Q_{if} and Q_{is} have the emitter areas specified by 1:k. Therefore, the area factor is represented by k, as is the case with Fig. 1.

In the example being illustrated, the i-th differential unit further comprises an additional differential circuit of first and second subsidiary transistors Q_{it} and Q_{io} which may be similar to the second and the first primary transistors Q_{if} and Q_{is}, respectively. Therefore, the first subsidiary transistor Q_{it} has the emitter area equal to k-times the emitter area of the second subsidiary transistor Q_{io}. Anyway, an area factor between the emitter areas of the first and the second subsidiary transistors Q_{it} and Q_{io} is represented by k. For brevity of description, the first and the second primary transistors Q_{if} and Q_{is} may be named first and second transistors, respectively, while the first and the second subsidiary transistors Q_{it} and Q_{io} may be called third and fourth transistors, respctively.

The third and the fourth transistors Q_{it} and Q_{io} have the emitter regions connected in common to a subsidiary constant current source depicted at I_{i2}. The base region of the third transistor Q_{it} is connected in common to the base region of the first transistor Q_{if} while the base region of the fourth transistor Q_{io} is connected in common to the base region of the second transistor Q_{is}. Moreover, the collector regions of the second and the third transistors Q_{is} and Q_{it} are connected in common to each other while the collector regions of the first and the fourth transistors Q_{if} and Q_{io} are also connected in common to each other.

From this fact, it is seen that the base regions of the third and the fourth transistors Q_{it} and Q_{io} are supplied with the output signal V_{i-1} of the (i-1)-th amplifier stage A_{i-1} in the manner illustrated in Fig. 5 while the base regions of the third and the fourth transistors Q_{1t} and Q_{1o} are supplied with the circuit input signal V_{IN}.

As a result, the collector regions of the first and the fourth transistors Q_{if} and Q_{io} are connected to the first adder input terminal of the adder circuit 23 while the collector regions of the first and the second transistor Q_{if} and Q_{is} are connected to the second adder input terminal of the adder circuit 23. The adder circuit 23 is similar in structure and operation to that illustrated in Fig. 1 and sums up collector currents I_{ci1} and I_{ci4} of the first and fourth translators Q_{if} and Q_{io} of the respective differential units B_1 to B_{n+1}. A result of the above-mentioned sum is produced through the collector of the transistor Q_{o2} as the output current which is depicted at a d.c. component $\bar{I}_o$ of the output current I_o in Fig. 5. The output current I_o is converted into a d.c. output voltage V_{log} by the capacitor C_{o1} and the resistor R_{o1}.

Now, description will be made about the i-th differential unit B_i on the assumption that the collector currents of the first and the fourth transistors Q_{i1} and Q_{i4} are represented by I_{ci1} and I_{ci4} and the output signal of the (i-1)-th amplifier stage A_{i-1} is represented by V_{i-1}. A sum I_i of the collector curents I_{ci1} and I_{ci4} can be calculated in a manner similar to that mentioned in conjunction with Fig. 1 and is given by:

$$\begin{aligned} I_i &= I_{ci1} + I_{ci4} \\ &= (\alpha_F\, I_{i1}) \,/\, (1 + (1/k)\, \exp(V_{i-1}/V_T)) \\ &\quad + (\alpha_F\, I_{i1}) \,/\, (1 + (1/k)\, \exp(-V_{i-1}/V_T)) \\ &= \alpha_F\, I_{i1}\, (1 + (k - 1/k) \div (2 \cosh\, (V_1/V_T) \\ &\quad + (k + 1/k)). \qquad (8) \end{aligned}$$

Inasmuch as cosh (V_1/V_T) be equal to cosh $(-V_1/V_T)$ as known in the art, Equation (8) represents an even function. Therefore, the sum I_i exhibits a characteristic symmetrical with respect to $V_{i-1} = 0$.

Referring to Fig. 6, wherein the abscissa and ordinate represent (V_{i-1}/V_T) and $\alpha_F\ I_i$, respectively, a relationship between V_{i-1} and I_i is specified by a curve 41 when k is equal to three. When the V_{i-1} varies with time as shown at a curve 42, the output current I_i also varies as depicted at a curve 43.

From the curve 41, it is seen that each differential unit has the full-wave rectification characteristic and a limiting characteristic.

Referring back to Fig. 5, saturation and limiting take place from the collector currents of the first and the fourth transistors $Q_{n+1,1}$ and $Q_{n+1,4}$ of the (n+1)-th differential unit B_{n+1}, like in Fig. 1. On occurrence of such saturation, the collector current I_{n+1} is nearly equal to zero. Under the circumstances, the logarithmic characteristic is accomplished by summing up the collector currents I_{ci1} and I_{ci4} and by smoothing them.

For example, the collector current I_i of the i-th differential unit B_i is equal to $\alpha_F\ I_{i1}\ /\ (1+k)$ on reception of no signal. On the other hand, the collector current I_i becomes zero when saturation occurs as a result of reception of a large signal.

Taking the above into consideration, a d.c. component $\bar{I}_o$ of the output current I_o in the adder circuit 23 is given by:

$$\bar{I}_o = \sum_{i=1}^{n+1} \alpha_F\, I_{i1} \left(1 + \frac{1 - 1/k}{2 \cosh\, (V_{i-1}/V_T) + k + (1/k)} \right) \qquad (9)$$

Referring to Fig. 7, a curve 45 shows a variation of the d.c. component $\bar{I}_o$ shown by Equation (9) on condition that the area factor k and the gain of each differential unit are equal to 3 and G_o, respectively. The illustrated curve 45 is drawn as a result of addition of curves 45_1 through $45_{(n+1)}$ which specify the collector currents I_1 to I_{n+1}.

Inasmuch the output voltage V_{log} is given by:
$V_{log} = R_{o1} \overline{I}_o$,
the output voltage V_{log} varies as depicted at a curve 46.

As shown by the curves 45 and 46, the output current I_o and the output voltage V_{log} have the logarithmic characteristics approximated by polygonal lines.

The amplification circuit illustrated in Fig. 5 is operable by the source voltage V_{cc} of 1.5V. Therefore, it is possible to reduce the source voltage V_{cc}.

Referring to Fig. 8, an intermediate frequency amplification circuit according to a modification of the second embodiment is similar in structure and operation except that the adder circuit 23 comprises a series connection of a resistor R_{o1} and a capacitor connected to the first and the second source terminals, instead of a combination of the current mirror circuit and the parallel connection of the resistor R_{o1} and the capacitor C_{o1} illustrated in Fig. 5.

With this structure, the output voltage V_{log} is given by:

$$V_{log} = V_{cc} - R_{o1} \overline{I}_o,$$

and can be further reduced in comparison with that illustrated in Fig. 5. In fact, the amplification circuit illustrated in Fig. 8 is operable by the source voltage V_{cc} of 1.0V.

Referring to Fig. 9, an intermediate frequency amplification circuit according to a third embodiment of this invention comprises similar parts designated by like reference numerals and symbols. In Fig. 9, the illustrated amplification circuit is supplied with the circuit input signal V_{IN} through an antenna 51, a radio frequency (RF) amplifier 52, a frequency converter 53, and an intermediate frequency (IF) filter 54 to supply the circuit output signal V_{out} and the field strength signal or output signal V_{log} to a detector 56 and an analog-to-digital (A/D) converter 57, respectively.

Like in Fig. 5, the amplification circuit has the first and the second source terminals supplied with the source voltage V_{cc} thereacross and comprises an amplification part 21 similar to that illustrated in Fig. 5, a measuring part 22 to be described in detail later, and an adder circuit 23 of a series connection of a resistor R_{o1} and a capacitor C_{o1} which is similar to that illustrated in Figs. 4 and 7. The field strength signal V_{log} is derived from a point P1 of connection between the resistor R_{o1} and the capacitor C_{o1}. The point P1 of connection may therefore be called an output terminal.

Now, the illustrated measuring part 22 comprises first through (n+1)-th differential units B_1 to B_{n+1} which are connected to the amplifier stages A_1 to A_n in the manner described in conjunction with Figs. 1 and 5, respectively, and which are similar in structure to one another. Under the circumstances, the first differential unit B_1 alone will be described as a representative of the differential units B_1 and B_{n+1}.

In Fig. 9, the illustrated differential unit B_1 comprises first through sixth unit transistors Q_{11}, Q_{12}, Q_{13}, Q_{14}, Q_{15} and Q_{16} which may be generally represented by Q_{i1} to Q_{i6}, respectively, and which are divided into an odd number group of the first, the third, and the fifth unit transistors Q_{i1}, Q_{i3}, and Q_{i5} and an even number group of the second, the fourth and the sixth unit transistors Q_{i2}, Q_{i4}, and Q_{i6}. The unit transistors Q_{i1}, Q_{i3}, and Q_{i5} of the odd number group have collector regions connected in common to the point P1 of connection and which may collectively be referred to as a first group of transistors. The unit transistors of the first odd number group further have emitter regions each of which has an emitter area depicted at S_o. The unit transistors Q_{i2}, Q_{i4}, and Q_{i6} of the even number group have collector regions connected in common to the first source terminal (V_{cc}) and emitter regions which have emitter areas equal to $k_{11}S_o$, $k_{12}S_o$, and $k_{13}S_o$ where k_{11}, k_{12}, and k_{13} are greater than unity.

The base regions of the odd number group transistors of the first differential unit B_1 are connected in common to the base of the transistor Q_{11} of the amplifier stage A_1 while the base regions of the even number group transistors of the first differential unit B_1 are connected in common to the base of the transistor Q_{12} of the amplifier stage A_1.

As readily understood by comparing Fig. 9 with Fig. 5, the base regions of the odd number group transistors of the second through (n+1)-th differential unit are connected in common to the collector of the second transistor $Q_{(i-1)2}$ of the (i-1)-th amplifier stage A_{i-1} while the base regions of the even number group transistors of the second through (n+1)-th differential units A_2 to A_{n+1} are connected in common to the collector of the first transistor $Q_{(i-1)1}$ of the (i-1)-th amplifier stage A_{i-1}.

Each transistor of the odd number group is paired with a selected one of the even number transistors. More particularly, the first and the second transistors Q_{11} and Q_{12} have the emitter regions connected in common to a first subsidiary constant current source specified by a constant current I_{11} through first and second emitter resistors R_{e1} and R_{e2}, respectively. The first and the second unit transistors Q_{11} and Q_{12} may be made to correspond to the first and the second primary transistors Q_{if} and Q_{is} described with reference to Fig. 1.

The third and the fourth unit transistors Q_{13} and Q_{14} have the emitter regions connected to a second subsidiary constant current source (I_{12}) through third and fourth emitter resistors R_{e3} and R_{e4}, respectively. The third and the fourth unit transistors Q_{13} and Q_{14} may be made to correspond to the second and the first additional transistors Q_{l0} and Q_{ll} illustrated in Fig. 5, respectively.

Likewise, the fifth and the sixth unit transistors Q_{15} and Q_{16} have the emitter regions connected to a third subsidiary constant current source (I_{13}) through fifth and sixth emitter resistors R_{e5} and R_{e6}, respectively, and may be called first and second subsidiary transistors, respectively.

It is assumed that the second, the fourth, and the sixth emitter resistors R_{e2}, R_{e4}, and R_{e6} are given by:

$R_{e2} = (1/k_{11})\ R_{e1}$
$R_{e4} = (1/k_{12})\ R_{e3}$
and
$R_{e6} = (1/k_{13})\ R_{e5}$

Herein, the number of the transistor pairs may be generalized into m_1 in addition to the number of the emitter register pairs. In this event, the transistors Q_{11}, Q_{13}, and Q_{15} of the odd number group can be represented by $Q_{1,2m1-5}$; $Q_{1,2m1-3}$; and $Q_{1,2m1-1}$,respectively, while the transistors Q_{12}, Q_{14}, and Q_{16} of the even number group can be represented by $Q_{1,2m1-4}$; $Q_{1,2m1-2}$; and $Q_{1,2m1}$, respectively, when $m_1 = 3$.

Likewise, the resistors R_{e1}, R_{e3}, R_{e5} may be generalized into R_{e2m1-5}, R_{e2m1-3}, R_{e2m1-1} while the resistors R_{e2}, R_{e4}, R_{e6} can be replaced by R_{e2m1-4},R_{e2m1-2}, and R_{e2m1}.

As regards Fig. 9, collector currents of the first, the third, and the fifth unit transistors Q_{11}, Q_{13}, and Q_{15} are assumed to be represented by I_{c11}, I_{c13}, and I_{c15}, respectively. Under the circumstances, relationship among the circuit input signal V_{IN}, the collector currents I_{c11}, I_{c13}, and I_{c15}, and the constant currents, I_{11}, I_{12}, and I_{13} are given by:

$$\begin{aligned} V_{IN} &= V_T \ln (1/k_{11})\ ((\alpha_F I_{11}/I_{c11}) - 1) \\ &\quad + (R_{e1} /\alpha_F)\ (((1/k1) + 1)\ I_{c11} + \alpha_F I_{11}) \\ &= V_T \ln (1/k_{12})\ ((\alpha_F I_{12})/I_{c12}) - 1) \\ &\quad + (R_{e2}/\alpha_F)\ (((1/k_{12}) + 1)\ I_{c12} + \alpha_F I_{12}) \\ &= V_T \ln (1/k_{13})\ ((\alpha_F I_{13}/I_{c13}) - 1) \\ &\quad + (R_{e3}/\alpha_F)\ (((1/k_{13}) + 1)\ I_{c13} + \alpha_F I_{13}), \end{aligned} \tag{10}$$

where α_F is representative of a current amplification factor.

When, each of the first through (n+1)-th differential units B_1 to B_{n+1} may comprise first through m_1-th pairs of the transistors selected from the odd and the even number groups of the transistors, introduction may be made about a variable j which is variable between unity and m_1, both inclusive. Taking this into account, Equation (10) is generalized into:

$$V_{IN} = V_T\ 1n\ (1/kj)\ ((\alpha_F I_{1j}/I_{c1,2j-1}) - 1) + (R_{ej}/\alpha_F)\ (((1/k_{1j}) + 1)\ I_{c1,2j-1} + \alpha_F I_{1j}) \qquad (11)$$

Differentiation of Equation (11) with respect to $I_{c1,2j-1}$ gives:

$$dV_{IN}/dI_{c1,2j-1}$$
$$= -(V_T \alpha_F I_{1j}) / I_{c1,2j-1}{}^2\ ((\alpha F\ I_{1j}/I_{c1,2j-1}) - 1 + R_{e1}/\alpha_F\ ((1/k_{1j}) + 1). \qquad (12)$$

If $I_{c1,2j-1} = \alpha_F I_{1j}/2$, Equation (12) is rewritten into:

$$dV_{IN}/dI_{c1,2j-1} = (-4V_T/\alpha_F I_{1j}) + (R_{ej}/2)\ ((1/k_{1j}) + 1). \qquad (13)$$

Likewise, Equation (11) is rewritten into:

$V_T = (1/2) R_{ej} I_{1j} ((1/k_{1j}) + 3) - V_T 1n k_{1j}$.   (14)

If a tangential line specified by Equation (12) passes through an origin, division of Equation (14) by ($\alpha_F I_{1j}/2$) gives:

$$\begin{aligned} V_{IN}/(\alpha_F I_{1j}/2) &= ((1/2) R_{ej} I_{1j} ((1/k_{1j}) + 3) \\ &\quad - V_T \ln k_{1j}) / (\alpha_F I_{1j}/2) \\ &= (-4V_T/I_{1j}) + ((1/k_{1j}) + 1) R_{ej}/\alpha_F . \end{aligned}$$

Accordingly, the following equation (15) holds:

$R_{e1} I_{1j} = V_T (-2 + 1n k_{1j})$.   (15)

Referring to Fig. 10, the collector current $I_{c1,2j-1}$ exhibits a half-wave rectification waveform in response to the circuit input signal V_{IN} , as shown by curves 61 and 62 as long as k_{1j} is equal to or greater than exp 2, because Equation (15) is positive when k_{1j} falls within the above-mentioned range.

With this structure, it is possible to respond to a wide range of the circuit input signal V_{IN} and therefore to expand a dynamic range. With an increase of the circuit input signal V_{IN}, saturation takes place and the collector current gradually becomes near to $\alpha_F I_{1j}$.

On the other hand, consideration will be made about a predetermined constant determined by:

$y_{1j} = 4 / (k_{1j} + (1/k_{1j}) + 2)$,

and about gain g_{o1} of the first amplifier stage A1 given by:

$g_{o1} = (R_{11} I1/ 2V_T)$.

As regards the gain g_{o1} , it is possible to design the area factors k_{1j} and k_{1j+1} of the transistors of the first differential unit B_1 such that the following equation (18) holds:

$$y_{1j+1}/y_{1j} = \sqrt[m]{g_{o1}} . \qquad (18)$$

In this event, each input signal level which gives the relationship of $I_{c1,2j-1} = (\alpha_F I_{1j}/2)$ differs from one another in each differential unit B_1 and B_{n+1} by

$$\sqrt[m]{g_{o1}} .$$

Therefore, the output current I_o of the adder circuit 23 is given by:

$$I_o = \sum_{i=1}^{n+1} \sum_{j=1}^{mi} I_{c1,2j-1} . \qquad (19)$$

Since each collector current $I_{c1,2j-1}$ has the same phase, a d.c. component of each collector current $I_{c1,2j-1}$ never disappears even on a sum of the respective collector currents.

Therefore, the output current I_o is given as a logarithmically approximated value with respect to the circuit input signal V_{IN} .

Herein, Equation (18) may be generalized into:

$$y_{i,j+1} / y_{i,j} = \sqrt[mi]{g_{o,j-1}}. \qquad (20)$$

Similar logarithmic characteristic can be accomplished by the use of Equation (20) in relation to the circuit input signal V_{IN} .

If the source voltage and the d.c. component of the output current I_o are represented by V_{cc} and $\bar{I}_o$, respectively, the field strength signal V_{log} is given by:

$$\bar{V}_{log} = V_{cc} - R_{o1} \bar{I}_o.$$

Thus, a logarithmic value of the circuit input signal V_{IN} is produced in the form of a d.c. voltage.

Referring to Fig. 11, a relationship between the circuit input signal V_{IN} and the output current I_o is specified by the logarithmic characteristic.

Referring to Fig. 12, an intermediate frequency amplification circuit according to a fourth embodiment of this invention is specified only by each differential unit which is represented by an n-th differential unit. The illustrated differential unit comprises third through (2m + 4)-th transistors Q_3 to Q_{2m+4} which are divided into an odd number group and an even number group. The transistors of the odd number group have base regions connected in common to one another while the transistors of the even number group have base regions connected in common to one another. Let the transistors represented by $Q_{n,2j+2}$ and $Q_{n,2j+3}$ have emitter areas represented by 1 and the transistors represented by $Q_{n,2j+1}$ and $Q_{n,2j+4}$ have emitter areas given by km, as symbolized by thick lines in Fig. 12.

Each emitter region of the transistors is connected to an emitter resistor depicted at a corresponding suffix. Herein, a relationship between a pair of the resistors is defined by:

$$R_{n,2j+1} = kj\, R_{n,2j+2},$$

where j = 1, 2 ....., m.

Anyway, the emitter regions of the transistors $Q_{n,2j+1}$ and $Q_{n,2j+2}$ or $Q_{n,2j+3}$ and $Q_{n,2j+4}$ are connected to each other through the corresponding resistors. The illustrated differential unit B_n is divisible into first through m-th full-wave rectification units which are driven by constant current sources I_{n1}, I_{n2} ..., I_{nm} and which are represented by B_{n1}, B_{n2}, ..., B_{nm}. Each rectification characteristic of the rectification circuits has a gentle inclination in compliance with a product of $R_{n,2j+1}$ and I_{nj} as compared with that illustrated in Fig. 10.

When such a product of $R_{n,2j+1}$ and I_{nj} is changed with a variation of the number j, it is possible to improve logarithmic approximation because the number of the rectification circuits is increased.

With this structure, a dynamic range of the logarithmic characteristic can be expanded because the circuit input signal level becomes large due to addition of each emitter resistor.

Claims

1. An intermediate frequency amplification circuit operable in response to a circuit input signal (V_{IN}) to produce a circuit output signal (V_{OUT}) subjected to amplification, said intermediate frequency amplification cirucit comprising first through n-th differential amplifiers (1st STAGE ... n-th STAGE; A_1 ... A_n) which have first through n-th amplifier input terminal pairs and first through n-th amplifier output terminal pairs, respectively, and which are connected in cascade from said first to said n-th differential amplifiers by successively connecting the amplifier output terminal pair of a differential amplifier to the amplifier input terminal pair of the next following differential amplifier, said circuit input signal being supplied across said first amplifier input terminal pair while said circuit output signal is produced at said n-th amplifier output terminal pair, said intermediate frequency amplification cirucit further comprising a measuring circuit (22) responsive to said circuit input signal for measuring a field strength to produce a field strength signal (V_{log}) representative of said field strength, said measuring circuit comprising:
   first through (n + 1)-th differential units (1st UNIT ... (n + 1)-th UNIT; B_1 ... B_{n+1}) which have first through (n + 1)-th unit input terminal pairs connected to said first through n-th amplifier input terminal pairs and to said n-th amplifier output terminal pair, respectively, and first through (n + 1)-th unit output terminal pairs supplied with first through (n + 1)-th unit output signals, respectively; and
   an adder circuit (23) connected to said first through (n + 1)-th unit output terminal pairs for adding said

first through (n + 1)-th unit output signals to one another to produce said field strength signal (V_{log});
each of said first through (n + 1)-th differential units comprising:
a primary differential circuit of first and second primary transistors (Q_{1f} ...$Q_{(n+1)f}$, Q_{1s} ...$Q_{(n+1)s}$; Q_{11},Q_{12}; Q_{n5}, Q_{n6}) which have first and second base regions, first and second emitter regions, and first and second collector regions, respectively, said first and said second collector regions being connected to said unit output terminal pair, respectively, characterized in that said first and said second base regions are connected to the amplifier input terminal pair of the related differential amplifier, respectively, while said first and said second emitter regions have an area ratio of 1:k, where k is greater than unity, and are coupled in common to each other.

2. An intermediate frequency amplification circuit as claimed in claim 1, wherein each differential unit comprises:
an additional differential circuit of first and second transistor parts which are differentially connected to each other and which are linked to both of the amplifier input terminal pair of said related differential amplifier and the unit output terminal pair.

3. An intermediate frequency amplification circuit as claimed in claim 2, each of said amplifier input terminal pairs consisting of a first and a second amplifier input terminal, wherein:
said first and said second base regions are connected to said first and said second amplifier input terminals, respectively;
said first transistor part comprising:
a first additional transistor (Q_{10}; Q_{13}; Q_{n4}) which has an emitter region having a predetermined emitter area, a base region connected to said second amplifier input terminal, and a collector region connected in common to the first collector region of said first primary transistor;
said second transistor part comprising:
a second additional transistor (Q_{11}; Q_{14}; Q_{n3}) having an emitter region which has an emitter area equal to k-times said predetermined emitter area of said first additional transistor and which is coupled in common to the emitter region of said first additional transistor, said second additional transistor having a base region connected in common to said first base region, and a collector region connected in common to said second collector region of said second primary transistor.

4. An intermediate frequency amplification circuit as claimed in claim 2, each of said first through n-th amplifier input terminal pairs consisting of first and second amplifier input terminals while each of the unit input terminal pairs consists of first and second unit input terminals, each of the unit output terminal pairs consisting of first and second unit output terminals, wherein:
said first transistor part comprises:
a plurality of first subsidiary transistors (Q_{13},Q_{15}; Q_{n4},Q_{n8},Q_{n9}, ..., Q_{n2m+2}, Q_{n2m+3}) having collector regions connected in common to said first collector region of said first primary transistor, emitter regions having emitter areas substantially equal to that of said first emitter region, and base regions connected in common to said first amplifier input terminal;
said second transistor part comprising:
a plurality of second subsidiary transistors (Q_{14},Q_{16}; Q_{n3},Q_{n7},Q_{n10}, ..., Q_{n2m+1}, Q_{n2m+4}) which equal in number to said first subsidiary transistors and which have collector regions connected in common to the second collector region of said second primary transistor, base regions connected in common to the second base region of said second primary transistor, and emitter regions having emitter areas substantially equal to that of said second emitter region and coupled to the emitter regions of said first subsidiary transistors.

Patentansprüche

1. Zwischenfrequenz-Verstärkerschaltung betreibbar in Abhängigkeit von einem Schaltungseingangssignal (V_{IN}) zur Erzeugung eines Schaltungsausgangssignals (V_{OUT}), das einer Verstärkung ausgesetzt wird, wobei die Zwischenfrequenz-Verstärkerschaltung aufweist erste bis n-te Differenzverstärker (1st STAGE ... n-th STAGE; A_1 ... A_n), die erste bis n-te Verstärker-Eingangsanschlußpaare bzw. erste bis n-te Verstärker-Ausgangsanschlußpaare aufweisen und die in Kaskade von dem ersten bis zum n-ten Differenzverstärker geschaltet sind durch aufeinanderfolgendes Verbinden des Verstärker-Ausgangsanschlußpaares eines Differenzverstärkers mit dem Verstärker-Eingangsanschlußpaar des nächstfolgenden Differenzverstärkers, wobei das Schaltungseingangssignal über das erste Verstärker-Eingangsan-

schlußpaar zugeführt wird, während das Schaltungsausgangssignal am n-ten Verstärker-Ausgangsanschlußpaar erzeugt wird, wobei die Zwischenfrequenz-Verstärkerschaltung ferner eine Meßschaltung (22) aufweist, die abhängig ist vom Schaltungseingangssignal, zum Messen einer Feldstärke zur Erzeugung eines Feldstärkensignals (V_{log}), das die Feldstärke angibt, wobei die Meßschaltung aufweist:

Erste bis (n + 1)-te Differenzeinheiten (1st UNIT ... (n + 1)-th UNIT; B_1 ... B_{n+1}), die erste bis (n + 1)-te Einheits-Eingangsanschlußpaare aufweisen, die mit den ersten bis n-ten Verstärker-Eingangsanschlußpaaren bzw. dem n-ten Verstärker-Ausgangsanschlußpaar verbunden sind, und erste bis (n + 1)-te Einheits-Ausgangsanschlußpaare, die jeweils mit den ersten bis (n + 1)-ten Einheits-Ausgangssignalen versorgt werden, und

einer Addierschaltung (23), die mit den ersten bis (n + 1)-ten Einheits-Ausgangsanschlußpaaren verbunden sind, zum Addieren der ersten bis (n + 1)-ten Einheits-Ausgangssignale miteinander zur Erzeugung des Feldstärkesignals (V_{log}),wobei jede der ersten bis (n + 1)-ten Differenzeinheiten aufweist:

Eine primäre Differenzschaltung aus ersten und zweiten Primärtransistoren (Q_{1f} ... $Q_{(n+1)f}$, Q_{1s} ... $Q_{(n+1)s}$; Q_{11}, Q_{12}; Q_{n5}, Q_{n6}), die erste und zweite Basisbereiche, erste und zweite Emitterbereiche und erste und zweite Kollektorbereiche aufweisen, wobei der erste und der zweite Kollektorbereich mit dem Eingangs-Ausgangsanschlußpaar verbunden sind, dadurch **gekennzeichnet,** daß der erste bzw. der zweite Basisbereich mit dem Verstärker-Eingangsanschlußpaar des zugeordneten Differenzverstärkers verbunden sind, während der erste und der zweite Emitterbereich ein Flächenverhältnis von 1:k aufweisen, wobei k größer als 1 ist, und sie gemeinsam miteinander verbunden sind.

2. Zwischenfrequenz-Verstärkerschaltung nach Anspruch 1, wobei jede Differenzeinheit aufweist:

   Eine zusätzliche Differenzschaltung aus ersten und zweiten Transistorteilen, die differenzartig miteinander verbunden sind und die sowohl mit dem Verstärker-Eingangsanschlußpaar des zugeordneten Differenzverstärkers als auch mit dem Einheits-Ausgangsanschlußpaar verknüpft sind.

3. Zwischenfrequenz-Verstärkerschaltung nach Anspruch 2, wobei jedes der Verstärker-Eingangsanschlußpaare aus einem ersten und einem zweiten Verstärker-Eingangsanschluß besteht, wobei:

   Der erste und der zweite Basisbereich mit dem ersten bzw. dem Zweiten Verstärker-Eingangsanschluß verbunden sind, der erste Transistorteil aufweist:

   Einen ersten Zusatztransistor (Q_{10}; Q_{13}; Q_{n4}), der einen Emitterbereich mit einem vorgegebenen Emitterareal aufweist, einen Basisbereich, der mit dem zweiten Verstärker-Eingangsanschluß verbunden ist, und einen Kollektorbereich, der gemeinsam mit dem ersten Kollektorbereich des ersten Primärtransistors verbunden ist,

   der zweite Transistorteil aufweist:

   Einen zweiten Zusatztransistor (Q_{11}; Q_{14}; Q_{n3}) mit einem Emitterbereich, der eine Emitterfläche gleich k-mal dem vorgegebenen Emitterareal des ersten Zusatztransistors aufweist und der gemeinsam mit dem Emitterbereich des ersten Zusatztransistors gekoppelt ist, wobei der zweite Zusatztransistor einen Basisbereich aufweist, der gemeinsam mit dem ersten Basisbereich verbunden ist, und einen Kollektorbereich, der gemeinsam mit dem zweiten Kollektorbereich des zweiten Primärtransistors verbunden ist.

4. Zwischenfrequenz-Verstärkerschaltung nach Anspruch 2, wobei jedes der ersten bis n-ten Verstärker-Eingangsanschlußpaare aus ersten und zweiten Verstärker-Eingangsanschlüssen besteht, während jedes der Einheits-Eingangsanschlußpaare aus ersten und zweiten Einheits-Eingangsanschlüssen besteht, jedes der Einheits-Ausgangsanschlußpaare aus ersten und zweiten Einheits-Ausgangsanschlüssen besteht, wobei:

   Der erste Transistorteil aufweist:

   Eine Anzahl erster Hilfstransistoren (Q_{13}, Q_{15}; Q_{n4}, Q_{n8}, Q_{n9}, ..., Q_{n2m+2}, Q_{n2m+3}) mit Kollektorbereichen, die gemeinsam mit dem ersten Kollektorbereich des ersten Primärtransistors verbunden sind, Emitterbereiche mit Emitterarealen, die im wesentlichen gleich der des ersten Emitterbereiches sind, und Basisbereiche, die gemeinsam mit dem ersten Verstärker-Eingangsanschluß verbunden sind,

   wobei der zweite Transistorteil aufweist:

   Eine Anzahl zweiter Hilfstransistoren (Q_{14}, Q_{16}; Q_{n3}, Q_{n7}, Q_{n10}, ..., Q_{n2m+1}, Q_{n2m+4}), die in der Anzahl gleich der Zahl der ersten Hilfstransistoren sind und die Kollektorbereiche aufweisen, die gemeinsam mit dem zweiten Kollektorbereich des zweiten Primärtransistors verbunden sind,

   Basisbereiche, die gemeinsam mit dem zweiten Basisbereich des zweiten Primärtransistors verbunden sind, und Emitterbereiche mit Emitterarealen, die im wesentlichen gleich der des zweiten Emitterbereiches sind und mit den Emitterbereichen der ersten Hilfstransistoren verbunden sind.

Revendications

1. Circuit amplificateur à fréquence intermédiaire pouvant être mis en oeuvre en réponse à un signal d'entrée du circuit (V_{IN}) afin de produire un signal de sortie de circuit (V_{OUT}) qui a été amplifié, le circuit amplificateur à fréquence intermédiaire comprenant des premier à $n^{ième}$ amplificateurs différentiels (1er ETAGE, ... $n^{ième}$ ETAGE ; A_1 ... A_n) qui comportent des première à $n^{ième}$ paires de bornes d'entrée d'amplificateur et des première à $n^{ième}$ paires de bornes de sortie d'amplificateur, respectivement, et qui sont reliées en cascade à partir des premier à $n^{ième}$ amplificateurs différentiels en reliant successivement la paire de bornes de sortie d'amplificateur d'un amplificateur différentiel à la paire de bornes d'entrée d'amplificateur du prochain amplificateur différentiel suivant, le signal d'entrée de circuit étant appliqué aux bornes de la première paire de bornes d'entrée d'amplificateur tandis que le signal de sortie du circuit est produit sur la $n^{ième}$ paire de bornes de sortie d'amplificateur, le circuit amplificateur à fréquence intermédiaire comprenant de plus un circuit de mesure (22) sensible au signal d'entrée du circuit afin de mesurer l'intensité du champ afin de produire un signal d'intensité du champ (V_{log}) représentatif de l'intensité du champ, le circuit de mesure comprenant :
   des première à $(n+1)^{ième}$ unités différentielles (1ère UNITE ... $(n+1)^{ième}$ UNITE ; B_1 ... B_{n+1}) qui comportent des première à $(n+1)^{ième}$ paires de bornes d'entrée reliées aux première à $n^{ième}$ paires de bornes d'entrée d'amplificateur et à la $n^{ième}$ paire de bornes de sortie d'amplificateur, respectivement, et des première à $(n+1)^{ième}$ paires de bornes de sortie d'unité qui reçoivent des premier à $(n+1)^{ième}$ signaux de sortie d'unité, respectivement, et
   un circuit additionneur (23) relié aux première à $(n+1)^{ième}$ paires de bornes de sortie d'unité pour additionner les premier à $(n+1)^{ième}$ signaux de sortie d'unité l'un à l'autre afin de produire le signal d'intensité du champ (V_{log}) ;
   chacune des première à $(n+1)^{ième}$ unités différentielles comprenant :
   un circuit différentiel primaire constitué de premier et second transistors primaires (Q_{1f} ... $Q_{(n+1)f}$, Q_{1s} ... $Q_{(n+1)s}$; Q_{11}, Q_{12} ; Q_{n5}, Q_{n6}) qui comportent des première et seconde régions de base, des première et seconde régions d'émetteur et des première et seconde régions de collecteur, respectivement, les première et seconde régions de collecteur étant reliées à la paire de bornes de sortie d'unité, respectivement, caractérisé en ce que les première et seconde régions de base sont reliées aux paires de bornes d'entrée d'amplificateur de l'amplificateur différentiel concerné, respectivement, tandis que les première et seconde régions d'émetteur ont un rapport de surface de 1:k, où k est supérieur à un et sont couplées en commun l'une à l'autre.

2. Circuit amplificateur à fréquence intermédiaire selon la revendication 1, dans lequel chaque unité différentielle comprend :
   un circuit différentiel supplémentaire constitué de première et seconde parties de transistors qui sont différentiellement connectés l'un à l'autre et qui sont reliés à la fois à la paire de bornes d'entrée d'amplificateur et à l'amplificateur différentiel concerné et à la paire de bornes de sortie d'unité.

3. Circuit amplificateur à fréquence intermédiaire selon la revendication 2, dans lequel chacune des paires de bornes d'entrée d'amplificateur est constituée d'une première et d'une seconde bornes d'entrée d'amplificateur, dans lequel :
   les première et seconde régions de base sont connectées aux première et seconde bornes d'entrée d'amplificateur, respectivement ;
   la première partie de transistors comprenant :
   un premier transistor supplémentaire (Q_{10}, Q_{13}, Q_{n4}) qui comporte une région d'émetteur ayant une surface d'émetteur prédéterminée, une région de base connectée à la seconde borne d'entrée d'amplificateur et une région de collecteur connectée en commun à la première région de collecteur du premier transistor primaire ;
   une seconde partie de transistors comprenant :
   un second transistor supplémentaire (Q_{11}, Q_{14}, Q_{n3}) comportant une région d'émetteur qui présente une surface d'émetteur égale à quatre fois la surface d'émetteur prédéterminée du premier transistor supplémentaire et qui est couplée en commun à la région d'émetteur du premier transistor supplémentaire, le second transistor supplémentaire ayant une région de base reliée en commun à la première région de base et une région de collecteur reliée en commun à la seconde région de collecteur du second transistor primaire.

4. Circuit amplificateur à fréquence intermédiaire selon la revendication 2, dans lequel chacune des

première à $n^{ième}$ paires de bornes d'entrée d'amplificateur est constituée de première et seconde bornes d'entrée d'amplificateur tandis que chacune des paires de bornes d'entrée d'unité est constituée des première et seconde bornes d'entrée d'unité, dans lequel chacune des paires de bornes de sortie d'unité est constituée des première et seconde bornes de sortie d'unité, dans lequel :

la première partie de transistors comprend :

une multitude de premiers transistors auxiliaires (Q_{13}, Q_{15} ; Q_{n4}, Q_{n8}, Q_{n9}, ..., Q_{n2m+2}, Q_{n2m+3}) ayant des régions de collecteur reliées en commun à la première région de collecteur du premier transistor primaire, des régions d'émetteur ayant des surfaces d'émetteur pratiquement égales à celles de la première région d'émetteur et des régions de base reliées en commun à la première borne d'entrée d'amplificateur ;

la seconde partie des transistors comprenant :

une multitude de seconds transistors auxiliaires (Q_{14}, Q_{16} ; Q_{n3}, Q_{n7}, Q_{n10}, ..., Q_{n2m+1}, Q_{n2m+4}) qui sont d'un nombre égal aux premiers transistors auxiliaires et qui ont des régions de collecteur reliées en commun à la seconde région de collecteur du second transistor primaire, des régions de base reliées en commun à la seconde région de base du second transistor primaire et des régions d'émetteur ayant des surfaces d'émetteur pratiquement égales à celles de la seconde région d'émetteur et couplées aux régions d'émetteur des premiers transistors auxiliaires.

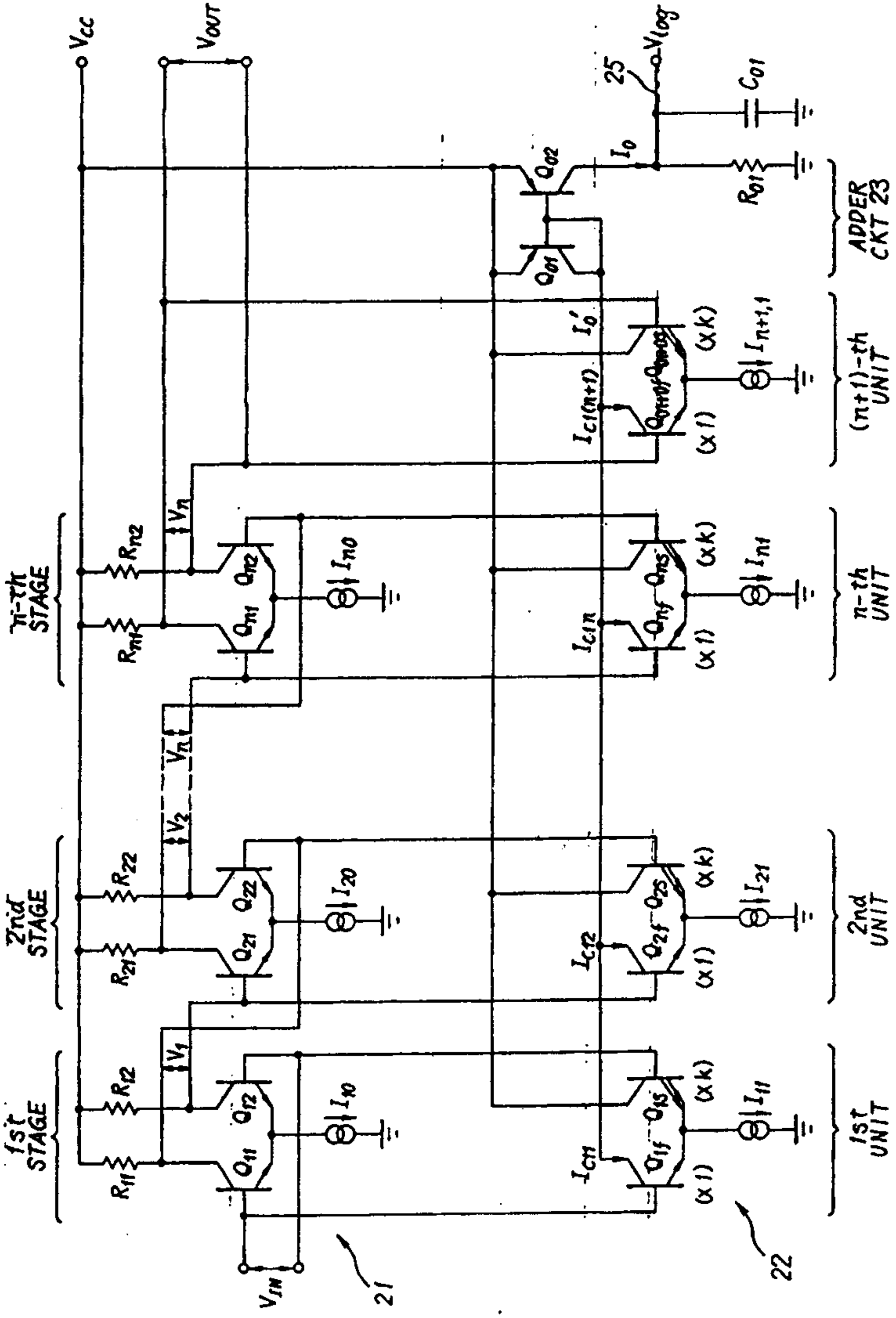
Vcc
VOUT
Vlog
25
C01
I0
Q02
Q01
R01
ADDER CKT 23
I0'
IC1(n+1)
Q(n+1)f
Q(n+1)s
(x1)
(xk)
In+1,1
(n+1)-th UNIT
n-th STAGE
Rn1
Rn2
Vn
Qn1
Qn2
In0
ICIn
Qnf
Qns
In1
n-th UNIT
Vn1
V2
2nd STAGE
R21
R22
Q21
Q22
I20
IC12
Q2f
Q2s
I21
2nd UNIT
V1
1st STAGE
R11
R12
Q11
Q12
I10
IC11
Q1f
Q1s
I11
1st UNIT
VIN
21
22

FIG. 1

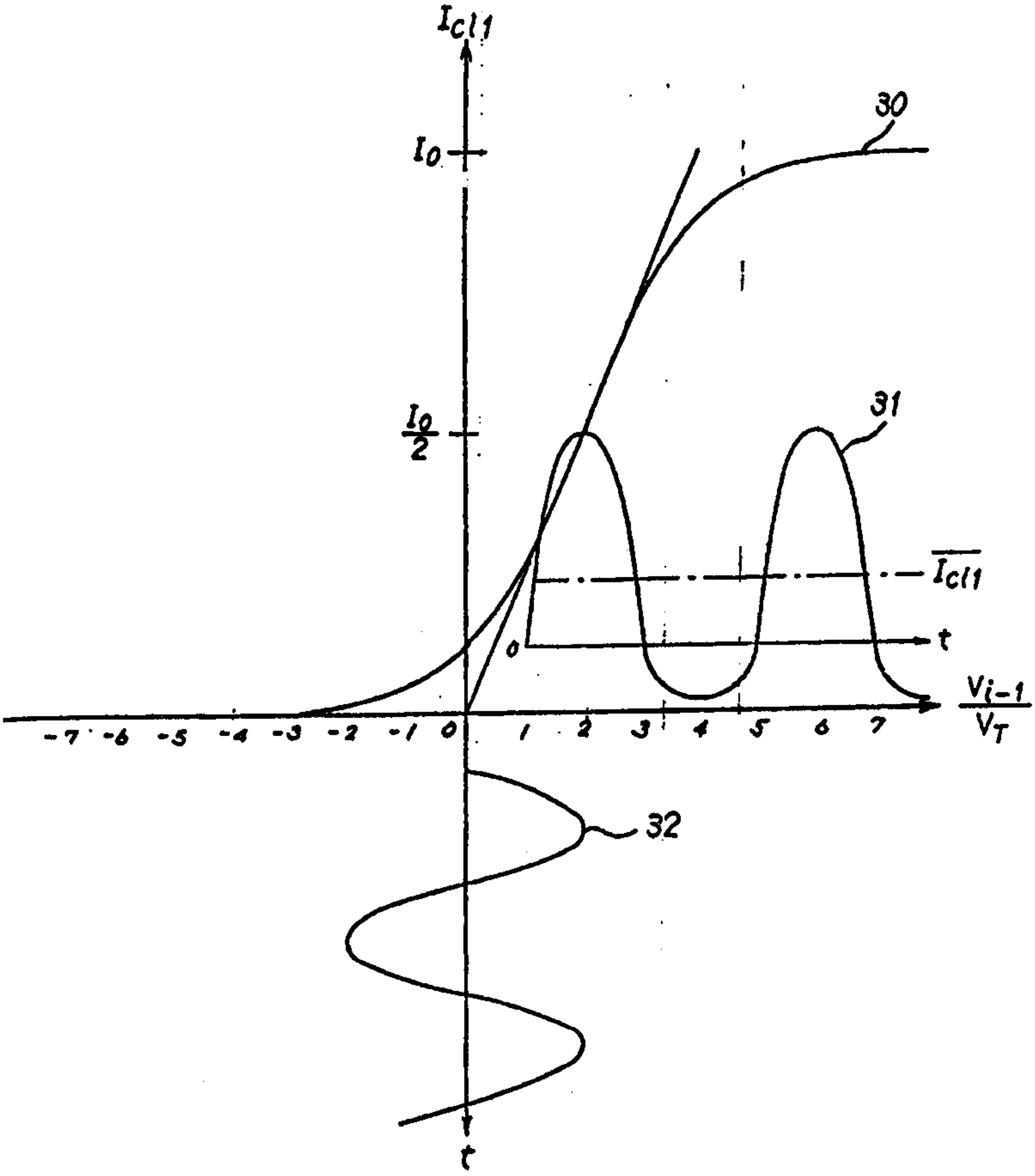
I_{cl1}
I_0
$\frac{I_0}{2}$
30
31
$\overline{I_{cl1}}$
0
t
$\frac{V_{i-1}}{V_T}$
-7
-6
-5
-4
-3
-2
-1
0
1
2
3
4
5
6
7
32
t

FIG. 2

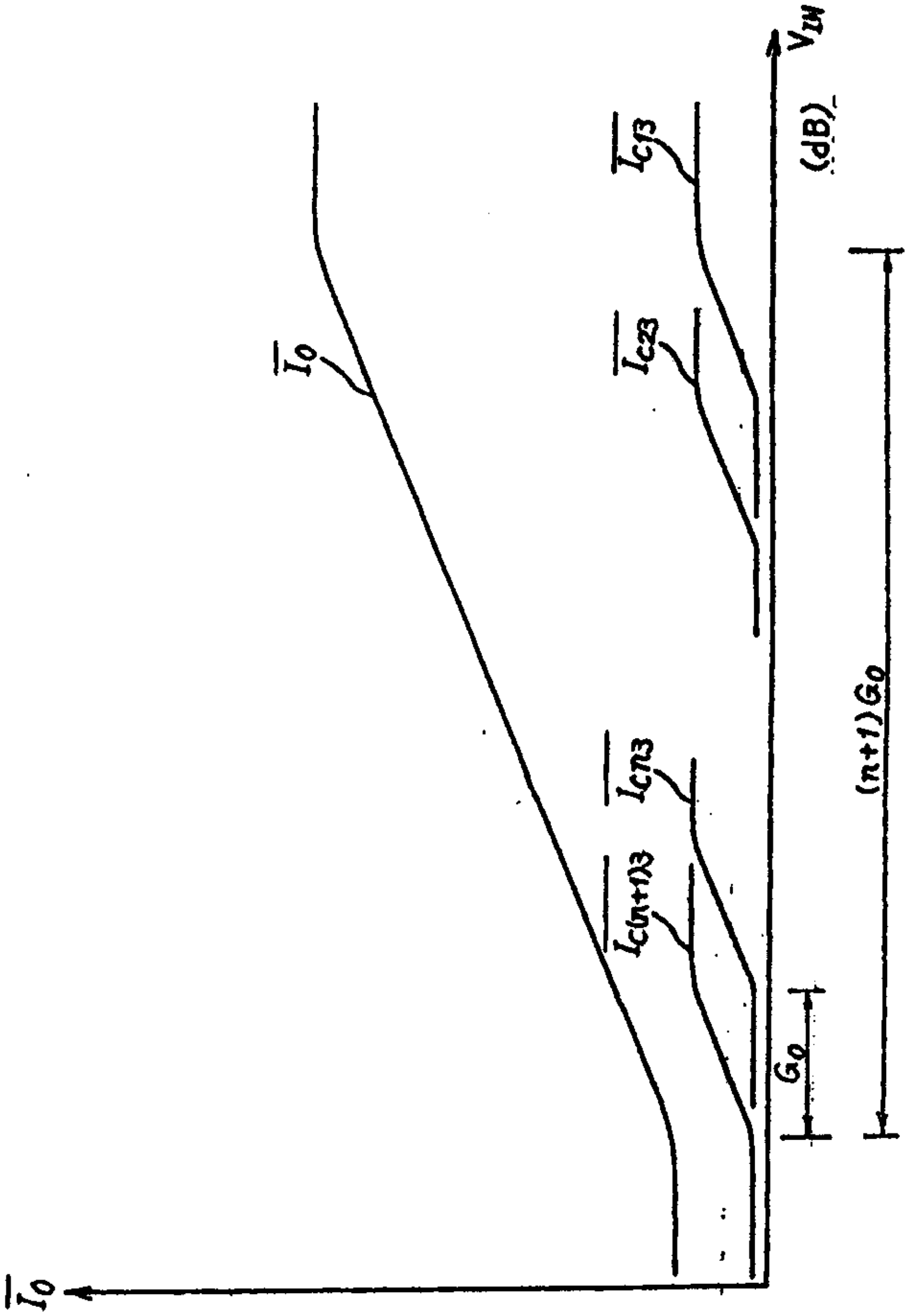
$\overline{I_0}$
$\overline{I_0}$
$\overline{I_{C13}}$
$\overline{I_{C23}}$
$\overline{I_{Cn3}}$
$\overline{I_{C(n+1)3}}$
V_{IN}
(dB)
G_0
$(n+1)G_0$

FIG. 3

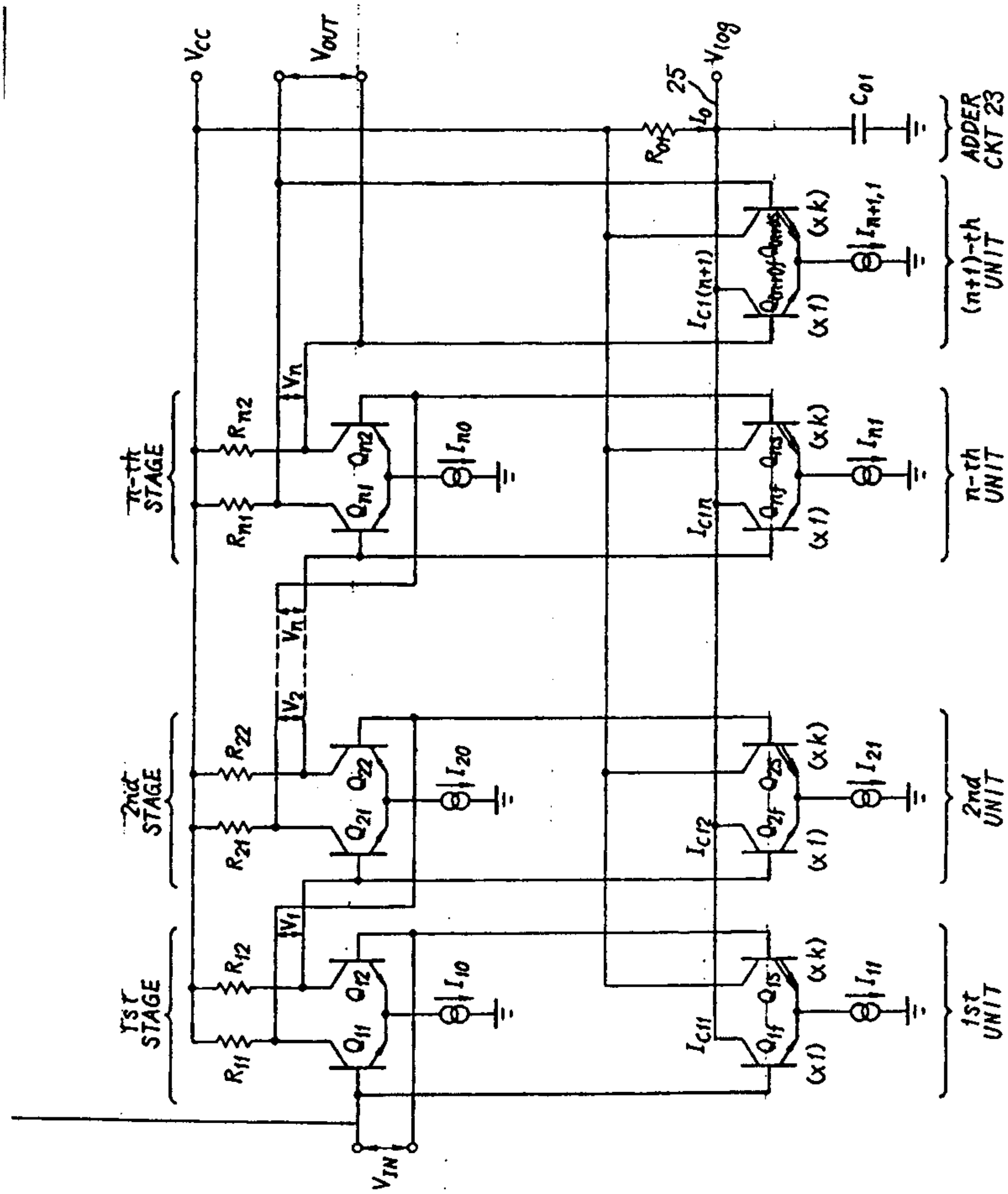
VCC
VOUT
Vlog
25
R01
I0
C01
ADDER CKT 23
1st STAGE
2nd STAGE
n-th STAGE
R11
R12
R21
R22
Rn1
Rn2
Q11
Q12
Q21
Q22
Qn1
Qn2
I10
I20
In0
V1
V2
Vn
VIN
IC11
IC12
IC1n
IC1(n+1)
Q1f
Q1s
Q2f
Q2s
Qnf
Qns
Q(n+1)f
Q(n+1)s
(x1)
(xk)
I11
I21
In1
In+1,1
1st UNIT
2nd UNIT
n-th UNIT
(n+1)-th UNIT

FIG. 4

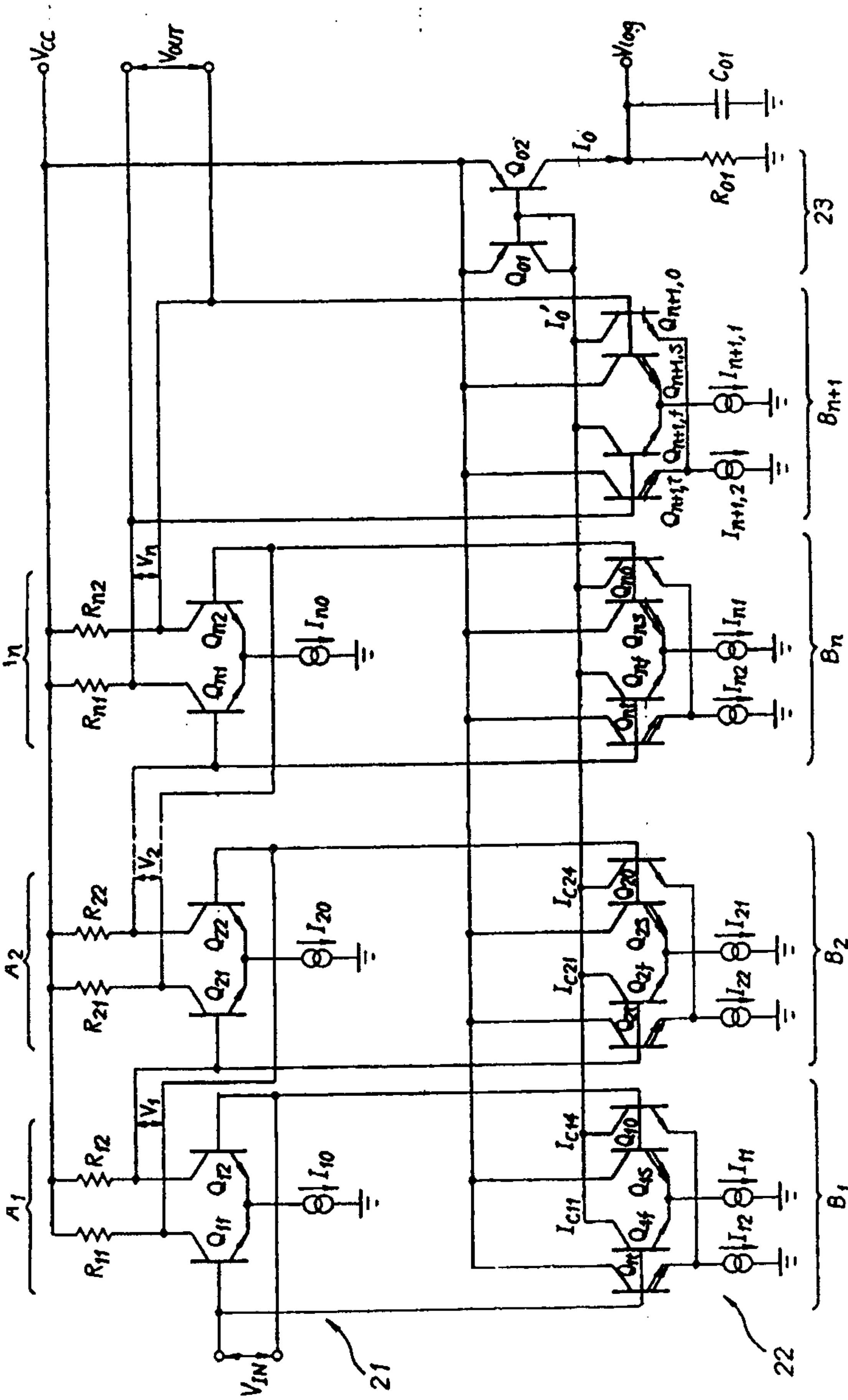
V_CC
V_OUT
V_log
C01
R01
Q01
Q02
I0
I0'
23
Q_{n+1,0}
Q_{n+1,3}
Q_{n+1,1}
Q_{n+1,2}
I_{n+1,1}
I_{n+1,2}
B_{n+1}
V_n
R_{n2}
R_{n1}
Q_{n1}
Q_{n2}
I_{n0}
Q_{n0}
Q_{n3}
Q_{n4}
Q_{n1}
I_{n1}
I_{n2}
B_n
V_2
A2
R22
R21
Q21
Q22
I20
I_{C24}
I_{C21}
Q20
Q23
Q24
Q21
I21
I22
B2
V1
A1
R12
R11
Q11
Q12
I10
I_{C14}
I_{C11}
Q10
Q13
Q14
Q11
I11
I12
B1
V_IN
21
22

FIG. 5

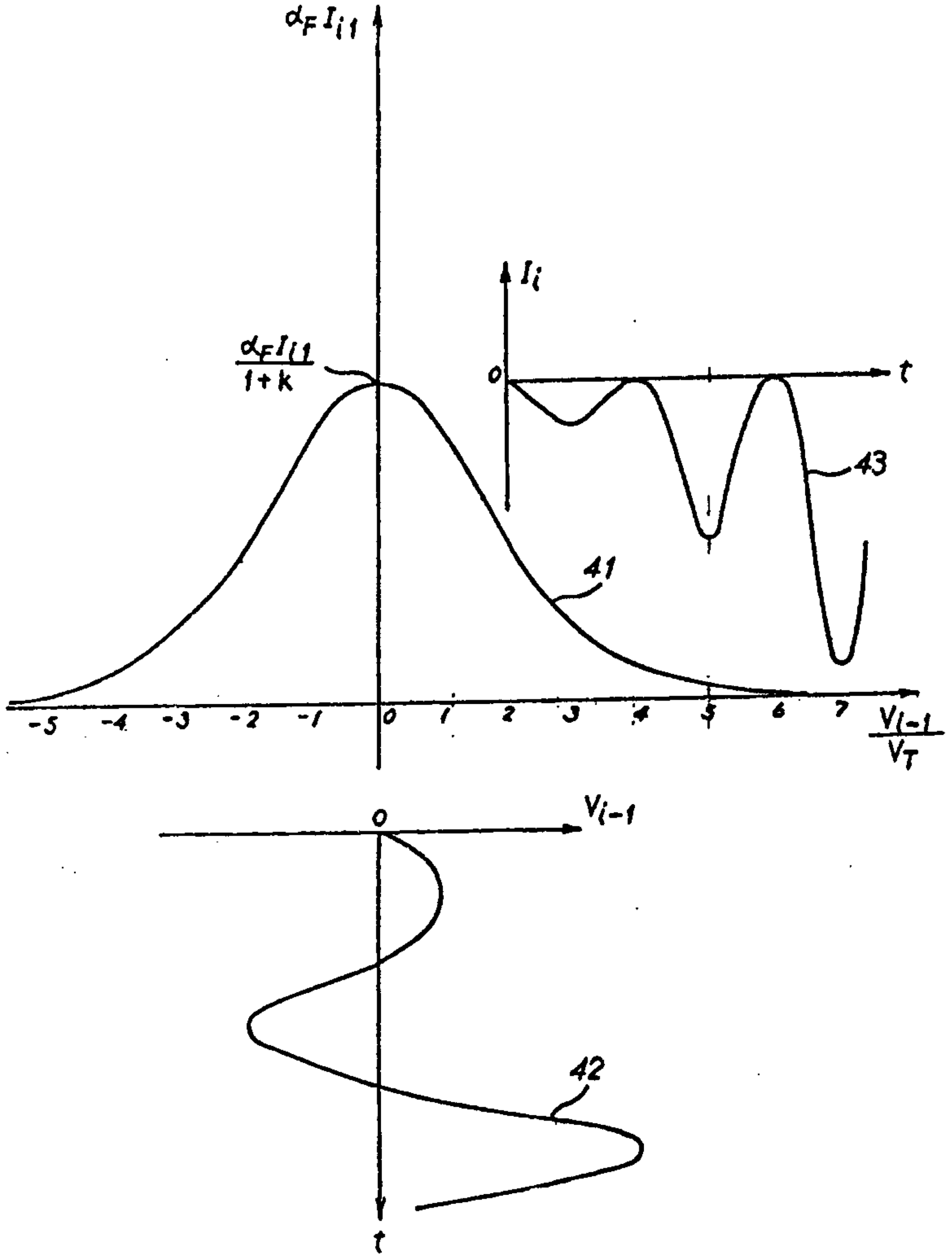
$\alpha_F I_{i1}$
$\frac{\alpha_F I_{i1}}{1+k}$
I_i
0
t
43
41
-5
-4
-3
-2
-1
0
1
2
3
4
5
6
7
$\frac{V_{i-1}}{V_T}$
0
V_{i-1}
42
t

FIG.6

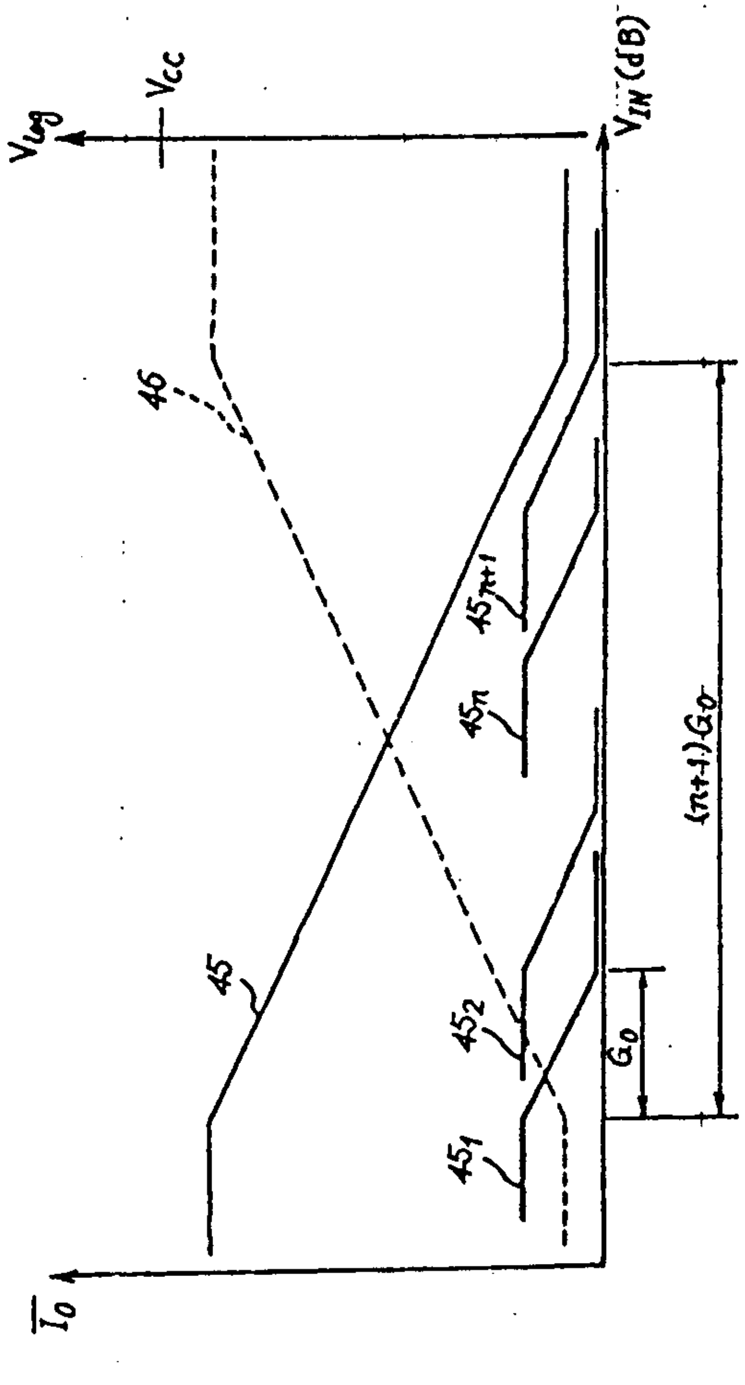

FIG.7

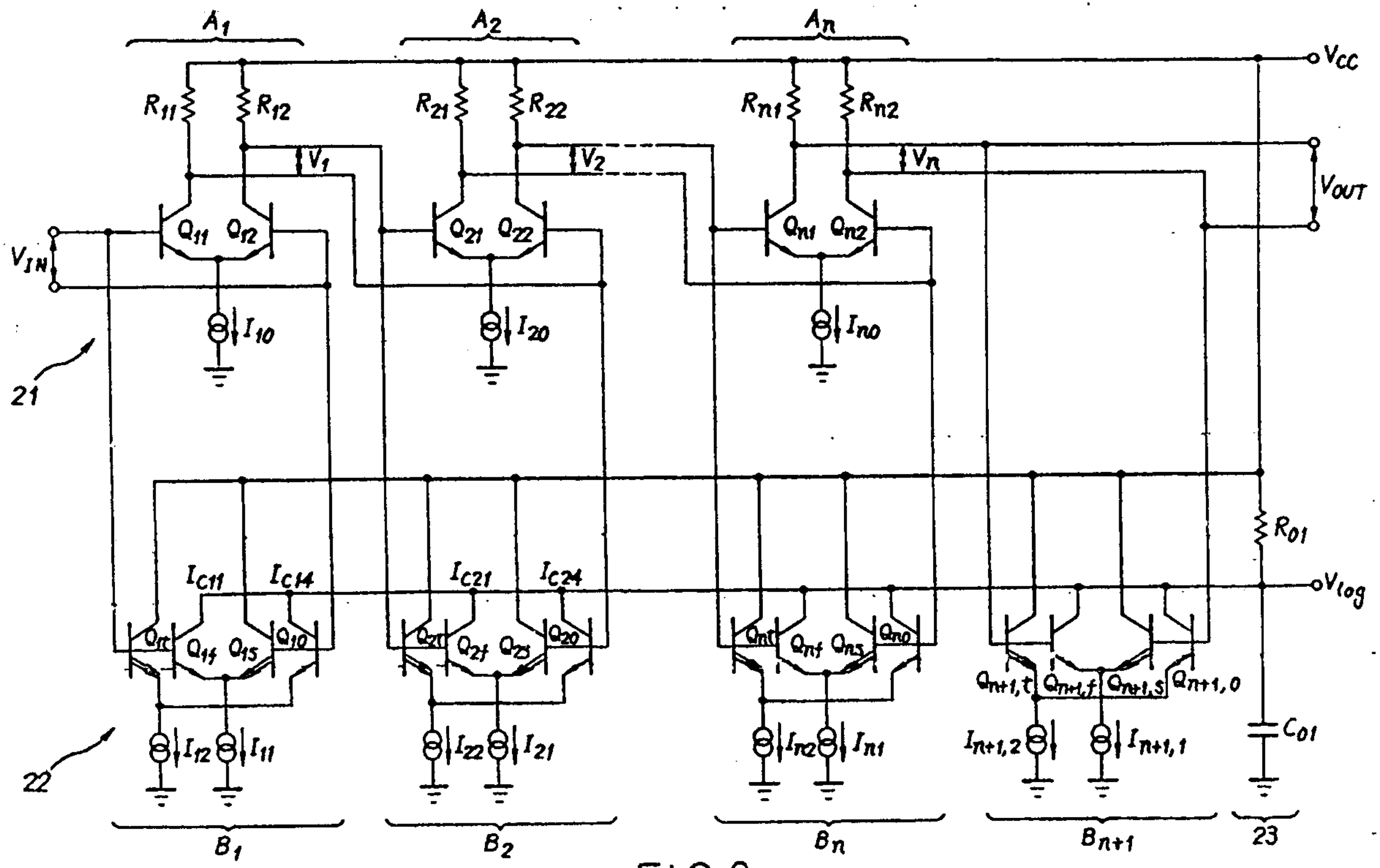
A1
A2
An
VCC
R11
R12
R21
R22
Rn1
Rn2
V1
V2
Vn
VOUT
VIN
Q11
Q12
Q21
Q22
Qn1
Qn2
I10
I20
In0
21
22
IC11
IC14
IC21
IC24
Vlog
R01
Q1t
Q1f
Q15
Q10
Q2t
Q2f
Q25
Q20
Qnt
Qnf
Qns
Qn0
Qn+1,t
Qn+1,f
Qn+1,s
Qn+1,0
I12
I11
I22
I21
In2
In1
In+1,2
In+1,1
C01
B1
B2
Bn
Bn+1
23

FIG.8

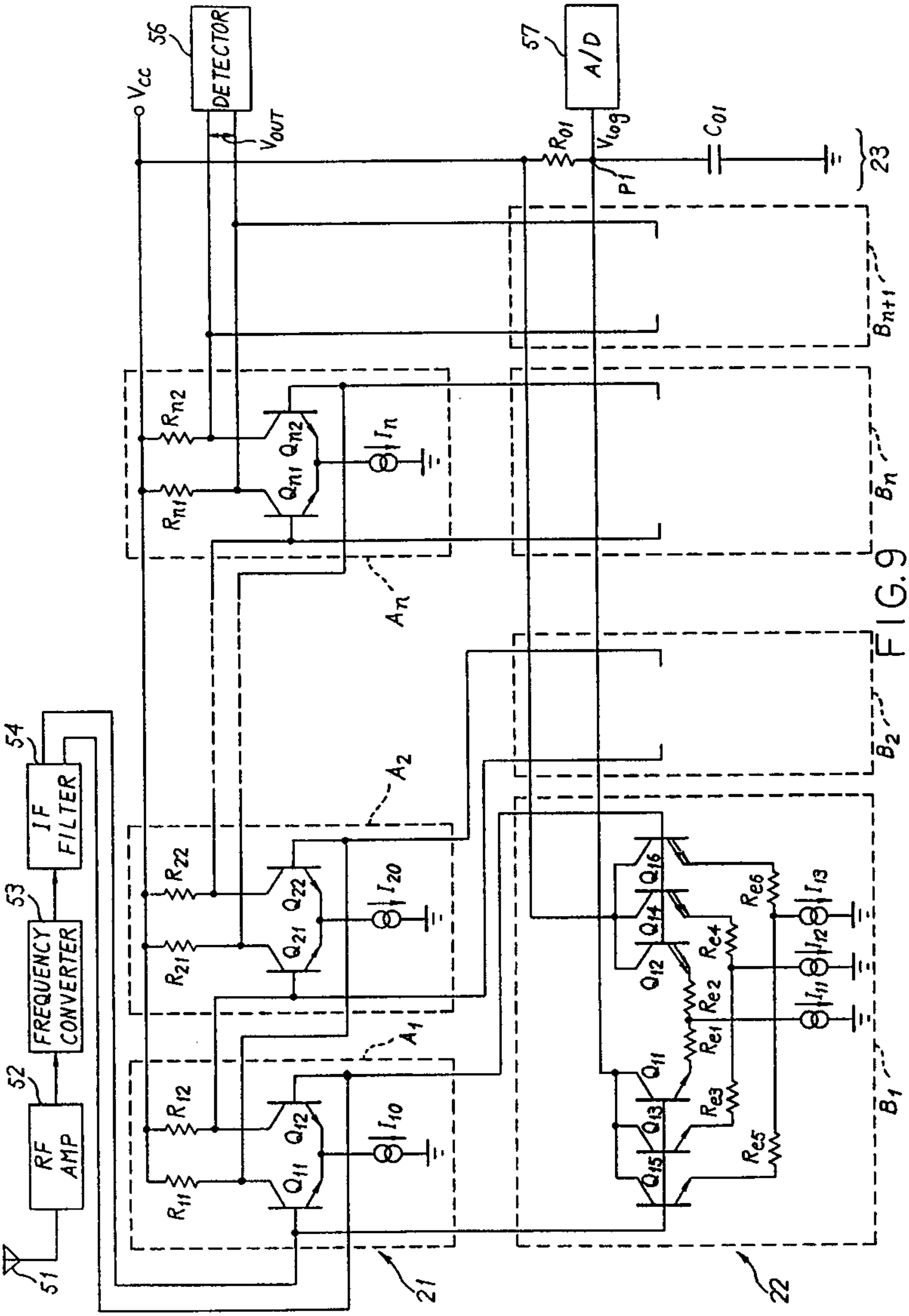
RF AMP
52
FREQUENCY CONVERTER
53
IF FILTER
54
51
DETECTOR
56
Vcc
VOUT
A/D
57
R01
Vlog
P1
C01
23
R11
R12
Q11
Q12
I10
A1
21
R21
R22
Q21
Q22
I20
A2
Rn1
Rn2
Qn1
Qn2
In
An
Q11
Q12
Q13
Q14
Q15
Q16
Re1
Re2
Re3
Re4
Re5
Re6
I11
I12
I13
B1
22
B2
Bn
Bn+1

FIG.9

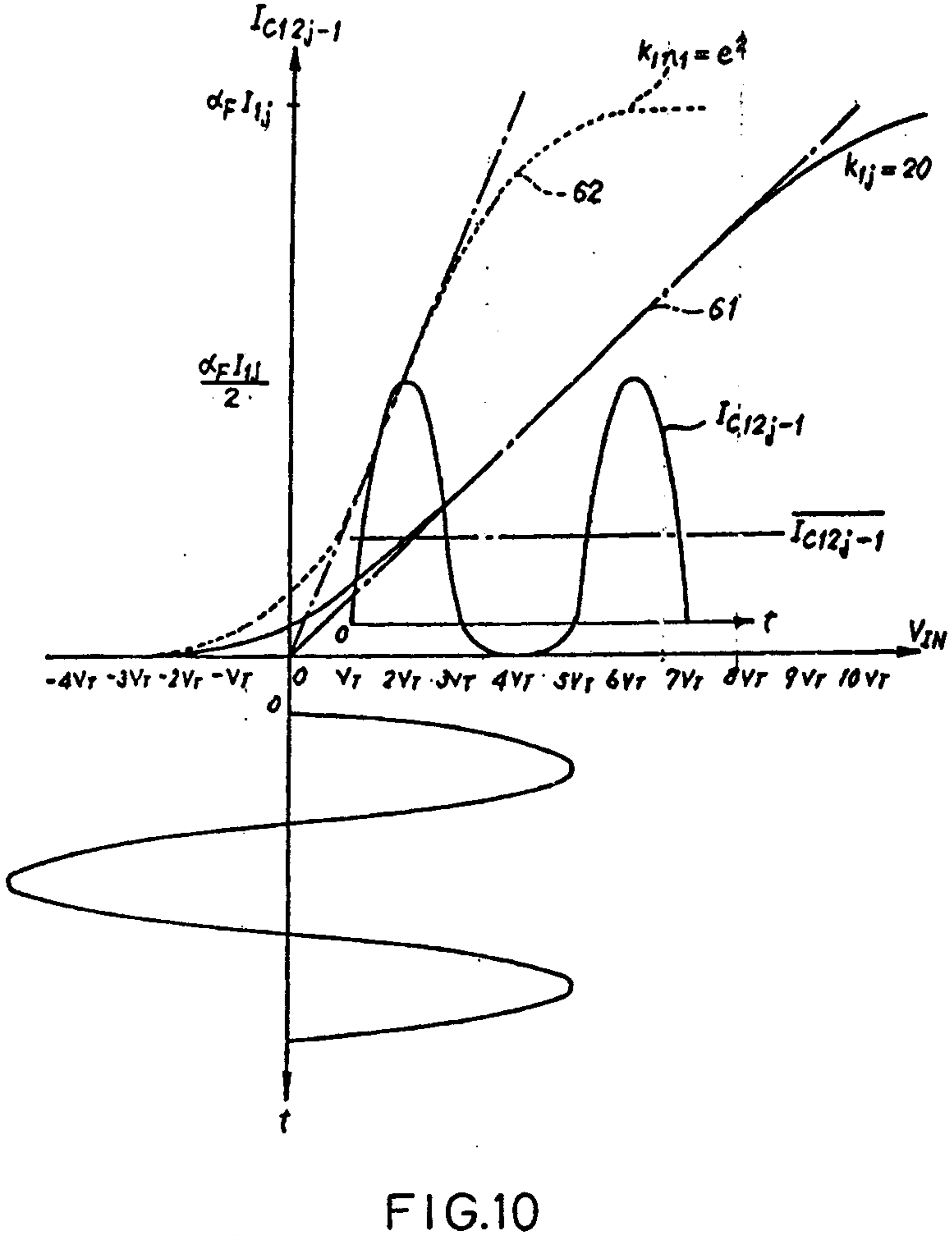
I_{C12j-1}
$\alpha_F I_{1j}$
$\frac{\alpha_F I_{1j}}{2}$
$k_{1}n_{1} = e^4$
62
$k_{1j} = 20$
61
I_{C12j-1}
$\overline{I_{C12j-1}}$
0
t
V_{IN}
$-4V_T$
$-3V_T$
$-2V_T$
$-V_T$
0
V_T
$2V_T$
$3V_T$
$4V_T$
$5V_T$
$6V_T$
$7V_T$
$8V_T$
$9V_T$
$10V_T$
0
t

FIG.10

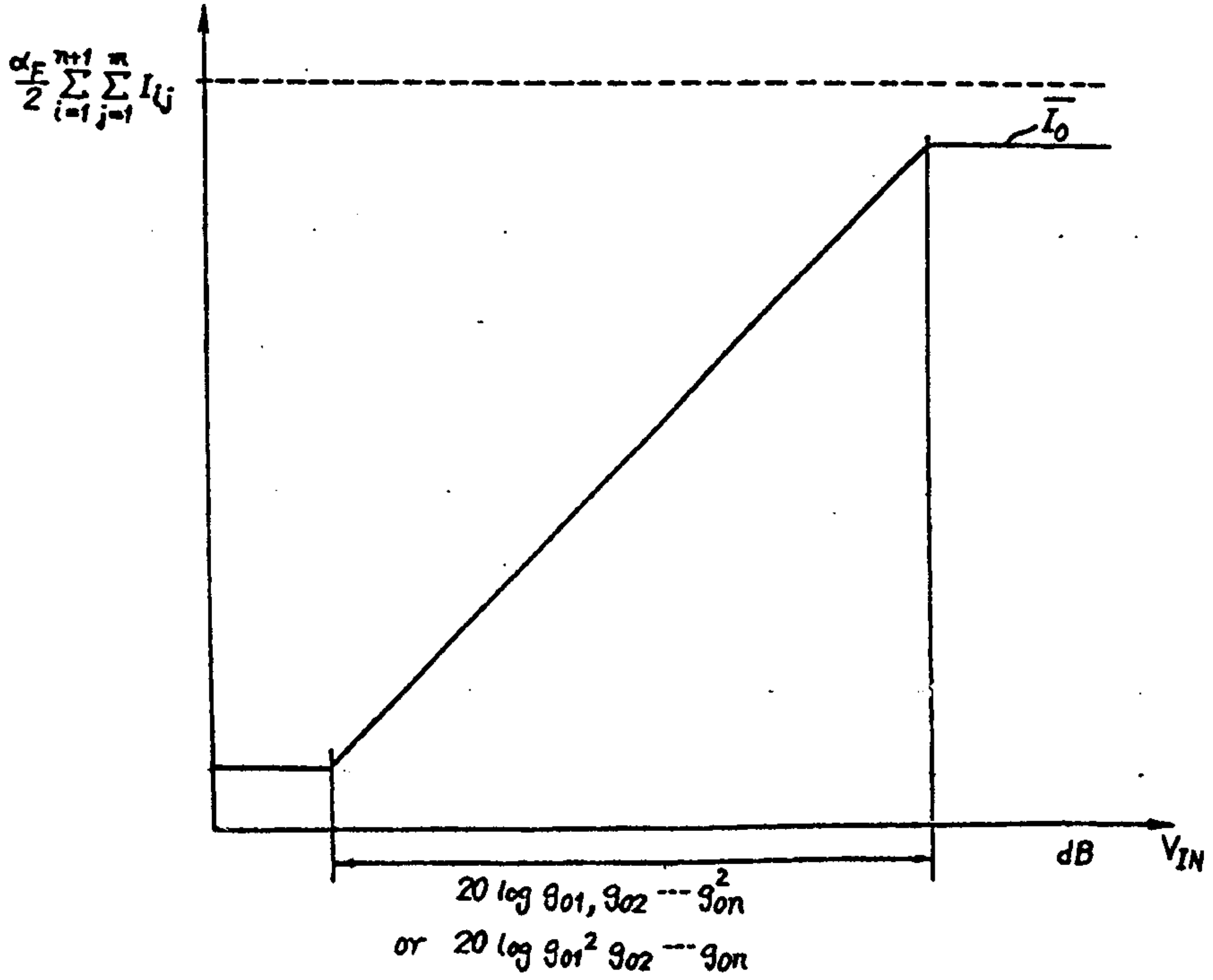
$\frac{\alpha_F}{2}\sum_{i=1}^{n+1}\sum_{j=1}^{m} I_{ij}$
$\overline{I_0}$
dB
V_{IN}
$20 \log g_{01}, g_{02} \cdots g_{0n}^2$
or $20 \log g_{01}^2 g_{02} \cdots g_{0n}$

FIG.11

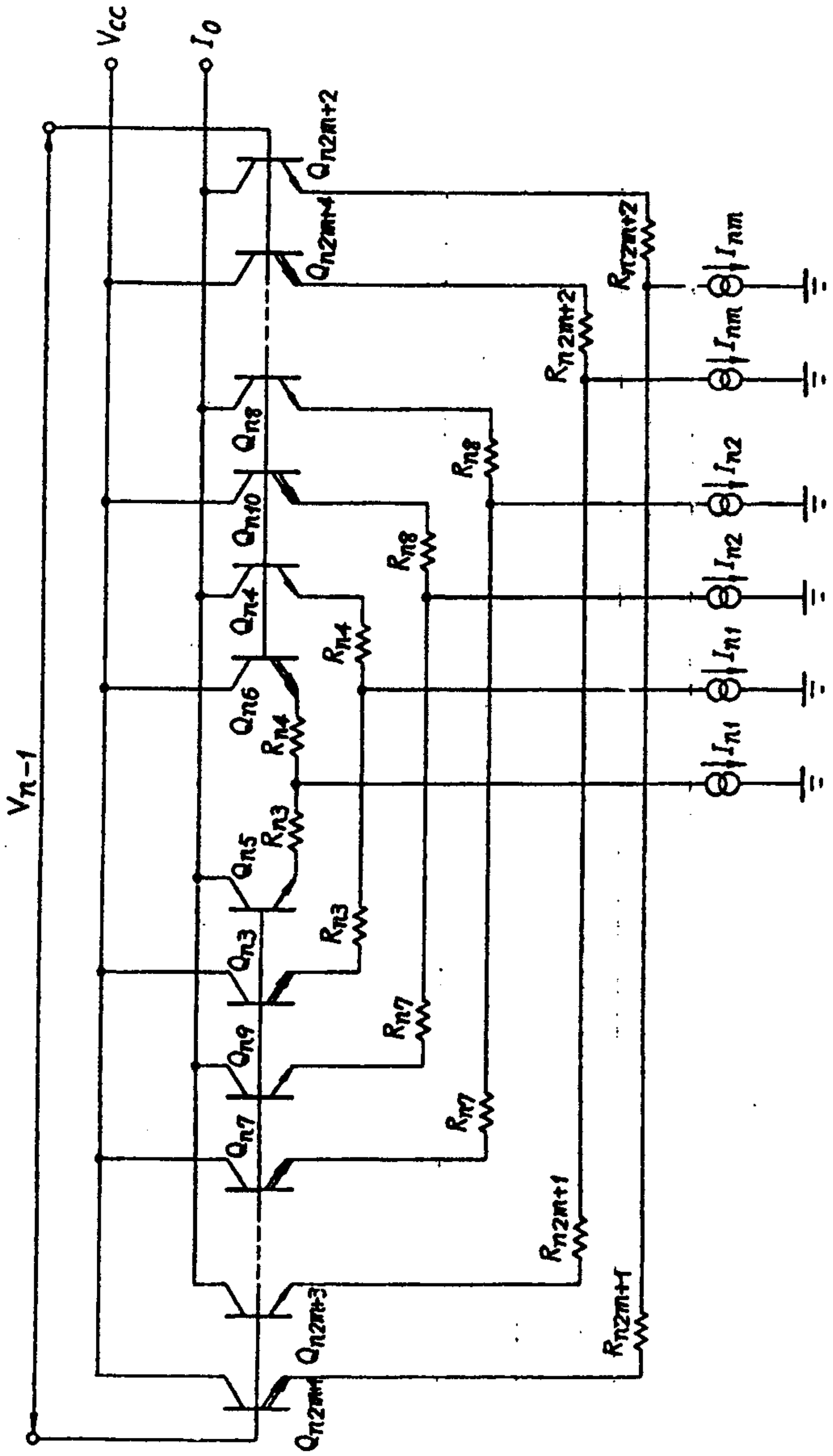
Vcc
Io
Vn-1
Qn2m+2
Qn2m+4
Rn2m+2
Rn2m+2
Inm
Inm
Qn8
Rn8
Qn10
Rn8
In2
In2
Qn4
Rn4
In1
In1
Qn6
Rn4
Qn5
Rn3
Rn3
Qn3
Qn9
Rn7
Qn7
Rn7
Rn2m+1
Rn2m+1
Qn2m+3
Qn2m

FIG.12

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European Application No EP87108099.0 filing date 04.06.1987

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Title INTERMEDIATE FREQUENCY AMPLIFICATION CIRCUIT CAPABLE OF DETECTING A FIELD STRENGTH WITH LOW ELECTRIC POWER

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Classified to
G1U H3Q
G01R H03F H03G

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21.02.1989 EPO: Search report published on 22.02.1989
Entry Type 25.11 Staff ID. Auth ID. EPT

18.12.1992 Notification from EPO of change of Applicant/Proprietor details from
NEC CORPORATION, 33-1, Shiba 5-chome, Minato-ku, Tokyo 108, Japan
[ADP No. 50045780002]
to
NEC CORPORATION, 7-1, Shiba 5-chome Minato-ku, Tokyo 108-01, Japan
[ADP No. 50045780002]
Entry Type 25.14 Staff ID. RD06 Auth ID. EPT

[illegible] noted.

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18.12.1992 Notification from EPO of change of EPO Representative details from
           GLAWE, DELFS, MOLL & PARTNER PATENTANWÄLTE, Postfach 26 01 62
           Liebherrstrasse 20, D-8000 München 26, Federal Republic of Germany
                                                           [ADP No. 50184688001]
           to
           GLAWE, DELFS, MOLL & PARTNER PATENTANWÄLTE, Postfach 26 01 62
           Liebherrstrasse 20, W-8000 München 26, Federal Republic of Germany
                                                           [ADP No. 50184688001]
                               Entry Type 25.14  Staff ID. RD06  Auth ID. EPT

05.01.1993 REDDIE & GROSE, 16 Theobalds Road, London, WC1X 8PL, United Kingdom
                                                           [ADP No. 00000091001]
           registered as address for service
                               Entry Type  8.11  Staff ID. SW2   Auth ID. AA

        **** END OF REGISTER ENTRY ****
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RENEWAL DETAILS

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PROPRIETOR(S)

NEC CORPORATION, 7-1, Shiba 5-chome Minato-ku, Tokyo 108-01, Japan

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YEAR OF LAST RENEWAL	07
STATUS	PATENT IN FORCE