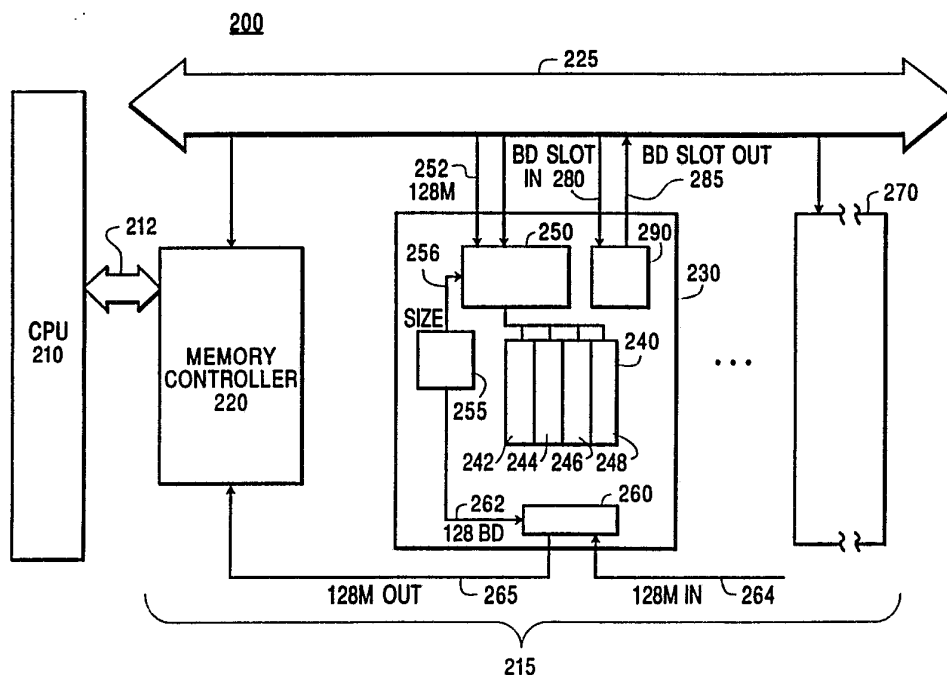


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(54) Title: APPARATUS AND METHODS FOR DISTRIBUTED ADDRESS DECODING AND MEMORY CONFIGURATION



(57) Abstract

In a data processing system, a memory board recognizes the presence of a special condition in the system, such as a 128 MB memory board. In such a situation, the memory board configures itself to map its address space accordingly, such as around a "hole" in the available memory to prevent conflicts between memory space and I/O space. In the absence of the special condition, the memory space will be contiguous. In addition, slot identification signals are passed sequentially to aid the memory boards in determining where their address spaces exist.

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Description

Apparatus and Methods for Distributed Address Decoding and Memory Configuration

Background of the Invention

The present invention relates generally to the field of memory systems and, more particularly, to self-configuring memory systems.

The storage systems of most data processing systems include a memory controller and one or more memory boards. The memory boards, as well as the other boards in the data processing systems, are generally placed in "slots" connected to a backplane. The backplane transfers signals between boards in different slots.

The memory boards include data cells which each have a unique address. The addressable locations for all of the memory boards of a data processing system are called "the memory address space." "I/O address space," on the other hand, identifies the locations which address I/O devices directly.

The memory controllers in this type of data processing system, which generally reside on the same board as the central processing units, decode memory addresses received from a central processing unit to decide which of the memory boards contains the data cells corresponding to the different addresses. Based on its decision, the memory controllers activate appropriate selection signals which the boards containing the addressed data cells use to provide the desired memory access. If the data cells on each board are organized into banks, the selection signals are also used to access the bank containing the addressed data cell.

This type of memory system provides a great amount of flexibility because it can accommodate several different memory configurations. For example, such a memory system can

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usually contain different sizes of memory boards, and eliminate the restriction of certain boards to specified memory board slots.

The use of a memory controller that provides this degree of address signal decoding, however, usually requires a large number of signals to be sent between the memory controller and the memory boards. As the number of memory boards and banks increases, so does the number of memory board and bank select signals.

One problem facing memory system designers is limited signal capacity on backplanes. Although different techniques have been proposed to reduce the number of signals passing between memory boards and memory controllers, the challenge is to reduce the number of signals without losing flexibility.

In addition to the need to accommodate different sizes of memory boards in different slots, flexibility is also needed for other reasons. Sometimes the physical memory address space must be configured in a noncontiguous manner. The memory controller and memory boards must then have sufficient flexibility to provide the configuration needed for the operating system to manage memory resources.

This can be necessary, for example, on certain platforms such as the R3000® computer using the ULTRIX® operating system. ULTRIX operating systems require the usable memory to be mapped to physically contiguous space. The R3000 computer, on the other hand, requires that I/O devices must be accessed through an uncached space resident in the lower 512MB of the memory. This can cause a conflict in systems which large amounts of memory (i.e. approaching 512MB or greater).

Figure 1 shows a diagram 100 of one configuration of physical address space on a R3000/ULTRIX platform. The configuration is designed to ensure the largest block of contiguous address space beginning at location 0. In diagram 100, the lower 256MB portion memory 110 from location 0000 0000 to location 0FFF FFFF is available memory address space.

A second 256MB portion 120 from location 1000 0000 to location 1FFF FFFF is dedicated to uncached I/O. If memory boards with too large of a capacity are used in an R3000/ULTRIX platform having the configuration of Figure 1, it is possible that the memory address space starting at location 0 would overlap the I/O address space.

There is, therefore, a need to provide a memory system which requires a small number of backplane signals for addressing that will allow memory mapping around "holes," such as I/O space, if special conditions exist, such as the use of large capacity boards. There is also a need for such a system to allow contiguous memory address space if the special condition does not exist.

Disclosure of the Invention

To meet these needs, the present invention provides a mechanism for recognizing when a special condition, such as a large capacity board, is present in the system. In such a situation, the memory boards configure their own address space as needed, such as to map around a "hole" in the address space, and thereby prevent any conflicts between memory space and I/O space.

In the preferred embodiment of the invention described below, the problems of 128MB boards in an R3000/ULTRIX environment are addressed in a manner which allows small memories to be contiguous.

Specifically, a memory board of this invention determines its own address space. The memory board is in a data processing system which identifies data cells contained in the memory board according to an address signal capable of assuming a plurality of values. The memory board comprises: size means for generating a size signal identifying the number of the data cells in the memory board; means for receiving a system special condition signal to indicate the presence of a system special condition; and address space determining means, coupled to the size means and to the system special condition signal generating means, for analyzing the system special condition signal to determine

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the values of the address signal which identify the data cells in the memory board.

Additionally, a method of this invention for providing access to data cells in a memory board operating in a data processing system, the data cells corresponding to different values of an address signal, comprises the steps of: generating a size signal identifying the number of the data cells in the memory board; receiving a system special condition signal to indicate the presence of a system special condition; and analyzing the system special condition signal to determine the values of the address signal which identify the data cells on the memory board.

The accompanying drawings, which are incorporated in and which constitutes a part of this specification, illustrate an implementation of the invention and, together with the description, explain the advantages and principles of the invention.

Brief Description of the Drawings

Figure 1 is a diagram of available address space for one configuration of an R3000 computer system.

Figure 2 is a diagram of major components of a preferred implementation of the present invention.

Figure 3A is a table showing the allocation of memory address space when no 128MB boards are present in the preferred implementation.

Figure 3B is a diagram of two examples of memory address space allocation in accordance with the table of Figure 3A.

Figure 4 is a table showing some of the possible configurations of the memory in the preferred implementation in the presence of only 32MB and 64MB memory boards.

Figure 5 is a diagram showing beginning addresses for memory boards in the memory address space if a 128MB memory board is present in the preferred implementation.

Figures 6A - 6E show the different ways in which a 32-bit address should be decoded in the preferred implementation according to the size of the memory and in accordance with

the presence or absence of 128MB memory boards in the memory system.

Figure 7 shows a preferred implementation of a circuit shown in Figure 2 for determining the presence of 128MB memory boards in the preferred implementation of the memory system.

Figure 8 is diagrammatic illustration of the elements in the preferred implementation for decoding addresses on each memory board.

Figure 9 is a diagram of a preferred implementation for a circuit shown in Figure 2 to determine present configuration signals.

Figure 10 is a more detailed block diagram of a memory board shown in Figure 2.

Figure 11 is diagram of a preferred implementation of a memory configuration register in a memory controller shown in Figure 2.

Best Mode for Carrying Out the Invention

Reference will now be made in detail to a preferred implementation of this invention which is illustrated in the accompanying drawings.

Figure 2 is a diagram of a data processing system 200 constructed in accordance with this invention. Data processing system 200 includes a central processing unit ("CPU") 210 which is capable of executing various programs requiring access to memory. To provide such access, CPU 210 sends address and timing signals to a memory controller 220 in a memory system 215 via communication system 212. CPU 210, memory controller 220, and communication system 212 are generally located on the same board.

Memory system 215 includes memory controller 220 and memory boards 230 and 270. In the preferred implementation of this system on a R3000/ULTRIX platform, up to four memory boards may be used, but the practice of the present invention is not constrained to any specific number of memory boards.

Memory controller 220 generates an address signal from the address and timing signals received from CPU 210. Unlike

conventional memory controllers, however, memory controller 220 does not decode the address signals from CPU 210 to form board and bank selection signals. Instead, memory controller 220 sends the generated address signal to memory boards 230 and 270 for those boards to decode.

Data processing system 200 also includes a memory bus or interconnect 225 to transfer addresses and data between memory controller 220 and memory boards 230 through 270. Memory bus 225 not only carries the address signal and data signals, it also carries necessary control signals, some of which are described in detail below. Specific details about the timing of the signals on memory bus 225 will not be discussed because such details are conventional and would be readily apparent to persons skilled in this art.

In the preferred implementation, addresses are transferred between memory controller 220 and memory boards 230 through 270 in a 78-bit path, which consists of dual 39-bit paths. Each 39-bit path includes 32 bits of data and 7 bits of error correction code. The present invention, however, is not dependent on a particular data or address length. For clarity, the following discussion will focus only upon the 32 bits of the address signal rather than the dual path that includes error correction codes.

Memory boards 230 through 270 receive the address signal from memory bus 225. Because memory boards 230 through 270 preferably have the same design, except perhaps for different capacities, only memory board 230 will be described in detail.

Memory board 230 includes a plurality of data cells 240 each corresponding to a different value of the address signal. Preferably, the data locations are organized into banks, usually two or four banks per board, and into rows and columns within each bank. The banks, in turn, are organized into half banks. Other memory board configurations would work as well. Memory board 230 is shown as having four memory banks, 242, 244, 246, and 248.

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In accordance with the present invention, the memory boards determine the values of the address signal which identify the data cells in the corresponding memory board. To understand how the elements in Figure 2 accomplish this, a preferred addressing scheme in accordance with the present invention must be described.

As Figure 1 shows, to obtain the maximum contiguous memory address space beginning with location 0, the unmapped I/O address space in the R3000/ULTRIX platform would occupy locations just below IFFF FFFF, or in this case, locations 1000 0000 - 1FFF FFFF. Locations 0000 0000 - 0FFF FFFF represents a 256MB block of contiguous memory address space. Because the R3000 computer can contain up to four memory boards, the physical memory space can only be guaranteed to fit contiguously into the lower 256MB of memory if each memory board contains no more than $256\text{MB} \div 4$, or 64MB of memory.

Current DRAM technology, however, allows the use of a 128MB memory board. Presumably, future memory boards may be even larger. When a 128MB memory board is used in the preferred implementation, a possibility exists that the combination of a 128MB board with two or three other boards could total more than 256MB of memory. If this occurred, and no accommodation were made for I/O address space, memory address space would overlap I/O address space.

The preferred implementation of the present invention uses a scheme for addressing which checks for the presence of 128MB memory boards. If none exists, i.e., each memory board in memory system 215 has either 64MB or 32MB of memory, memory address space will be contiguous in the lower 256MB (e.g., portion 110 in Figure 1) of memory. This is consistent with conventional addressing techniques.

Figure 3A is a table showing the address space for each slot if there were no 128MB boards in the data processing system 200. The memory address space for the memory board for slot 1 starts at address 0000 0000, and the memory address space for the memory boards in slots 2, 3, and 4

begin at values which are one greater than the largest address for the memory board in the prior slot.

Figure 3B contains two diagrams showing the address space allocation if all the memory boards were either only 32MB or only 64MB boards. As Figure 3B illustrates, even with a memory system having all 64MB boards, the entire memory address space fits contiguously into the lower 256MB of memory.

All combinations of 32MB and 64MB boards can be accommodated in the lower 256MB. Figure 4 is a table 400 showing starting and ending addresses for seven of sixteen possible configurations of 32MB boards and 64MB boards in the four slots. In all configurations, the memory address space is contiguous.

When a 128MB board is present, however, conventional addressing schemes are no longer used because of the possibility of overlap with the I/O address space. In the preferred addressing scheme in accordance with the present invention, the beginning address boundaries for the memory boards are set at the beginning points and mid-points, or effectively the 128MB boundaries, of the first and fourth 256MB portions of memory. This is shown graphically in table 500 in Figure 5. The lower 256MB locations in memory have addresses from 0000 0000 to 0FFF FFFF. The mid-point of that lower 256MB begins at location 0800 0000.

Similarly, the fourth 256MB portion of memory begins at location 3000 0000 and ends at location 3FFF FFFF. The mid-point of this portion begins at location 3800 0000.

With this addressing scheme, memory data is never written into I/O space 120 (Figures 1 and 5), or into locations in the third 256MB block 130 (Figure 7) of the memory map. In addition, because each slot can support 128MB of memory, this implementation could even accommodate a 512MB memory for a data processing system having four slots for memory boards.

The implementation will work because the ULTRIX operating system can be modified to support "holes" in memory

as long as the holes fall on 32MB boundaries and are at least 32MB large. What remains is to ensure that the memory boards similarly support such "holes."

Figures 6A - 6E show the different ways in which the 32-bit address signal is decoded by the preferred implementation of the memory boards to obtain BOARD SELECT and BANK SELECT signals, as well as ROW ADDRESS and COLUMN ADDRESS signals. In all cases, the upper and lower two bits of the address signal are not used, and the third bit (bit 2) is always a half-bank address.

Figure 6A shows the address decoding for a 32MB board if no 128MB boards are present in the memory system 215 of data processing system 200. In this case, the BOARD SELECT signal is drawn from bits 25-29 of the address signal. Bits 28 and 29 are always 0, however, because in the absence of 128MB boards, all the memory boards reside in the lowest 256MB portion of memory.

The BANK SELECT signal is always drawn from bits 23-24 of the address signal because 32MB boards contain four banks of memory in the preferred embodiment. The ROW ADDRESS signals are drawn from bits 13-22 of the address signal, and the COLUMN ADDRESS signals are drawn from bits 3-12 of the address signal. The ROW ADDRESS and COLUMN ADDRESS signals are each ten bits wide because 1Mbit DRAMs are used in the preferred embodiment.

Figure 6B shows how a 64MB board decodes the address signal in the absence of a 128MB board in data processing system 200. The 64MB board uses bits 26-29 of the address signal to determine the BOARD SELECT signal, but bits 29 and 28 are always 0 because this board would reside in the lower 256MB of address space in the absence of a 128MB board. Only bit 25 of the address signal is used to form the BANK SELECT signal because 64MB boards contain just two banks of memory in the preferred embodiment. The ROW ADDRESS signals are drawn from bits 14-22 and bit 24 of the address signal, and the COLUMN ADDRESS signals are drawn from bits 3-12 and bit 23 of the address signal. The COLUMN ADDRESS and ROW ADDRESS

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signals are each eleven bits wide each because 4Mbit DRAMs are used in the preferred embodiment and 10 of the 11 bits of each address are common with those used for 1M bit DRAM, making the address logic simpler.

Figure 6C shows how a 32MB board decodes the 32-bit address signal if a 128MB board is present in data processing system 200. The BOARD SELECT signal is drawn from the same address signal bits 25-29, but bits 25 and 26 are 0 rather than bits 28 and 29. The change reflects the fact that the starting address for these boards will be at 128MB boundaries in the first and fourth 256MB portions of the memory address space. The BANK SELECT signal continues to be drawn from bits 23 and 24 of the address signal.

Figure 6D shows the address decoding for 64MB boards where a 128MB board is present in data processing system 200. The BOARD SELECT is still drawn from bits 26-29 of the address signal, but bit 26 is 0 for the same reason that bits 25-26 are 0 for 32MB boards when 128MB boards are present in data processing system 200. The BANK SELECT signal continues to be drawn from bit 25 of the address signal.

Figure 6E shows the address decoding for a 128MB board. The BOARD SELECT signal is drawn from bits 27-29 of the address signal, and the BANK SELECT signal is drawn from bits 25 and 26. The ROW ADDRESS signal is taken from bits 14-22 and bit 24 of the address signal, and the COLUMN ADDRESS signal is drawn from bits 3-12 and bit 23 of the address signal.

In order to configure the memory system 215 so that the address schemes shown in Figures 6A - 6E will operate correctly, each memory board must know whether the data processing system 200 contains a 128MB board. Accordingly, the memory board of the present invention includes means for receiving a system special condition signal to indicate the presence of a system special condition in the data processing system. In the preferred implementation, the system special condition is the presence of a 128MB board in the memory

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system 215, although this invention could be used to adjust addressing in response to other conditions as well.

In memory board 230 (Figure 2), address circuitry 250 preferably acts as such a receiving means. Address circuitry 250, which in the preferred implementation of memory board 230 also decodes the address signal from memory bus 225 for data cells 240, receives from memory bus 225 a 128M signal 252 indicating the presence of a 128MB memory board in memory system 215.

Memory controller 220 generates the 128M signal 252 from signals received from the memory boards. The memory boards in accordance with this invention also include means for generating a board special condition signal indicating whether the memory board has a board special condition (i.e., is a 128MB board). An example of an element to act as such a means is element 255 shown in memory board 230 (Figure 2). Element 255 generates a 128BD signal 262 if memory board 230 is a 128MB board.

In the preferred embodiment, the memory boards sequentially pass information to each other about the presence or absence of 128MB boards. In general, the memory board of this invention contains means for receiving an input special condition signal which indicates the presence of the board special condition, (e.g., a 128MB board) in selected other boards. Preferably, those selected other boards are located at a greater signal distance from the memory controller 220 along memory bus 225. The input special condition signal is shown as 128Min signal 264 (Figure 2).

The memory board of this invention also includes means for combining the board special condition signal and the input special condition signal to generate a propagating system special condition which indicates whether the memory board or the selected other memory boards have the board special condition. In the preferred implementation of this invention, circuit 260 in Figure 2 acts as such a means. Circuit 260 receives 128BD signal 262 and 128Min signal 264 and generates a propagating system condition signal 128Mout

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265 indicating that a 128MB board is present in the current board or in a board more distant from memory controller 220 along memory bus 225. A pull-up resistor forces the active-low signal 128Min to be inactive (high) in the most distant memory board since no output will be driving this input on that board.

Figure 7 shows a preferred embodiment of circuit 260 as AND gate 760. For ease of understanding, AND gate 760 should be considered as an OR gate with inverted inputs and an inverted output because its inputs and outputs are in active low form.

AND gate 760 receives the 128BD signal at terminal 768, and receives the 128Min signal at terminal 766. AND gate 760 combines those signals to form the 128Mout signal 265 at output terminal 770.

In data processing system 200 (Figure 2), because memory board 230 is nearest to controller 220 along bus 225, memory board 230 transmits the final 128Mout signal to controller 220. This final 128Mout signal indicates whether any of the boards in the entire memory system 215 is a 128MB board. Controller 220 then uses that final 128Mout signal to generate and transmit to all of the memory boards along memory bus 225 the 128M signal 252 indicating whether there is a 128MB board anywhere in memory system 215.

With the knowledge of the existence of a special condition, the memory boards can begin to determine their address space. Other information is needed as well. Thus, in accordance with the present invention, the memory boards have a size means for generating a size signal identifying the number of data cells in the memory board. As embodied herein, the size means is also shown in Figure 2 as circuit element 255 which generate a SIZE signal 256. This circuit is described in greater detail below.

The memory board according to this invention also includes address space determining means, coupled to the size means and to the system special condition signal receiving means, for analyzing the system special condition signal to

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determine the values of the address signal for that board. An example of this address space determining means is the selection circuitry and buffers shown schematically in Figure 8 by system 800, which would reside in element 250 in Figure 2. In Figure 8, the 24-bit address signal 810 (the lower three bits of the 32-bit word are not provided to the memory boards) from the memory bus 225 (Figure 2) provides inputs to a board selection element 820, a bank selection element 830, and a row and column address buffer 840.

Board selection element 820 operates in accordance with the addressing scheme shown in Figure 6A - 6E. If the SIZE signal 256 indicates that the memory board is 32MB, and the 128M signal 252 indicates that there is no 128MB board in memory system 215, then a BOARD SELECT signal 825 is generated from address bits 25-29 of address signal 810 (bits 28 and 29 being 0) and a BDSLOTIN signal, which is described below.

Bank selection element 830, under the same conditions (i.e., a SIZE signal 256 indicating a 32MB board), generates a BANK SELECT signal 835 from bits 23 and 24 of address signal 810. This is consistent with the addressing scheme shown in Figure 6A.

If the 128M signal 252 indicates that there is no 128MB board present in memory system 215 and the SIZE signal 256 indicates that the corresponding memory board is 64MB, then the board selection element 820 examines bits 26-29 (bits 28 and 29 being 0) of the address signal and generates a BOARD SELECT signal 825 based on the BDSLOTIN signal. Bank selection element 830 generates BANK SELECT signal 835 from bit 25 of address signal 810 as shown in Figure 6B.

If, on the other hand, the 128M signal 252 indicates that a 128MB board is present somewhere in the system, then the addressing scheme must change. In this case, for a SIZE signal 256 indicating a 32MB board, the BOARD SELECT signal 825 generated by board select element 280 depends on different values of bits 25-29 of address signal 810 and the

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BDSLOTIN signal. The bank select element 830, however, is unaffected by the state of the 128M signal 252.

If the 128M signal 252 indicates the presence of a 128MB board in memory system 215, and the SIZE signal 256 indicates a 64MB board, then board selection element 820 generates the BOARD SELECT signal 825 according to different values of bits 26-29 of address signal 810 which values are based on the BDSLOTIN signal. Again, the bank selection element 830 is unaffected by this change in signal 128M.

Finally, if the SIZE signal 256 indicates that the current board is a 128MB board, hence insuring that the 128M signal 252 will also indicate the presence of a 128MB board in memory system 215, then board selection element 820 will generate BOARD SELECT signal 825 based on an examination of bits 27-29 of the address signal 810 and the BDSLOTIN signal. Bank selection element 820 will generate the BANK SELECT signal 825 from bits 25 and 26 of memory address 810.

Row and column address buffer 840 is independent of the 128M signal 252 and is only dependent upon the SIZE signal 256 to indicate the number of bits for the row and column addresses. Preferably, the signals into buffer 840 are time-multiplexed over a common set of wires to a common buffer. The design of buffer 840 is conventional.

As system 800 indicates, it is important for the memory boards to receive slot identification signals such as BDSLOTIN. Thus, in accordance with the present invention, a memory board includes means for receiving a prior configuration signal from another memory board in the memory system, and a means for generating a present configuration signal from the prior configuration signal. In memory board 230 of data processing system 200 (Figure 2), a prior configuration signal, BDSLOTIN 280, is received from memory controller 220 via memory bus 225, and the present configuration signal, BDSLOTOUT 285, is sent to another memory board via memory bus 225. BDSLOTIN 280 and BDSLOTOUT 285 are preferably multi-bit signals.

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In Figure 2, element 290 is a circuit element for generating the present configuration signal, based, at least in part, on the prior configuration signal. Figure 9 shows element 290 in greater detail with all of its inputs shown. As Figure 9 indicates, SIZE signal 252 and 128M signal 256 are also used in the preferred implementation to determine the proper present configuration signal from the input configuration signals.

The purpose of the configuration signals is to allow the boards to know their relative positions in the memory system 215 so they can determine their address space. If the 128M signal 252 indicates that a 128MB board is present in memory system 215, then each board generates its present configuration signal, BDSLOTOUT 285, by adding a "1" to the input configuration signal, BDSLOTIN signal 280. These configuration signals allow a board to generate the BOARD SELECT signal under the following conditions:

(BDSLOTIN <2:0> = 0 and ADDR <29:27> = 0) or
(BDSLOTIN <2:0> = 1 and ADDR <29:27> = 1) or
(BDSLOTIN <2:0> = 2 and ADDR <29:27> = 6) or
(BDSLOTIN <2:0> = 3 and ADDR <29:27> = 7).

If the 128M signal 252 indicates that no 128MB board is present anywhere in memory system 215, then the generation of the BDSLOTOUT signal 285 becomes more intricate to insure contiguous memory. For 32MB boards, the BDSLOTOUT signal 285 is set equal to the BDSLOTIN signal 280 plus 1. For 64MB boards, however, the BDSLOTOUT signal 285 is set equal to the BDSLOTIN signal 280 plus 2.

Returning to board selection element 820 in Figure 8, if the memory board's SIZE signal 256 indicates that the board is 32MB, board selection element 820 will generate BOARD SELECT signal 825 if the value of the BDSLOTIN signal 280 is equal to the examined bits (bits 27-25) of the address signal 810, and bits 28 and 29 are 0. If the memory board's SIZE signal 256 indicates that the board is 64MB, then the board selection element 820 will generate BOARD SELECT signal 825 only if the value of BDSLOTIN 280 is equal to the examined

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bits (bits 27-25) of address signal 810 or the value of those bits minus 1, and bits 29 and 28 are 0.

As is apparent, the present invention greatly reduces the number of backplane signals necessary for board selection. In the preferred embodiment, only twelve signals need to be transmitted over the backplane to achieve bank and board decoding. These signals include seven lines, bits 29-23, of address signal 810, three board slot identification lines (BDSLOTIN 280/BDSLOTOUT 285 are three bits), and the two additional lines 128M signal 252 and the 128Min/128Mout signals (264/265). In addition, the implementation in accordance with the present invention allows the simultaneous decoding of the board select and bank select signals in a single layer of logic, which minimizes selection time.

Figure 10 shows the preferred implementation of a memory board 1000 (which can be boards 230 or 270 or another board in accordance with this invention) as used with a standard Q-bus backplane. Because the Q-bus backplane has a fixed number of connectors, the compatibility of memory system 215 with the Q-bus backplane depends on the ability to operate with the number of connectors in the CD INTERCONNECT portion of the Q-bus, which is part of memory bus 225.

As shown in Figure 10, there are four banks divided into four high half-banks 1001-1004 and four low half-banks 1005-1008. This division into high and low bank pairs merely reflects the implementation of the dual 39-bit transfers and is by no means a requirement of the present invention.

Memory half-banks 1001-1008 each respond to address signals ADDR<10:0> 1011, write enable signal WE 1012, column address strobe signals CASH 1013 and CASL 1014, and row address strobe signal RAS 1015. The eleven address signals ADDR<10:0> 1011 represent twenty-two inputs to the row and column buffer 840 in Figure 8 multiplexed onto eleven address lines.

The CASH 1013 and CASL 1014 signals are buffered by buffer 1009 and are generated from column address strobe signals CASH 1023 and CASL 1024, respectively, received from

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the CD INTERCONNECT portion of memory bus 225 (Figure 2). Prior to buffering, these signals are conditioned by element 1016.

The write enable signal WE 1012 is buffered via buffer 1017 from a write enable signal WE 1022 received from the CD INTERCONNECT portion of bus 225, and are also signal conditioned by element 1016. The board write enable signal BDWE 1015 activate drivers 1060 and 1065, respectively, to drive the DATA HI 1018 and DATA LO 1019 signals from the data cable portion 1090 of memory bus 225 to the BD DATA HI 1028 and BD DATA LO 1029 signals, respectively. BD DATA HI signal 1028 and BD DATA LO signal 1029 are the data signals into and out of half banks 1001-1008, respectively.

If data is being read from the memory half banks 1001-1008, that data is buffered via registers 1061 and 1066 for BD DATA HI signals 1028 and BD DATA LO signals 1029, respectively. Registers 1061 and 1066 are controlled by a BD CLK signal 1041, which is received via signal conditioning element 1016 from a CLK signal 1031 on the CD INTERCONNECT portion of memory bus 225, and a RD EN signal 1033 generated from OR gate 1070. OR GATE 1070 has as inputs a BOARD SELECT signal 825 and a BOE signal 1044 which is a signal-conditioned version, via signal conditioning element 1016, of BOE signal 1034 on the CD INTERCONNECT portion of bus 225.

The presence of a 128MB board in memory board 1000 or the other boards more distant from memory controller 220 along bus 225, is determined using OR gate 1020, which is preferably in a PAL array used to generate other signals shown in Figure 10. OR gate 1020 is functionally the same as the AND gate 760 shown in Figure 7.

Gate 1020 receives a 128Min signal 264 from the CD INTERCONNECT portion of memory bus 225. The 128Min signal 264 is preferably pulled up to 5 volts via a resistor 1026. OR gate 1020 also receives as an input a 128BD signal 262 generated on memory board 1000 to indicate whether memory board 1000 is 128MB. The output of gate 1020 is the 128Mout signal 265 which is sent to the CD INTERCONNECT portion of

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memory bus 225 for transmission either to another board or to memory controller 220.

PAL circuit 1030, like circuit 290 in Figure 9, generates the BDSLOTOUT signal 285. It receives as inputs the BDSLOTIN signal 280 from either the memory controller 220 or from another memory board. Circuit 1030 also receives the 128M signal 252 indicating the presence in the system of a 128MB board anywhere in memory system 215. In addition circuit 1030 receives the 128BD signal 262, and a HALFPOP signal 1035 indicating whether memory board 1000 has 2 or 4 banks of memory. The HALFPOP signal 1035 is similar to the SIZE signal 256 shown in the other figures.

Circuit elements 1040 and 1045 together generate the BOARD SELECT signal 825 and other timing signals. Circuit element 1040 receives from the CD INTERCONNECT portion of bus 225 a RAS CLK clock signal 1051, as well as bits 23-29 of the memory address BRADR 1052 which have been latched by memory controller 220. Circuit element 1040 creates from those inputs a BD RAS TIME signal 1043 and a buffered BDADR signal 1042 containing bits 23-29 of the address signal which is to be used for decoding.

Bits 29-25 of BDADR signal 1042, as well as the 128M signal 252 and BDSLOTIN signal 280, also received from the CD interconnect portion of bus 225, are inputs to PAL element 1045. PAL element 1045 generates the 128BD signal 262 as well as the HALFPOP signal 1035 for use elsewhere on board 1000. In addition to HALFPOP signal 1035 and 128BD signal 262, PAL element 1045 generates the BOARD SELECT signal 825, preferably according to the explanation given above for the operation of board select element 820.

PAL element 1045 also generates CASE-SEL signals 1049 which are used to help determine which BANK SELECT signals should be activated according to the size (i.e., the number of banks) of board 1000.

PAL element 1050 generates the BANK SELECT signal 835 (see Figure 8). In memory board 1000, BANK SELECT signal 835 is a four-bit signal to reflect the four possible banks on

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memory board 1000. PAL element 1050 generates BANK SELECT signal 835 from the 128BD signal 262, the HALFPOP signal 1035, the 128Min signal 264, the 128M signal 252, and bits 23-26 of the BDADR signal 1042. BANK SELECT signal 835 is provided as an input to PAL element 1055, along with the CASE-SEL signals 1049.

From BANK SELECT signal 835 and the CASE-SEL signals 1045, PAL element 1055 generates RAS EN <3:0> signals 1051 which are provided as an input to gate 1058. Gate 1058 also receives the BD RAS TIME signal 1043 from buffer 1040, and generates the RAS 0 - RAS 3 signals 1091 - 1094. RAS 0 signal 1091 is sent to half banks 1001 and 1005, RAS 1 signal 1092 is sent to half banks 1002 and 1006, RAS 2 signal 1093 is sent to half banks 1003 and 1007, and RAS 3 signal 1094 is sent to half banks 1004 and 1008.

BOARD SELECT signal 825 is an input to inverter 1080, whose output is the NXM signal 1081. NXM signal 1081 indicates the presence or absence of memory for the corresponding board. If the memory board is present, and BOARD SELECT signal 825 is active, then NXM signal 1081 indicates that memory is present. If there is no address match, then NXM signal 1081 remains deactivated, and CPU 210 is advised that there is no memory for the corresponding address.

The NXM signals can thus be used for initial memory configuration to determine where memory is and is not present. In this way CPU 210, during initialization procedures, can send out addresses and, based on the NXM signals' response, construct a memory map for the entire memory system 215. CPU 210 must construct such a map to formulate the proper addresses.

As indicated above, many operating systems, such as the ULTRIX operating system, can be adapted to perform with a noncontiguous memory. The operating systems need to know where the holes are, however. The additional overhead from such mapping need be negligible, because the mapping can occur as part of the memory diagnostics.

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In addition to the signals described above, a REFRESH signal 1099 is received from the CD INTERCONNECT portion of memory bus 225 and is shown as connected to PAL elements 1045, 1050 and 1055. The purpose of REFRESH signal 1099 is to indicate that the refresh cycle is taking place on memory bus 225. PALS 1045, 1050, and 1055 use the REFRESH signal as an override to enable all the banks which need to be refreshed. REFRESH signal 1099 is generated from memory controller 220 in the preferred embodiment.

To complete the explanation of the preferred implementation of this invention, some mention will be made of a portion of memory controller 220 (Figure 2). Figure 11 shows a memory configuration register 1100, which preferably resides inside memory controller 220. Configuration register 1100, under the control of logic 1190, is used to manage certain of the functions of signals in memory system 215.

Bit 1110 of register 1100 is a 128M register signal which CPU 210 can set to force the 128M signal 252 (Figures 2 and 10) to its active state even if the 128Mout signal is inactive. Normally, memory controller 220 merely transmits the 128Mout signal 265 to CPU 210 which then gates the signal back to memory controller 220. Memory controller 220 then transmits that gated signal as 128M signal 252. By forcing memory controller 220 to override the gated signal, CPU 210 can test whether the memory boards would respond correctly to different memory configurations.

Memory configuration register 1100 also preferably includes a diagnostic bit 1120 which is used to perform ECC checks on the memory. Finally, board select bits 1130 are used to generate the initial BDSLOTIN signal 280 sent to the memory board, such as board 230, which has the shortest signal distance along bus 225 from memory controller 220. Board select bits 1130 are normally all zeros, however, the CPU 210 can also set these bits to various different values to allow the CPU to check different memory configurations during diagnostics.

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As the preceding description explains, the present invention reduces the number of control signals needed for memory configuration and addressing, and allows the memory to reconfigure itself around "holes" created by special circumstances, such as the R3000/ULTRIX platform with large memory boards. This invention also allows small memory configurations (less than 256MB) to be contiguous so that they can be supported by the existing ULTRIX operating system.

The present invention also reduces the amount of time required to select portions of memory, which makes the memory subsystems faster, and allows use of a single memory board to test the entire memory address space completely. Persons of ordinary skill in the art will recognize that various modifications and variations may be made in this invention without departing from the spirit and scope of the general inventive concept. This invention in its broader aspects is therefore not limited to the specific details or representative methods shown and described.

Claims

1. A memory board for determining its own address space in a data processing system which identifies data cells contained in the memory board according to an address signal capable of assuming a plurality of values, the memory board comprising:

size means for generating a size signal identifying the number of the data cells in the memory board;

means for receiving a system special condition signal to indicate the presence of a system special condition; and

address space determining means, coupled to the size means and to the system special condition signal generating means, for analyzing the system special condition signal to determine the values of the address signal which identify the data cells in the memory board.

2. The memory board of claim 1 wherein the size means includes

means for generating a board special condition signal indicating whether the memory board has a board special condition.

3. The memory board of claim 2 further including means for receiving an input special condition signal indicating the presence of the board special condition in selected other memory boards in the data processing system; and

means, coupled to the board special condition signal generating means and to the input special condition signal receiving means, for combining the board special condition signal and the input special condition signal to generate a propagating system special condition signal indicating whether the memory board or any of the selected other memory boards in the data processing system has the board special condition.

4. The memory board of claim 2 wherein the means for generating the board special condition signal includes

large capacity board means for generating the board special condition signal to indicate whether the memory board contains a predetermined number of the data cells.

5. The memory board of claim 4 further including large capacity receiving means for receiving an input system special condition signal indicating the presence of selected other memory boards in the data processing system having the predetermined number of the data cells; and

means, coupled to the large capacity board means and to the large capacity receiving means, for combining the board special condition signal and the input system special condition signal to generate a propagating system special condition signal to indicate whether the memory board or any of the selected other memory boards in the data processing system has the predetermined number of the data cells.

6. The memory board of claim 1 wherein the address space determining means includes

means for receiving an input configuration signal; and

means, coupled to the size means and to the input configuration signal receiving means, for generating a present configuration signal.

7. The memory board of claim 1 wherein the address space determining means includes

board selection means for determining when the memory board contains data cells corresponding to the values of the address signal.

8. The memory board of claim 7 wherein the board selection means is coupled to the size means and includes

means for examining the size signal to determine when the memory board contains data cells corresponding to the values of the address signal.

9. The memory board of claim 7 wherein the address space determining means includes

means for receiving an input configuration signal, and

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wherein the board selection means includes

means for examining the input configuration signal to determine when the memory board contains data cells corresponding to the values of the address signal.

10. The memory board of claim 7 wherein the data cells in the memory board are organized into banks, and

wherein the address space determining means further includes

bank selection means, coupled to the size means, for selecting the one of the memory banks on the memory board which contains the cells corresponding to the values of the address signal.

11. The memory board of claim 10, wherein the bank selection means includes

means for selecting the one of the memory banks according to an input special condition signal indicating the presence of a board special condition in selected other memory boards in the data processing system.

12. The memory board of claim 7 or 10 further including cell selection means for determining, from a row selection portion and a column selection portion of the address signal, the cells corresponding to the values of the address signal.

13. A memory system for use with a data processing system, the memory system comprising:

a memory controller for receiving address and timing signals from the data processing system and for generating an address signal capable of assuming a plurality of values;

an interconnect, coupled to the memory controller, for transmitting the address signal; and

memory boards, coupled to the interconnect to receive the address signal, each of the memory boards including

size means for generating a size signal identifying the number of the data cells in the memory board;

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means for receiving a system special condition signal to indicate the presence of a system special condition; and

address space determining means, coupled to the size means and to the system special condition signal generating means, for analyzing the system special condition signal to determine the values of the address signal which identify the data cells in the corresponding memory board.

14. The memory system of claim 13 wherein the memory controller includes

means for storing a system special condition signal; and

means for sending the system special condition signal to the memory boards.

15. The memory system of claim 13 wherein the size means includes

means for generating a board special condition signal indicating whether the memory board has a board special condition.

16. The memory system of claim 15 wherein at least one of the memory boards includes

means for receiving an input special condition signal indicating the presence of the board special condition in selected other ones of the memory boards; and

means, coupled to the board special condition signal generating means and to the input special condition signal receiving means, for combining the board special condition signal and the input special condition signal to generate a propagating system special condition signal indicating whether the at least one memory board or any of the selected other memory boards has the board special condition.

17. The memory system of claim 16 wherein the means for generating the board special condition signal includes

large capacity board means for generating the board special condition signal to indicate whether the

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at least one memory board contains a predetermined number of data cells;

wherein the input system special condition signal indicates the presence of at least one of the selected other memory boards having the predetermined number of data cells; and

wherein the condition means includes

means for combining the board special condition signal and the input special condition signal to generate the propagating system special condition signal to indicate whether the at least one memory board or any of the selected other memory boards has the predetermined number of data cells.

18. The memory system of claim 16 wherein the memory controller includes

means for storing the propagating system special condition signal received from a selected one of the memory boards as the system special condition signal.

19. The memory system of claim 16 wherein the means in the at least one memory board for generating the board special condition signal includes

means for indicating whether that memory board contains a predetermined number of the data cells.

20. The memory system of claim 13 wherein the address space determining means in at least one of the memory boards also includes

means for receiving an input configuration signal; and

means, coupled to the size means and to the input configuration means of that board, for generating a present configuration signal.

21. The memory system of claim 20 wherein the address space determining means includes

means for analyzing the input configuration signal to determine the values of the address signal which identify the data cells in the at least one memory board.

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22. The memory system of claim 13 wherein the memory boards are arranged in order of increasing signal distance along the interconnect from the memory controller, and wherein at least one of the memory boards includes means, connected to the interconnect, for receiving an input slot signal from the one of the memory boards immediately closer to the memory controller in terms of signal distance along the interconnect, and

means, coupled to the size means and to the input slot signal receiving means, for forming an output board slot signal for transmission along the interconnect.

23. The memory system of claim 22 wherein the address space determining means include

means for analyzing the input board slot signal to determine the values of the address signal which identify the data cells in the at least one memory board.

24. The memory system of claim 22 wherein the memory controller includes

means for transmitting an initial slot signal for transfer to the one of the memory boards having the smallest signal distance to the memory controller along the interconnect.

25. The memory system of claim 13 wherein the address space determining means in at least one of the memory boards includes

board selection means, coupled to the size means, for determining when the at least one memory board contains data cells corresponding to the values of the address signal.

26. The memory system of claim 25 wherein the board selection means in the at least one memory board is coupled to the size means and includes

means for examining the size signal to determine when the memory board contains data cells corresponding to the values of the address signal.

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27. The memory system of claim 25 wherein the address space determining means in at least one of the memory boards includes

means for receiving an input configuration signal, and

wherein the board selection means in each of the memory boards includes

means for examining the input configuration signal to determine when the at least one memory board contains data cells corresponding to the values of the address signal.

28. The memory system of claim 25 wherein the data cells in the at least one memory board are organized into banks, and

wherein the address space determining means in each of the at least one memory board further includes

bank selection means, coupled to the size means, for selecting the one of the memory banks on the at least one memory boards which contains the cells corresponding to the values of the address signal.

29. The memory system of claim 28 wherein the bank selection means includes

means, coupled to the board selection means, for activating the bank selection means when the board selection means determines that the at least one memory board contains data cells corresponding to the address signal.

30. The memory system of claim 26 or 29 wherein the at least one memory board also includes

cell selection means for determining from a row selection portion and a column selection portion of the address signal the cells corresponding to the values of the address signal.

31. A data processing system including

a central processing unit generating address and timing signals; and

a memory system for providing storage of data for the central processing unit, the memory system including

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a memory controller for receiving address and timing signals from the data processing system and for generating an address signal capable of assuming a plurality of values;

an interconnect, coupled to the memory controller, for transmitting the address signal; and
memory boards, coupled to the interconnect to receive the address signal, each of the memory boards including

size means for generating a size signal identifying the number of the data cells in the memory board;

means for receiving a system special condition signal to indicate the presence of a system special condition; and

address space determining means, coupled to the size means and to the system special condition signal generating means, for analyzing the system special condition signal to determine the values of the address signal which identify the data cells in the corresponding memory board.

32. The data processing system of claim 31 wherein the size means further includes

means for generating a board special condition signal indicating whether the memory board has a board special condition.

33. The data processing system of claim 32 wherein at least one of the memory boards also includes

means for receiving an input special condition signal indicating the presence of the board special condition in selected other memory boards in the data processing system; and

means, coupled to the board special condition signal generating means and to the input special condition signal receiving means, for combining the board special condition signal and the input special condition signal to generate a propagating system special condition signal

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indicating whether the at least one memory board or any of the selected other memory boards in the memory system has the special condition.

34. The data processing system of claim 31 wherein the central processing unit includes

means for generating an initial configuration signal;

wherein the memory controller includes

means for transmitting the initial configuration signal to one of the memory boards;

and wherein each of the memory boards includes means for receiving an input board signal from the initial configuration signal of the memory controller or from an output board signal from another one of the memory boards, and

output means, coupled to the receiving means and the size means, for generating an output board signal for use as one of the input board signals by another one of the memory boards.

35. The data processing system of claim 34 wherein the address determining means in each of the memory boards includes

means for analyzing the input board signal to determine the values of the address signal which identify the cells in the corresponding memory board.

36. The data processing system of claim 35 wherein the central processing unit includes

test means, coupled to the initial configuration transmitting means, for setting the initial configuration signal at selected values.

37. The data processing system of claim 34 wherein the central processing system also includes

test means for setting the system special condition signal at a selected value.

38. The data processing system of claim 31 wherein the central processing unit includes

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means for determining the configuration of the memory boards by testing for the values of the address signals that identify data cells in each of the memory boards, the configuration determining means including

means for transmitting to the memory system selected values of the address signal; and

means for determining whether any of the memory boards in the memory system has data cells identified for the selected signals.

39. In a memory board operating in a data processing system, the memory board containing a plurality of data cells which correspond to different values of an address signal, a method for providing access to the data cells comprising the steps of

generating a size signal identifying the number of the data cells in the memory board;

receiving a system special condition signal to indicate the presence of a system special condition; and

analyzing the system special condition signal to determine the values of the address signal which identify the data cells on the memory board.

40. The method of claim 39 further including the step of

generating a board special condition signal indicating whether the memory board has a board special condition.

41. The method of claim 40 further including the steps of

receiving an input special condition signal indicating the presence of the board special condition in selected other memory boards in the data processing system; and

combining the board special condition signal and the input special condition signal to generate a propagating system special condition signal indicating whether the memory board or any of the selected memory boards in the data processing system has the board special condition.

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42. The method of claim 40 wherein the step of generating the board special condition signal includes the substep of

generating the board special condition signal to indicate whether the memory board has a predetermined number of data cells.

43. The method of claim 42 further including the steps of

receiving an input system special condition signal indicating the presence of other memory boards in the data processing system having the predetermined number of data cells,

combining the special condition signal and the input system special condition signal to generate a propagating system special condition signal to indicate whether the memory board or any of the selected memory boards in the data processing means has the predetermined number of the data cells.

44. The method of claim 39 further including the step of

receiving an input configuration signal, and
generating a present configuration signal from the prior memory signal and the size signal.

45. The method of claim 39 wherein the step of analyzing the system special condition signal includes the step of

determining when the memory board contains data cells corresponding to the values of the address signal.

46. The method of claim 45 wherein the step of analyzing the system special condition signal includes the substep of

examining the size signal to determine when the memory board contains data cells corresponding to the values of the address signal.

47. The method of claim 46 wherein the step of analyzing the system special condition signal includes the substep of

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receiving an input configuration signal, and
wherein the step of determining when the memory board contains data cells corresponding to the values of the address signal includes the substep of

examining the input configuration signal to determine when the memory board contains data cells corresponding to the values of the address signal.

48. The method of claim 45 wherein the data cells in the memory board are organized into banks, and

wherein the step of analyzing the system special signal further includes the substep of

selecting the one of the memory banks on the memory board which contains the cells corresponding to the values of the address signal.

49. The method of claim 48 wherein the step of selecting the one of the memory banks on the memory board which contains the cells corresponding to the values of the address signal includes the substep of

activating the bank selection means when the board selection means determines that the memory board contains data cells corresponding to the address signal.

50. The method of claim 45 or 48 further including the step of

determining, from a row selection portion and a column selection portion of the address signal, the cells corresponding to the values of the address signal.

51. In a memory system of a data processing system, the memory system including memory boards containing a plurality of data cells which correspond to different values of an address signal, a method for providing access to the data cells comprising the steps of

receiving, in a memory controller of the memory system, address and timing signals from the data processing system;

generating, in the memory controller, an address signal capable of assuming a plurality of values;

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generating, in the memory boards, a size signal identifying the number of the data cells in the memory board;

receiving, in the memory boards, a system special condition signal to indicate the presence of a system special condition; and

analyzing, in the memory boards, the system special condition signal to determine the values of the address signal which identify the data cells on the corresponding memory board.

52. The method of 51 further comprising the steps of storing, in the memory controller, the system special condition signal; and

sending the system special condition signal from the memory controller to the memory boards.

53. The method of claim 51 wherein the memory boards are arranged in order of increasing signal distance along the interconnect from the memory controller,

and wherein the method includes the steps, executed by the memory boards of

receiving an input slot signal from the one of the memory boards located closest to the memory controller in terms of signal distance; and

forming an output board slot signal.

54. The method of claim 53 wherein the step of analyzing the system special condition signal includes the substep of

analyzing the output board slot signal to determine the values of the address signal which identify the data cells on the corresponding memory board.

55. The memory system of claim 54 further including the step of

generating, in the memory controller, an initial slot signal for transfer to the one of the memory boards having the smallest signal distance from the memory controller.

56. In a data processing system including memory boards containing a plurality of data cells which correspond to

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different values of an address signal, a method for providing access to the data cells comprising the steps of

generating address and timing signals in a central processing unit;

receiving, by a memory controller, the address and timing signals generated by the central processing unit;

generating, by the memory controller, an address signal capable of assuming a plurality of values;

generating, in the memory boards, a size signal identifying the number of the data cells in the memory board;

receiving, in the memory boards, a system special condition signal to indicate the presence of a system special condition; and

analyzing, in the memory boards, the system special condition signal to determine the values of the address signal which identify the data cells on the memory board.

57. The method of claim 56 further including the steps of

transmitting an initial address signal from the memory controller to one of the memory boards;

receiving, by the memory boards, an input board signal from the initial address signal of the memory controller or from an output board signal from another one of the memory boards; and

generating, by the memory boards, an output board signal for use as one of the input board signals by another one of the memory boards.

58. The method of claim 57 wherein the step of analyzing the system special condition signal includes the substep of

analyzing the input board signal to determine the values of the address signal which identify the cells in the corresponding memory board.

59. The method of claim 58 further including the step of

setting the initial address signal at selected values.

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60. The method of claim 59 further including the step of

determining the configuration of the memory boards by testing for the values of the address signals that identify data cells in each of the memory boards.

61. The method of claim 60 wherein the determining step includes the substeps of

transmitting selected values of the address signals; and

determining whether any of the memory boards has data cells identified for the selected signals.

62. A memory board for determining its own address space which maps around holes when it is not possible to obtain a contiguous address space in a data processing system which identifies data cells contained in the memory board according to an address signal capable of assuming a plurality of values, the memory board comprising:

size means for generating a size signal specifying whether the memory board contains 32MB or 64MB data cells and for generating a board special condition signal indicating whether the memory board has 128MB data cells;

means for receiving a system special condition signal to indicate the presence of any memory boards in the data processing system containing 128MB data cells;

means for receiving an input slot identification signal indicating a slot position for the memory board in the data processing system;

means, coupled to the size means, for generating an output slot identification signal from the input slot identification signal and the size signal;

address space determining means, coupled to the size means, to the system special condition signal generating means, and to the input slot identification signal receiving means, for analyzing the size signal, the system special condition signal, and the input slot identification signal to determine the values of the address signal which identify the data cells in the memory board;

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means for receiving an input special condition signal indicating the presence of boards containing 128MB data cells in selected other memory boards in the data processing system; and

means, coupled to the size means and to the input special condition signal indicating means, for combining the board special condition signal and the input special condition signal to generate a propagating system special condition signal indicating whether the memory board or any of the selected other memory boards in the data processing system contains 128MB data cells.

63. In a memory board operating in a data processing system, the memory board containing data cells which correspond to different values of an address, a method, performed by the memory board, of determining its own address space to map around holes when it is not possible to obtain a contiguous address space in the data processing system comprising the steps of:

generating a size signal specifying whether the memory board contains 32MB or 64MB data cells;

generating a board special condition signal indicating whether the memory board has 128MB data cells;

receiving a system special condition signal to indicate the presence of any memory boards in the data processing system containing 128MB data cells;

receiving an input slot identification signal indicating a slot position for the memory board in the data processing system;

generating an output slot identification signal from the input slot identification signal and the size signal;

analyzing the size signal, the system special condition signal, and the input slot identification signal to determine the values of the address signal which identify the data cells in the memory board;

receiving an input special condition signal indicating the presence of boards containing 128MB data cells

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in selected other memory boards in the data processing system; and

combining the board special condition signal and the input special condition signal to generate a propagating system special condition signal indicating whether the memory board or any of the selected other memory boards in the data processing system contains 128MB data cells.

FIG. 1

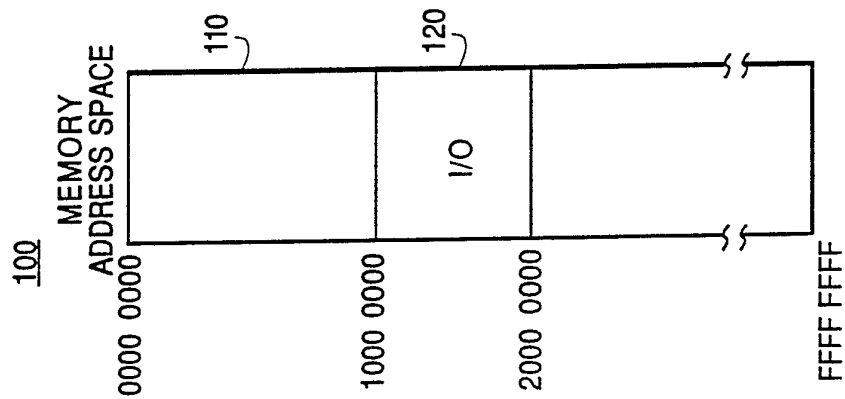


FIG. 3B

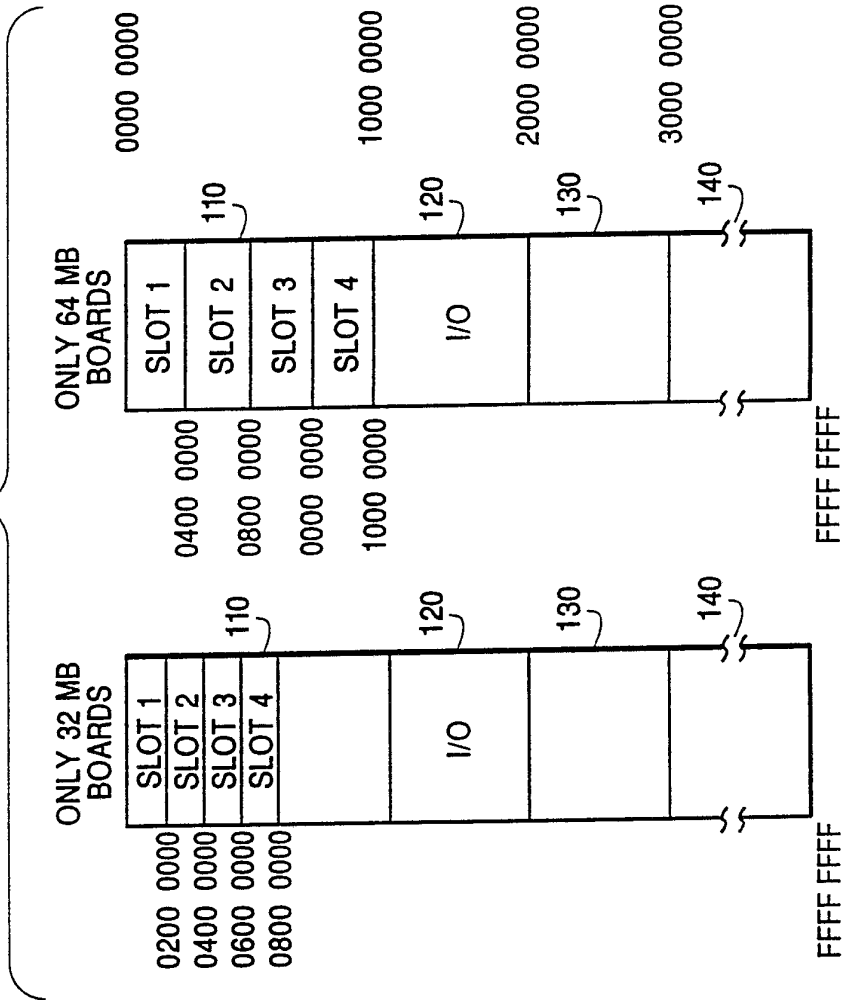


FIG. 2

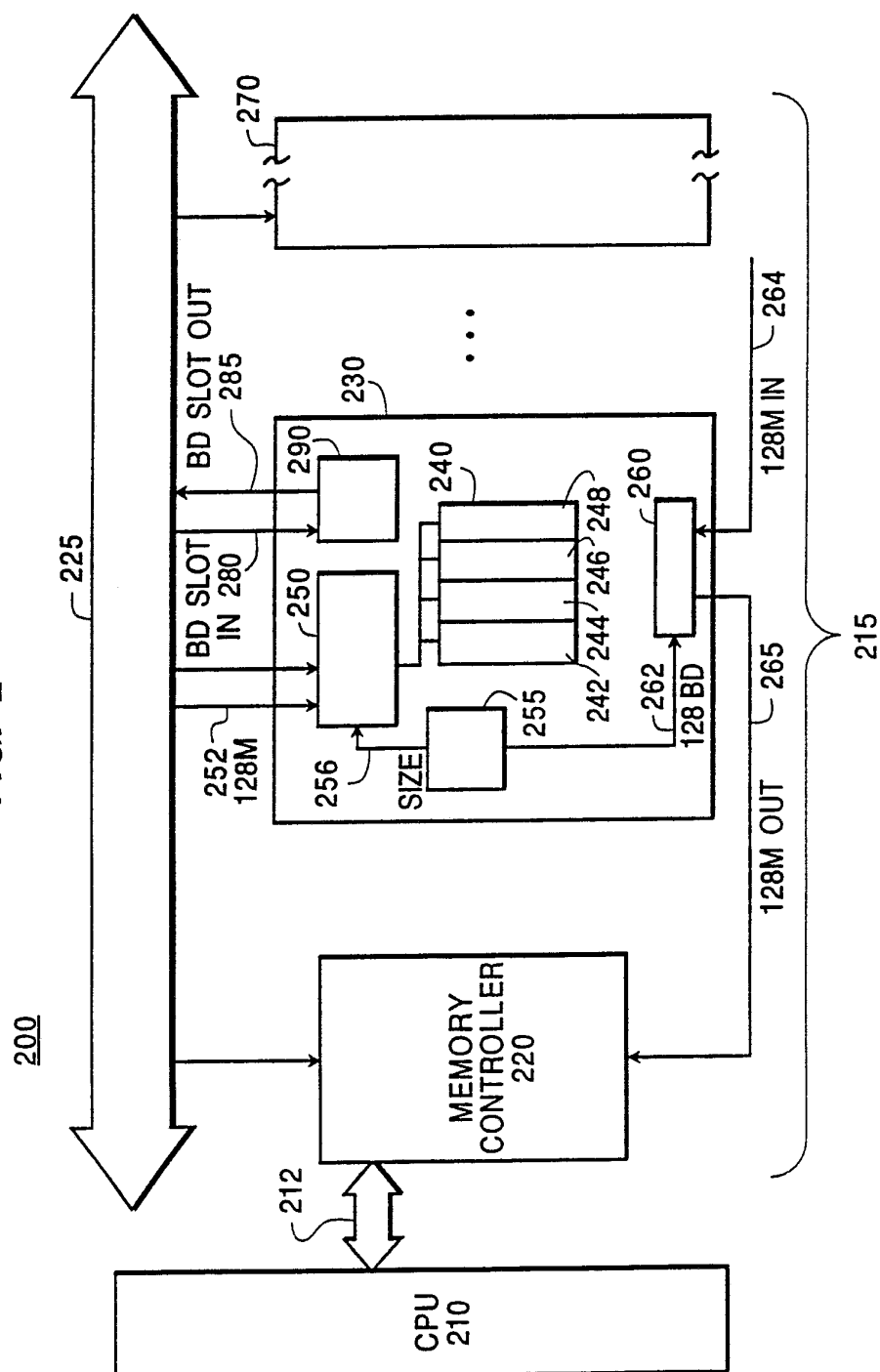
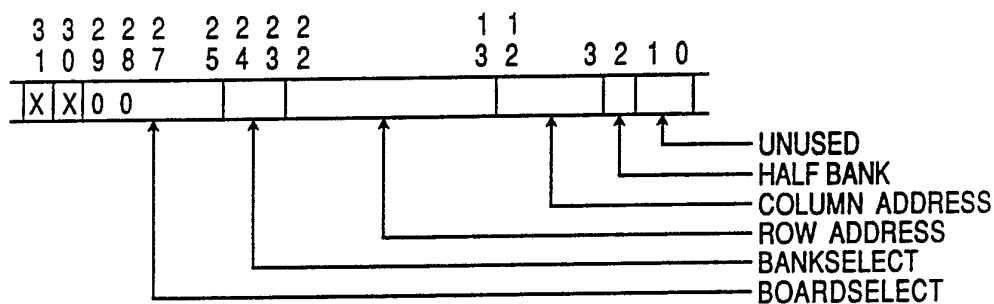
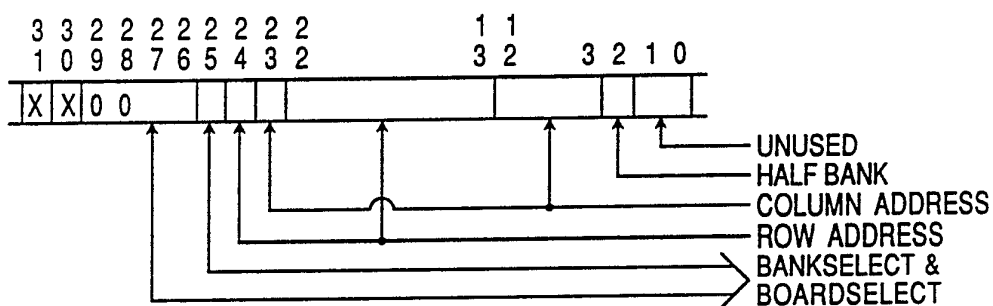
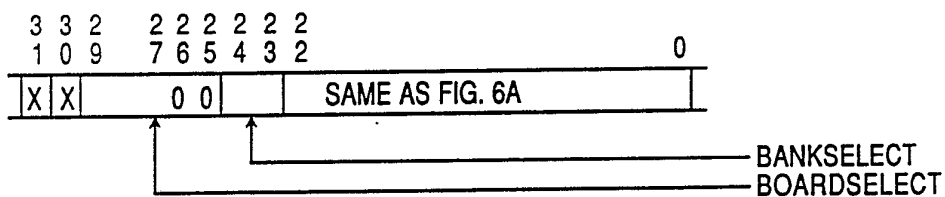
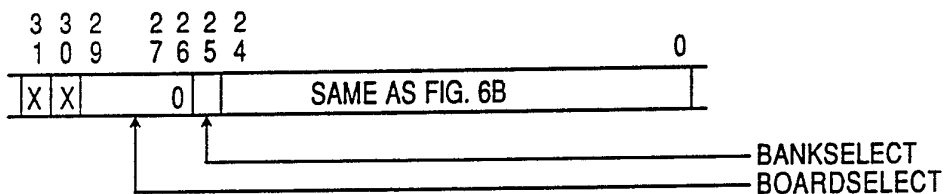
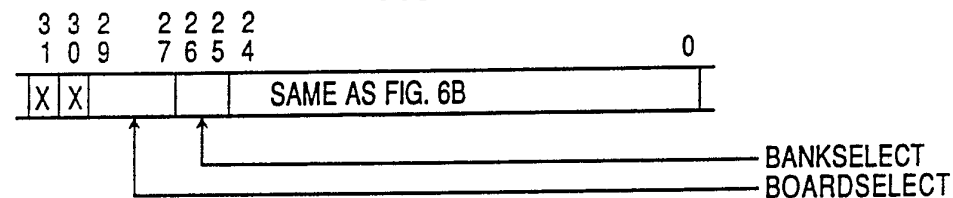


FIG. 4400

		SLOT #	STARTING ADDRESS		ENDING ADDRESS	
CASE 1	1	32MB	0000	0000	01FF	FFFF
	2	32MB	0200	0000	03FF	FFFF
	3	32MB	0400	0000	05FF	FFFF
	4	32MB	0600	0000	07FF	FFFF
CASE 2	1	32MB	0000	0000	01FF	FFFF
	2	64MB	0200	0000	05FF	FFFF
	3	32MB	0600	0000	07FF	FFFF
	4	64MB	0800	0000	0BFF	FFFF
CASE 3	1	64MB	0000	0000	03FF	FFFF
	2	32MB	0400	0000	05FF	FFFF
	3	64MB	0600	0000	09FF	FFFF
	4	32MB	0A00	0000	0BFF	FFFF
CASE 4	1	64MB	0000	0000	03FF	FFFF
	2	64MB	0400	0000	07FF	FFFF
	3	32MB	0800	0000	09FF	FFFF
	4	32MB	0A00	0000	0BFF	FFFF
CASE 5	1	32MB	0000	0000	01FF	FFFF
	2	32MB	0200	0000	03FF	FFFF
	3	64MB	0400	0000	07FF	FFFF
	4	64MB	0800	0000	0BFF	FFFF
CASE 6	1	32MB	0000	0000	01FF	FFFF
	2	64MB	0200	0000	05FF	FFFF
	3	64MB	0600	0000	09FF	FFFF
	4	32MB	0A00	0000	0BFF	FFFF
CASE 7	1	64MB	0000	0000	03FF	FFFF
	2	64MB	0400	0000	07FF	FFFF
	3	64MB	0800	0000	0BFF	FFFF
	4	64MB	0C00	0000	0FFF	FFFF

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FIG. 6A**FIG. 6B****FIG. 6C****FIG. 6D****FIG. 6E**

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FIG. 7

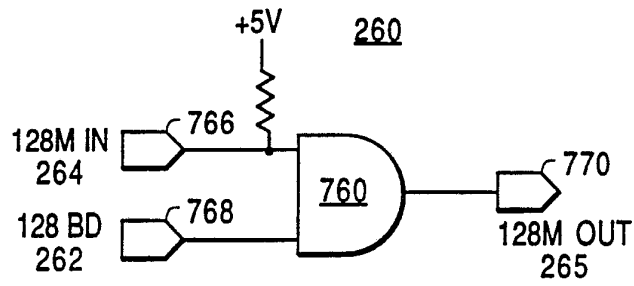


FIG. 9

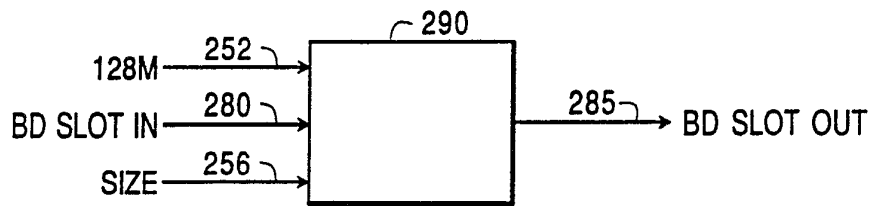


FIG. 11

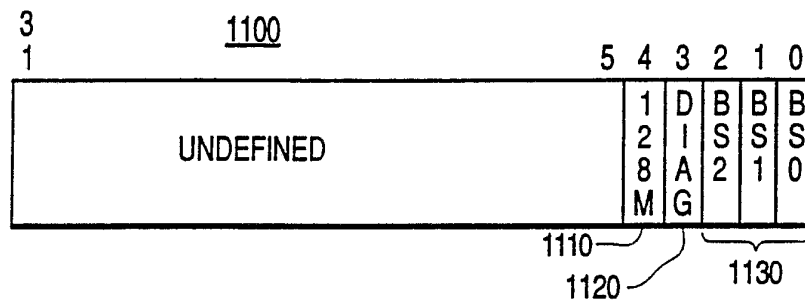
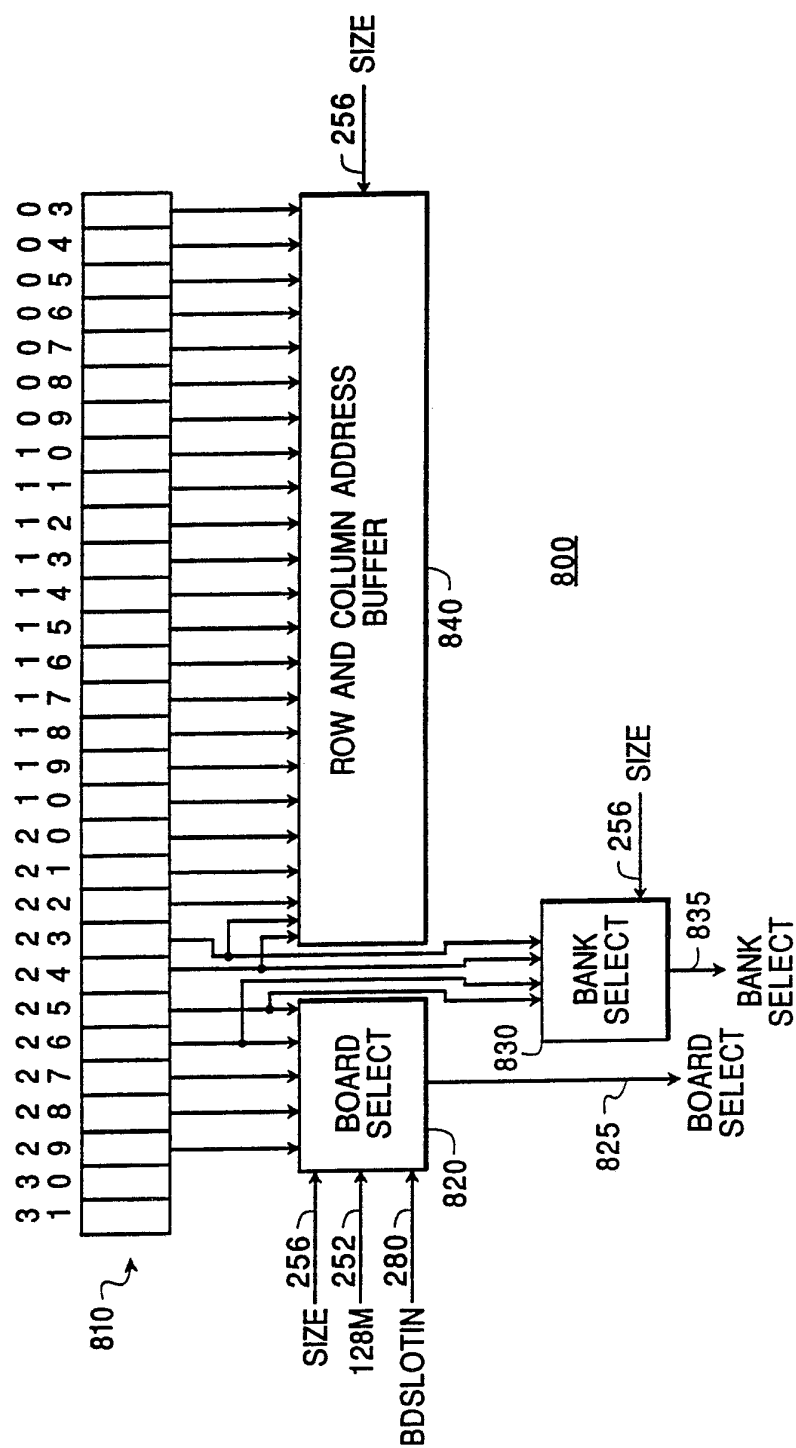
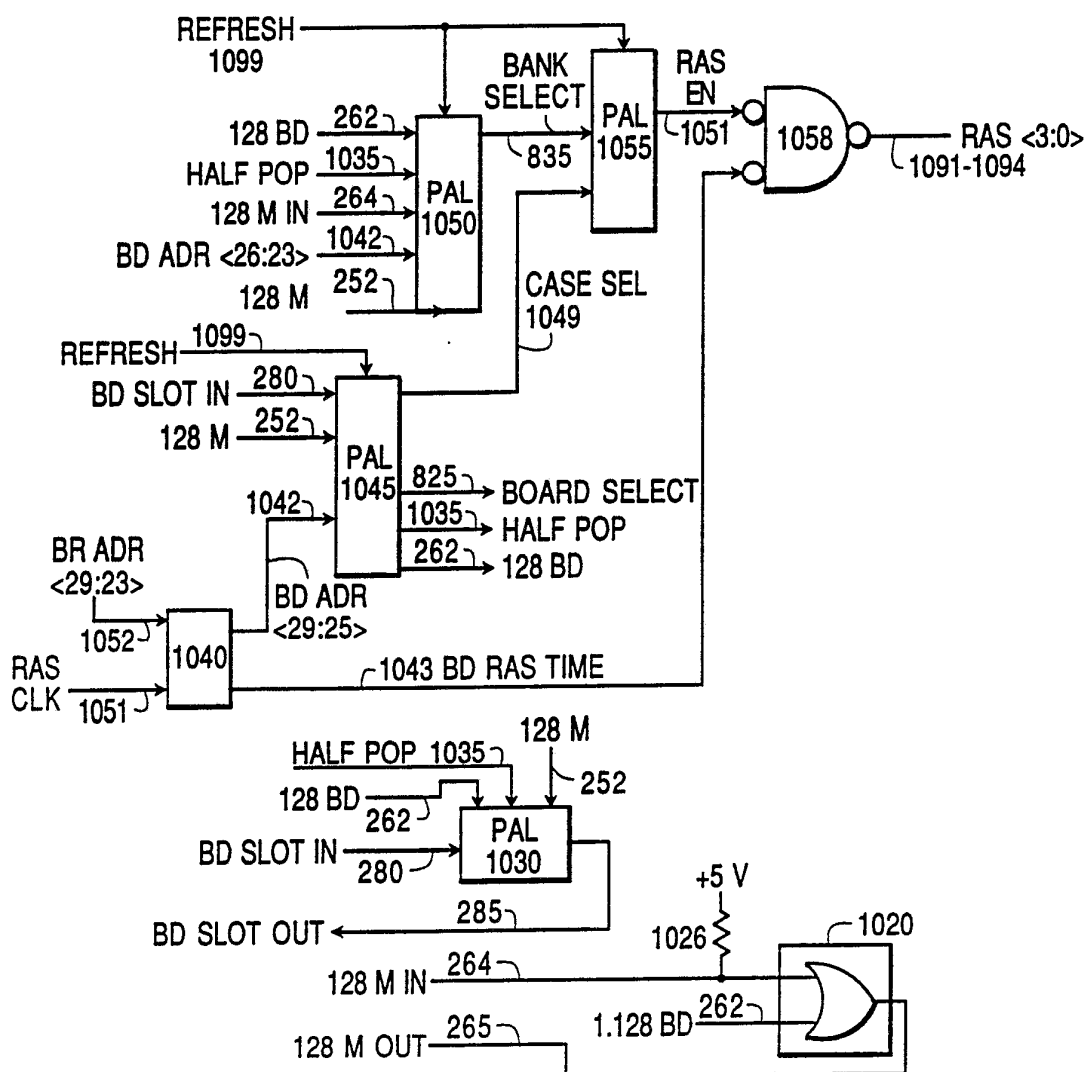


FIG. 8



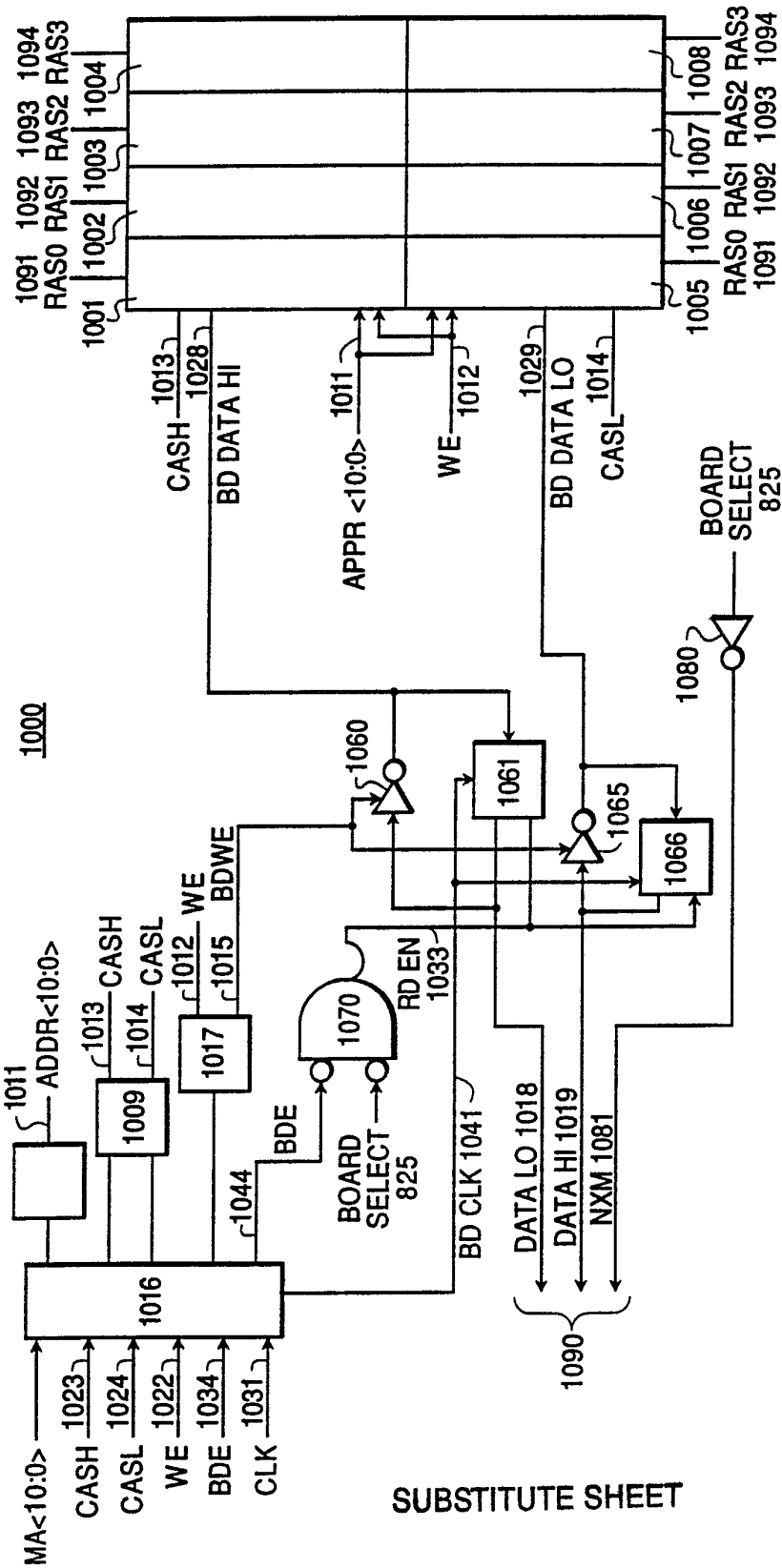
8 / 9

FIG. 10A



SUBSTITUTE SHEET

FIG. 10B



INTERNATIONAL SEARCH REPORT

PCT/US 91/06947

International Application No

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)⁶

According to International Patent Classification (IPC) or to both National Classification and IPC
Int.Cl. 5 G06F12/06

II. FIELDS SEARCHED

Minimum Documentation Searched⁷

Classification System	Classification Symbols
Int.Cl. 5	G06F

Documentation Searched other than Minimum Documentation
to the Extent that such Documents are Included in the Fields Searched⁸

III. DOCUMENTS CONSIDERED TO BE RELEVANT⁹

Category ¹⁰	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
X	GB,A,2 215 497 (SUN MICROSYSTEMS INC.) 20 September 1989	1,6-10, 12-14, 20-31, 34,35, 38,39, 44-61
	see page 3, line 1 - page 4, line 10 see page 7, line 9 - page 12, line 31 see page 13, line 7 - line 22 see abstract; figures 1-4	
Y		2,15,32, 40
A	---	62,62
	-/--	

¹⁰ Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
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"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
21 JANUARY 1992	28. 01. 92
International Searching Authority EUROPEAN PATENT OFFICE	Signature of Authorized Officer Alfredo Prein

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)		
Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
Y	GB,A,2 226 666 (INTEL CORP.) 4 July 1990 see page 1, line 28 - page 2, line 7 see page 4 see page 8, line 11 - page 9, line 2 see page 13, line 14 - page 14, line 8 see page 24, line 1 - page 25, line 26 see abstract	2,15,32, 40
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A	EP,A,0 336 435 (WANG LABORATORIES INC.) 11 October 1989 see page 2, line 25 - line 40 see page 3, line 4 - line 20 see page 4, line 18 - line 48 see page 7, line 4 - line 31; figures 1,3	1,6-9, 13, 20-23, 25-27, 31,38, 39,44, 46,47 51,53, 54,56-61
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**ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO. US 9106947
SA 52510**

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 21/01/92

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