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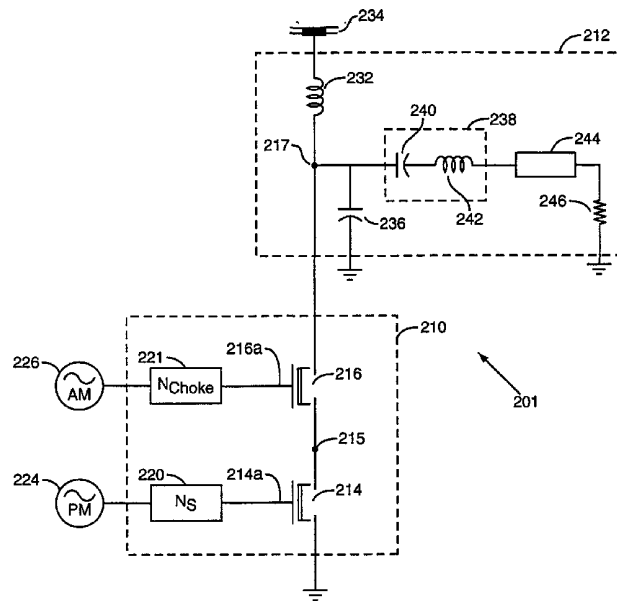
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(54) Title: TRIPLE CLASS E DOHERTY AMPLIFIER TOPOLOGY FOR HIGH EFFICIENCY SIGNAL TRANSMITTERS



(57) Abstract: A Doherty amplifier circuit is provided comprising at least three class E amplifiers (210) receiving separated amplitude (226) and phase information (224) from at least one signal source. At least one first impedance adjustment device is linked between the signal source and the inputs to at least two of the amplifiers, and a plurality of second impedance adjustment devices is linked to the outputs of the amplifiers to combine the outputs into an output of the circuit. In this way, a scheme for efficient amplification of amplitude modulated waveforms is achieved across a wide dynamic range and for a large peak-to-average ratio using only input modulated techniques.



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TRIPLE CLASS E DOHERTY AMPLIFIER TOPOLOGY FOR HIGH EFFICIENCY SIGNAL TRANSMITTERS

FIELD OF THE INVENTION

5 The present invention relates to power amplifiers. In particular, the present invention relates to efficient amplification of signals at a non-peaked average power level whose envelope is amplitude modulated, and specifically the application of linear amplification at RF frequencies of such signals up to high power levels.

BACKGROUND OF THE INVENTION

10 The requirements for higher data rates and bandwidth efficiency in wireless communication standards has caused designers to implement varying envelope modulation formats. The varying AM content of these formats allows for additional information to be transmitted in a given bandwidth. This varying envelope significantly constrains the ability of the power amplifier in a wireless device to linearly transmit the waveform. In addition, the varying envelope exhibits a "peak-to-average" ratio, where the average envelope power may be significantly below the peak envelope power. Ideally, the power amplifier would be capable of delivering peak power while operating at a much lower average power. Attempts at this, however, typically result in the application "backing-off" the power amplifier from peak in order to avoid clipping and distortion of the output waveform. This also results in an associated large decrease in efficiency from the peak. Moreover, the linearity of the power amplifier often requires that its output power be backed off even further than $P_{SAT} ((dBm) - PeakToAvgRatio(dB))$ in order to satisfy further constraints in adjacent channel power rejection (ACPR) and error vector magnitude (EVM). At a minimum, the power amplifier must provide "headroom" for the output power to actually reach the peak output power and not saturate prematurely. It thus becomes critical for efficiency that the power amplifier topology be able to maintain efficiency at higher power levels.

30 One established technique for extending peak efficiency under "backed-off" power conditions is the "Doherty" amplifier, an example of which

is shown in the schematic diagram of FIG. 1. The Doherty arrangement 2 utilizes two power amplifiers 4, 6 that saturate at different input power levels. This allows one amplifier to reach saturation and peak efficiency before the second. Because power amplifiers with higher output load impedances
5 saturate at lower output power levels, the dynamic loading of the first power amplifier by a second amplifier can change the output power level at which it saturates and achieves peak efficiency. This characteristic allows it to behave in a saturated mode over a range of output power because its load impedance decreases along with increasing output power. This dynamic loading and the
10 variation in output impedance over a range of output powers are achieved with a special power-combining load network 8.

In the typical exemplary implementation as shown, this output power combiner 8 utilizes a quarter-wave transformer 10 with characteristic impedance of 35.36 Ohms to transform from the load resistance of 50 to 25 at
15 the output combiner node 8. A second quarter-wave transformer 12 with characteristic impedance of 50 Ohms transforms the output combiner node impedance to the impedance seen at the output of the carrier power amplifier 4. In order to correct for the phase difference between the paths of the two amplifiers 4, 6, a quarter-wave transmission line 14 is inserted at the
20 input of the peaking amplifier 6, so that they sum coherently at their outputs. Initially, with the peaking amplifier 6 OFF, the load network 16 presents to the carrier power amplifier 4 in FIG. 1 a load impedance of $2 \cdot R_{OPT} = 100$ Ohms, and the high impedance of the peaking power amplifier does not significantly load the output combiner node.

25 The higher impedance presented to the carrier power amplifier 4 forces it to saturate earlier to optimum load impedance. In the exemplary case, shown in FIG. 1, the $2 \cdot R_{OPT}$ load forces it to saturate 3dB below peak. Once the peaking amplifier 6 activates, its finite output impedance starts to decrease the load impedance of the carrier power amplifier 4, until the point
30 when both the carrier and peaking amplifiers 4, 6 deliver equal power into their own respective local load impedances of $R_{OPT} = 50$ Ohms.

The effect of two power amplifiers delivering equally is that they provide 3dB more output power than one alone, and given the 3dB early saturation of the carrier amplifier 4, the pair 4, 6 provides a net 6dB power range over which efficiency is maintained at nearly peak saturated efficiency. This power range is critical "headroom" required for the envelope variation to be faithfully recreated at the power amplifier output, while still maintaining peak saturated efficiency.

Previous implementations of the Doherty configuration have utilized a class B amplifier as the carrier amplifier, and a class C amplifier as the peaking amplifier as shown in FIG. 1. The class C peaking amplifier is used because of its unique property of only turning "ON" once a threshold input power is delivered to it. This characteristic makes it convenient to drive both power amplifiers and to use this threshold property to turn on the peaking amplifier at the point that the carrier amplifier saturates.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

FIG. 1 is a schematic diagram of a prior art Doherty amplifier circuit that may be utilized in the present invention;

FIG. 2 is a schematic diagram illustrating an input modulation circuit for the load network of an amplifier as utilized in the present invention;

FIG. 3 is a graphical representation of the theoretical peak efficiencies of various power amplifiers according to their class topology;

FIG. 4 is a schematic diagram of a prior art Doherty amplifier configuration utilizing an input modulation approach applied in the present invention;

FIG. 5 is a schematic diagram of a first embodiment of the Doherty amplifier in accordance with the present invention;

FIG. 6 is a second embodiment of the Doherty amplifier in accordance with the present invention;

FIG. 7 is a third embodiment of the Doherty amplifier in accordance with the present invention implementing a feedback loop as an alternate configuration;

FIG. 8 is a schematic diagram of an alternative active switching circuit for providing a switched waveform input to standard class E output load matching network; and

FIG. 9 is another alternative embodiment showing a multiplexed input.

5 BRIEF SUMMARY OF THE INVENTION

The proposed invention introduces a novel extension of the Doherty concept to more than two stages, thereby extending the output power range over which peak efficiency may be attained. The general application of these architectures is further described with the use of class E amplifying stages with their significantly higher efficiencies. In particular, class E amplifiers are
10 utilized, and input modulation approaches proposed by the inventor are implemented. These implementations are disclosed in Case Reference Nos. P10550-US1-BMOT, P10551-US1-BMOT, and P10552-US1-BMOT, filed concurrently herewith and incorporated herein by reference.

15 In accordance with the present invention, a first embodiment of an amplifier circuit is disclosed comprising at least three class E amplifiers receiving separated amplitude and phase information from at least one signal source, at least one first impedance adjustment device linked between the signal source and the inputs to at least two of the amplifiers, and a plurality of
20 second impedance adjustment devices linked to the outputs of the amplifiers to combine the outputs into an output of the circuit.

In another aspect of the invention, another embodiment of a amplifier circuit is disclosed comprising at least one signal source producing a plurality of digital amplitude modulation signals and a digital phase modulated signal, and a first class E carrier amplifier linked to receive one of the amplitude
25 modulation signals and the phase modulation signal. A first class E peaking amplifier is linked to receive another of the amplitude modulation signals and the phase modulation signal via one or more impedance adjusting devices. A second class E peaking amplifier is linked to receive another of the amplitude
30 modulation signals and the phase modulation signal via one or more

impedance adjusting devices. A combining circuit links the outputs of the amplifiers via one or more impedance adjusting devices.

The invention may also be embodied in a method of providing high-efficiency signal amplification. The method comprises the steps of providing a first digital amplitude waveform to a class E carrier amplifier, providing a first digital phase waveform to a first class E peaking amplifier, providing a second digital phase waveform to a second class E peaking amplifier, providing a shared digital phase waveform to the carrier and peaking amplifiers, and combining the outputs of the carrier and peaking amplifiers via one or more impedance adjusting devices to produce an amplified signal output.

Advantages of the present invention will become readily apparent to those skilled in the art from the following description of the preferred embodiments of the invention, which have been shown and described by way of illustration. As will be realized, the invention is capable of other and different embodiments, and its details are capable of modifications in various respects. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not as restrictive.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

I. Input Modulation For Envelope Restoration In Class E Amplifiers.

The various amplifier embodiments referred to above and disclosed herein involve the use of saturated class E amplifiers. The input to the amplifiers is modulated in various ways to vary the output power. Each of these approaches may be utilized here, but the TIMER input modulation scheme (Transmitter using Input Modulation for Envelope Restoration) is used as an example throughout the preferred embodiment herein for purposes of continuity. The use of the TIMER scheme in the present embodiment involves utilizing a dual-gate FET device as the active switch component in a class E design as shown in FIG. 2. Generally, one switch is driven by the phase-only constant envelope information, and the other switch is used to modulate the output power envelope. The use of this second envelope

terminal allows for the power amplifier to be turned ON independently of the drive level, affording more flexibility for Doherty-like schemes where the peaking amplifier is typically turned on based on the input drive power level.

Turning now to the drawings, wherein like numerals designate like components, FIG. 2 is a diagram of an active device switching circuit 210 combined with an output load matching network 212 to make up a class E amplifier 201. The circuit 210 preferably includes a pair of switching devices 214 and 216, each of which may be independently controlled to exhibit different resistances to the total current flowing through the pair. The switching devices should be lower minimum "ON" resistance devices with high-speed switching capabilities, one example would be the MWT-5 Dual-gate FET (reference http://www.mwtinc.com/cat/fets/htm/new-html/MwT-5_1.htm) manufactured by MWT, Inc. These devices are exemplary only for this embodiment, and a wide variety of other components or structures may be substituted for the components described in accordance with the knowledge of one skilled in the art.

The switching devices 214, 216 are linked in series or "cascode" as shown connected to the output load matching network 212 at node 217. The gates 214a and 216a of each of the transistors 214 and 216 receive phase information 224 and amplitude information 226, respectively, from a primary waveform. The received information 224 and 226 into the gates 214a and 216a of the transistors 214 and 216 is utilized to vary the switching resistance of the transistors in accordance with the input primary waveform to create a secondary waveform at node 217.

The implemented standard class E amplifier comprises a single transistor switch and an output load matching network 212. The connection node 217 between the active switch devices 210 and this standard class E output load matching network 212 comprises an inductance coil 232 connecting to the supply voltage Vdd 234. A capacitance 236 which includes parasitic capacitance from the active device(s) in parallel with the active device output impedance. A tuned circuit filter 238 consisting of a capacitance 240 and an inductance 242 is connected in series with a reactive

component 244 and a load resistance 246, nominally 50 Ohms. Typically, frequency and phase modulation information is received from the switches at node 217, and amplitude modulation information is received by variation of the supply voltage Vdd at 234. However, in the present case, as will be
5 described below, the phase and amplitude information 224 and 226 are both received as a switched input at 214a and 216a and the input terminals are used to combine phase and amplitude information to a desired signal at node 217, such that the final signal delivered to the load 246 is as desired.

A matching network 220 is linked to input gate 214a of the active
10 switching device 214 to provide optimum power transfer from the phase modulated source to the switching device 214. The matching network 220 may comprise a number of reactive elements according to known methods. Another matching network 221 is linked to the input gate 216b of the active
15 switching device 216 to block any phase information from reaching the amplitude modulated source, while still providing a low frequency path from the amplitude modulated source to the switching device 216. This second matching network also may comprise a combination of reactive elements according to known methods.

During operation, the active switching device 214 is gated on and off
20 through the gate 214a in accordance with the received phase information 224. Similarly, the switching device 216 is gated on and off via the input 216a in accordance with envelope information 226 received at the gate. Given that one switch switches at an RF frequency between an entirely off state to an entirely on state, the output across the load 46 of the matching network 212 of
25 the amplifier 201 is determined by the total "ON" resistance of the pair of switching devices 214 and 216. The output can be modulated by the switch having the higher "ON" resistance. In the present case, switch 216 can thus be driven with a low frequency signal so that the "ON" resistance of the switch 216 produces a flexibly adjusted output amplitude and thus restores the
30 output envelope amplitude. The second switch 216 is continuously variable and allows for a smoothly continuous change in the "ON" resistance, and an associated continuous change in the output envelope amplitude.

The switching device 216 slowly varies the envelope information. The function of this information in the switch configuration of the circuit 210 is to provide additional isolation of the RF feedthrough between the high-speed switching of the phase information input and the node connected to the load network. The switching device 214 receives a high-frequency input and has a direct source connection to the load-inductance ground for enhanced stability. The node 215 between the switches 214 and 216 traces the output node connected to the load network, thereby causing the switch 216 to switch on and off at the same frequency as the lower switch. The switching device 214 receives a high-frequency input and has a direct source connection to low inductance ground for enhanced stability. Preferably, the switches are capable of switching at high frequencies so that maximum gain and efficiency may be attained from this cascode configuration.

The present switching circuit 210 advantageously allows a single RF input into the matching network 212 and a second low-frequency baseband envelope input to achieve the variable "ON" resistance necessary for input into the matching network 212. This reduces the necessity for multiple RF inputs and associated high-frequency signal lines on valuable circuit board real estate. Furthermore, the requirement for multiple matching networks or multiplexing functions preceding the actual matching network 212 are not required.

In class E devices, the peak efficiency is much higher than the class C configuration, theoretically 100% vs. 85% (for 73.5° conduction angle in class C case) as diagrammed in FIG. 3. Realistically achievable efficiencies at RF frequencies for class E vs. class C devices are upwards of 80% vs. 65% respectively. One shortcoming of the TIMER scheme is that for modulation formats requiring envelope variation, the average efficiency falls off as a function of the output power back off required. In simulation environments, a 3dB peak-to-average ratio results in a peak efficiency of greater than 80%, but average efficiency at roughly 50%. This roll-off in efficiency results because of the loss inherent in the increased switching ON resistance of the active device that is the basis for the modulation of the output envelope.

II. The Doherty Concept Including Input Modulation Class E Techniques.

5 A first implementation of an embodiment of a Doherty scheme using the TIMER input modulation of class E amplifiers is shown in FIG 4. The two amplifiers 404, 406 shown in this embodiment are both driven by a phase-only constant envelope signal, and the separate envelope modulation inputs are used to stagger the output powers of the carrier and peaking amplifiers to result in an extended peak efficiency range. As the carrier amplifier reaches saturation at peak power and efficiency with the peaking amplifier off, the peaking amplifier is turned on and the efficiency range is extended to the point 10 where both amplifiers deliver their peak output powers equally, and the maximum combined output power is reached.

III. Multiple-Stage Doherty Concepts.

15 In accordance with the present invention, the Doherty concept is extended in an attempt to increase the range of the peak efficiency to beyond 6dB backed-off from peak. This is accomplished by using more than just the two stages shown in FIG. 4. A three-stage Doherty configuration is shown in the amplifier circuit 501 of FIG. 5 and represents an extension of the peak efficiency to as much as 9.5dB backed-off from peak. As shown in the Figure, 20 three linked class E amplifiers 504, 506, and 508 are arranged as shown in the schematic diagram. The amplifier 504 acts as the carrier amplifier, while the amplifiers 506 and 508 act as the first and second peaking amplifiers, respectively. The outputs 504a, 506a, and 508a are linked by quarter-wave lines 510 and 512 having characteristic impedances of 50ohms and 25 17.68ohms, respectively. The outputs of the amplifiers are linked at 514a to a 25ohm quarter-wave line 514. The quarter-wave line 514 is in turn linked to the RF output 518 and a load resistance 516.

30 The digital signal processor 500 generates the separated amplitude and phase waveforms via outputs 540, 542, 543 and 544, completely controls the delay that is introduced between the phase and amplitude signal paths. The outputs 540, 542 and 546 output an amplitude modulated signal for the carrier and the peaking power amplifiers 504, 506 and 508, respectively. High

bit-rate digital to analog converters 550, 552 and 556 are connected to the outputs 540, 542 and 546, respectively, to convert the digital signals from the DSP 500 to analog signals before connection to the amplifiers 504, 506 and 508.

5 The output 543 of the DSP 500 produces a shared phase-modulated waveform at the RF frequency for input into the amplifiers 504, 506 and 508. The output 543 inputs the digital signal from the DSP 500 to a high bit-rate digital to analog converter 554 for conversion of the signal to analog format. The converter 554 is in turn linked to a quadrature-modulating upconverter
10 560 and a bandpass noise filter 562 if required. A filter is not required for the baseband amplitude modulated signals.

 The output of the bandpass noise filter 562 is input directly into the class E carrier amplifier 504. The phase modulation signal provided at line 520 is impedance-corrected by 50 ohm quarter-wave lines at the inputs of the
15 first and the second peaking amplifiers 506 and 508. In particular, the quarter-wave line 522 is linked to the input to the amplifier 506, and a pair of quarter-wave lines 524a and 524b are series-linked to an input of the peaking amplifier 508.

 One advantage of the architecture of FIG. 5 is that only a single filter
20 for the shared phase modulated RF signal is required for suppression of out-of-band noise, as the amplitude modulated baseband signals do not require filtering. The digital signal processor (DSP) is used to generate all three required signals, and high bit-rate digital-to-analog converters (DAC) are used to output high-resolution analog signals for the power amplifier inputs. The
25 bandpass filtering of the RF frequency phase modulated input signal may or may not be required in this implementation depending on the architecture of the modulator block and the specific communication standard applied.

 The principle in the circuit 501 is similar to the basic Doherty, with the following sequence of amplifier behavior and corresponding output
30 impedances presented to each amplifier 504, 506 and 508 by the load network of quarter-wave transmission lines:

Amplifier Sequence	Carrier Amplifier State / Rout	Peaking Amplifier #1 State / Rout	Peaking Amplifier #2 State / Rout	Total Solution Output
1	Saturated/100 Ohms	Off/25 Ohms	Off/12.5 Ohms	9dB
2	Saturated/50 Ohms	Saturated/50 Ohms	Off/12.5 Ohms	3dB below
3	Saturated/100 Ohms	Saturated/25 Ohms	Saturated/25 Ohms	Peak

5 The means for presenting these specific impedances to the amplifier stages is a novel combiner network of the invention where the quarter-wave lines diagrammed in FIG. 5 are arranged such that the characteristic impedance of the quarter-wave line 510 between the carrier amplifier 504 and first peaking amplifier 506 is defined as :

$$Z_{OC} = 2 * R_{OPT} \tag{1}$$

10 where R_{opt} is defined as the optimal load impedance for the carrier amplifier. The quarter-wave line 512 between the first peaking amplifier 506 and the second peaking amplifier 508 is defined with a characteristic impedance of :

$$Z_{OP} = R_{OPT} / (2)^{3/2} \tag{2}$$

And the quarter-wave line 514 between the second peaking amplifier 508 and the load resistance 516 is defined to be

$$Z_{OL} = (R_L R_{OPT})^{1/2} / 2 \tag{3}$$

15 The operation of the three-stage example in FIG. 5 proceeds according to the sequence of the above Table and begins with the lone carrier amplifier 504

powered on and presented with a 100 Ohm load at its output. Because the carrier amplifier of this example is optimized for peak power output at a load impedance of 50 Ohms, it will saturate at an output power 3dB lower than that optimum case. As the first peaking amplifier 506 turns on, the two branches feeding into quarter-wave line 512 (output 506a and the quarter-wave line 510) increase in impedance because two power sources in parallel are feeding that 25 Ohm impedance. As a result the impedance presented to the quarter-wave line 510 goes up by a factor of two to 50 Ohms, and the corresponding inverted impedance transformed to the output of carrier amplifier 504 goes down by a factor of two, to 50 Ohms. The impedance presented to the first peaking amplifier 506 is 50 Ohms as well, and both amplifiers deliver equal output power combining for roughly 6dB more total output power than in sequence 1 where the carrier amplifier operated alone. When the second peaking amplifier turns on according to sequence 3 in the Table, the impedance presented to both the output of the second peaking amplifier 508 (508a) and the quarter-wave line 512 go up by a factor of two to 25 Ohms. Through the inverting impedance transformation of quarter-wave line 512, the impedances presented to the output of the first peaking amplifier 506 and carrier amplifier 504 become 25 Ohms and 100 Ohms respectively. The second peaking amplifier sees a 25 Ohm load at its output also, and the first and second peaking amplifiers deliver equal power at the maximum capable for the total amplifier solution, roughly 3dB above sequence 2 and a full 9dB above sequence 1. The sum of the individual amplifier power levels shown in the Table above result in the overall amplifier output power, and peak efficiency is maintained over a range of over 9dB. A critical aspect of the selection of these output impedance levels and the corresponding values of the quarter-wave impedance inverting transmission lines is that the output impedance presented to the amplifiers that are OFF and about to ramp up must be greater than the critical low resistance value for which the output power and efficiency all drop off rapidly. If that resistance is too low (12.5 Ω in the case of the amplifier 508 in the above table), then the transition as the

amplifier 508 starts to contribute will cause a significant dip in the drain efficiency of the overall amplifier circuit 501.

5 Simulations for this configuration show that the peak efficiency is maintained at close to 80%. The configuration is designed to peak exactly at 3dB below the peak output power of the entire amplifier circuit 501. This is an ideal behavior for signals with a peak-to-average power ratio of 3.2dB such as IS-136 and EDGE. The addition of the third amplifier path (peaking amplifier 508) provides for significantly higher efficiency down to greater than 9dB output power back-off, and significantly extends the power range for peak efficiency over the two-path CEDA implementations of two-path Doherty configurations.

10 An additional extension of this concept is to size the amplifiers differently and to design the quarter-wave transmission lines differently such that a wider dynamic range is achieved. By sizing the carrier amplifier to be smaller than the peaking amplifiers, the lowest peak in efficiency will occur at a much lower power level and may be optimized for the specifics of a given communication system. As the ability of the carrier and peaking amplifiers to deliver the same peak power becomes limited by this, the efficiency at power levels between sequences 1 and 2, and 2 and 3 in the Table will become smaller causing larger dips in efficiency at power levels between those at which the amplifiers are delivering equal power. Some mitigation of this can be achieved by optimal sizing of the quarter-wave transmission lines, in order to optimize the power levels for which unequal impedances are presented to the combination of amplifiers.

25 An additional extension of the present three-stage embodiment is to add yet another path for a total of four paths. This is shown in the schematic diagram of FIG. 6, wherein a quadruple amplifier circuit is shown including the carrier amplifier 604 and three peaking amplifiers 606, 608 and 609. For clarity, the upconverter block and the bandpass filtering components shown in FIG. 5 are not shown in FIG. 6. The four amplifiers 604, 606, 608 and 609 define four stages 603, 605 and 607, including the fourth stage 611 as shown. The fourth stage 611 includes the third peaking amplifier 609 connected to

receive the amplitude modulated signal via the input 609b from a signal-generating source. The peaking amplifier 609 also receives the shared phase modulation input through three quarter-wave, 50ohm impedance lines 613, 615 and 617 linked in series as shown. The output 604a of the carrier amplifier 604 is linked to the output 606a of the first peaking amplifier 606 via a 100ohm quarter-wave line 618. These outputs are in turn linked to the output 608a of the second peaking amplifier 608 via a 35.35ohm quarter-wave line 614. These outputs are linked, in turn, to the output 609a of the third peaking amplifier 609 via a 17.68ohm quarter-wave line 612. The remainder of the circuit 601 is similar to that shown in FIG. 5 above.

This implementation extends the dynamic range of the peak efficiency further, and additional paths can be implemented until the circuit starts to exceed the reasonable range of characteristic impedance required in the design of the quarter-wave transmission lines, the complexity of predistorting additional envelope terminal voltages, and the area and output losses start to impact performance. These limitations depend on the core amplifier design and the transmission line technology implemented. The other implication is that the very high impedance seen by the carrier amplifier when it operates alone will become very high and the class E efficiency will eventually degrade significantly, but still operating at higher efficiencies than an amplifier of fewer paths at that minimum power.

A. Predistortion Options

As with the standard Doherty configuration, some amplitude and phase predistortion is required so that the envelope modulation on the input translates to the desired output envelope satisfying linearity specifications of adjacent channel power ratio (ACPR) and error vector magnitude (EVM). This implementation is shown in FIG. 7, wherein the phase is adjusted so that the AM/PM can be compensated. In particular, a unique input waveform for any given desired output may be defined so that a baseband digital signal processor can properly generate the corrected input waveform. This predistortion methodology is well-known in the art. In the alternative, an additional feedback loop may be implemented to periodically update the input-to-output relationship in accordance with any long-term degradation requirements. For example, a feedback loop 702 may be used to sense any voltage standing wave ratio ("VSWR") reflection from the antenna 774. The feedback loop may then control the digital signal processor 700 to adjust the amplitude information to correct for any VSWR reflection before the amplitude information is received by the amplifiers 704, 706 and 708. With this predistortion in place, the linearity of the amplifier module can be achieved with extremely high efficiency.

Several aspects differentiate this implementation from standard Doherty amplifiers using class C and class B amplifiers. For example, the separation in a class E amplifier of the RF constant envelope phase information from the lower frequency envelope modulation at the input allows for the second power amplifier to be turned on by the envelope modulation terminal, and not by the drive level of a combined I/Q modulated RF signal only.

In addition, the peak efficiency is much higher for the class E implementation, allowing the use of extremely high efficiency, constant envelope modulation within the same power amplifier module. Moreover, the use of fixed DC voltage steps down from the battery voltage allows for the same efficiency performance down to extremely low voltages. These voltages are even lower than for standard Doherty implementations using class B or C

amplifiers. Finally, distinctive advantages are possible through the use of class E amplifiers. These amplifiers allow for minimum die dimension and the smallest single stage power amplifier of all classes of amplifiers. The potential for stable use of ultra-small gate dimension FET's is not possible with other amplifier topologies.

The efficiency at lower output power levels for this configuration is governed by the carrier amplifier alone as the peaking amplifier is turned off. This efficiency will be better than for a single class E amplifier sized for the peak output power, because the carrier amplifier is designed to saturate at roughly 3dB below the peak output power of the triple stage Doherty class E module proposed. This results in a shift of the entire efficiency curve down in power by roughly 3dB and a net higher efficiency at all levels.

B. Other Implementations

The present invention may also be implemented in alternative configurations. Most importantly, other input modulation schemes may be utilized with implementations of the present invention, either substituted for or used in addition to the TIMER scheme illustrated herein.

1. Active Switch Input Modulation

For example, FIG. 8 shows a diagram of a active device switching circuit 810 combined with an output load matching network 812 to make up an amplifier 801. The circuit 810 preferably includes a single switching device 816 linked to a tuned filter 815. The switching device 816 should be a lower minimum "ON" resistance device with high-speed switching capabilities, one example would be the 2SK2922 LDMOS RF discrete FET transistor manufactured by Hitachi, Inc.

(<http://www.hitachi.co.jp/Sicd/English/Products/transise.htm>). These devices are exemplary only for this embodiment, and a wide variety of other components or structures may be substituted for the components described in accordance with the knowledge of one skilled in the art. The filter 815 preferably includes a capacitance 818 and an RF choke coil 819 linked in series and through their central connection node to the gated input 816a to the switching device 816. These devices are exemplary only, and a wide

variety of other components or structures may be substituted for the components described in accordance with the knowledge of one skilled in the art.

5 The filter 815 utilizes the capacitance 818 and the RF choke 819 for summation of the combined DC envelope and RF phase waveforms. Using this preferred configuration to combining the waveforms, the variation in "ON" voltage is small and the "ON" resistance can in turn be controlled with a minimum of distortion.

10 The switching device 816 is in turn linked as shown to the load network input 817 of the amplifier 812. The gate 816a of the switching device 816 receives a combined input of phase information 824 and amplitude information 826 that are input into the filter 815 through inputs 815a and 815b, respectively, from a primary waveform. A matching network 820 is linked to input 815a to provide optimum power transfer from the phase modulated
15 source through the tuned filter to the input gate 816a of the switching device 816. The matching network 820 may comprise a number of reactive elements according to known methods. The received information 824 and 826 is utilized to vary the switching resistance of the switching device 816 in accordance with the input primary waveform to create a secondary waveform
20 for the amplifier input 817.

During operation, the active switching device 816 is gated on and off through the gate 816a in accordance with the combined received phase and amplitude information 824 and 826. Given that the device 816 switches at an RF frequency between an entirely off state to an entirely on state, the output
25 across the load resistance 846 of the matching network 812 is determined by the modulated "ON" resistance of the switching device 816. The switch 816 can thus be driven with a low frequency signal so that the "ON" resistance of the switch 816 produces a flexibly adjusted output amplitude and thus restores the output envelope amplitude.

30 The switching device 816 slowly varies the envelope information. The function of this information in the switch configuration of the circuit 810 provides additional isolation of the RF feedthrough between the high-speed

switching of the phase information input and the node connected to the load network.

The present switching circuit 810 advantageously allows a single RF input into the matching network 812 and a low-frequency baseband envelope input to achieve the variable "ON" resistance necessary for input into the matching network 812. This reduces the necessity for multiple RF inputs and associated high-frequency signal lines on valuable circuit board real estate. Furthermore, the requirement for multiple matching networks or multiplexing functions preceding the actual matching network 812 are not required.

2. Multiplexed Input Modulation

In another input modulation implementation, a multiplexed input envelope restoration circuit may be utilized as shown in FIG. 9. In particular, FIG. 9 is a diagram of a active device switching circuit 910 combined with an output load matching network 912 to make up an amplifier 901. The circuit 910 preferably includes a control device 914 and a plurality of switching devices 916, 918, 920, and 922, each having a different current resistance, and a control device 914. The control device is preferably a multiplexer, such as that commonly available from Motorola, Inc. The switching devices should be lower minimum "ON" resistance devices with high-speed switching capabilities, one example would be the 2SK2922 LDMOS RF discrete FET transistor manufactured by Hitachi, Inc.

(<http://www.hitachi.co.jp/Sicd/English/Products/transise.htm>). These devices are exemplary only for this embodiment, and a wide variety of other components or structures may be substituted for the components described in accordance with the knowledge of one skilled in the art.

The control device 914 receives amplitude information 924 and phase information 926 from a primary waveform. The phase information 926 and amplitude information 924 are received into inputs 914a and 914b of the control device 914. A matching network 928 is linked to input 914b to provide optimum power transfer from the phase modulated source through the control device 914 to input gates 916a, 918a, 920a, and 922a of the switching devices 916, 918, 920, and 922. The matching network 928 may comprise a

number of reactive elements according to known methods. Alternative embodiments may include and/or replace matching network 928 with individual matching networks following the control device 914 for further optimization of the input matching for these different-sized switching devices 916, 918, 920, and 922.

The control device 914 uses the amplitude information 924 to select an active switching device from the plurality of switching devices 916, 918, 920, and 922. The switching devices 916, 918, 920, and 922 are controlled by the control device 914 via inputs 916a, 918a, 920a, and 922a. After selecting an active switching device, the control device 914 uses the phase information 926 to control the active switching device to create a secondary waveform for input to the amplifier load network 912 at node 917.

During operation, the control device 914 controls the active switching devices in accordance with the phase information 926. The control device 914 preferably turns the active switching device off and on in response to the phase information 926. As a result, the switch voltage varies between zero and the peak switch voltage of the active switching device.

Because the switching devices 916, 918, 920, and 922 each have a different "ON" resistance, they each exhibit a different peak switching voltage when activated. The control device 914 selects an active switching device in accordance with the amplitude information 924 to achieve a desired peak switch voltage. By selecting an appropriate active switching device for a given time period, the peak amplitude of the switch voltage may be varied to produce a quantized approximation of the amplitude envelope of the primary waveform. As the voltage across the active switching device varies in response to the phase information 926, it is limited to the peak switch voltage of the particular active switching device selected in accordance with the amplitude information 924. Preferably, the amplitude information 924 and phase information 926 are used to create a secondary waveform that approximates the primary waveform. The secondary waveform is then provided as input to the 912 matching network of the amplifier 901.

C. Use of High Dielectrics for Quarter Wave Delay and Transmission Lines

5 Other implementations are also contemplated. For example, high dielectric materials may be used to shrink the combiner network in the above embodiment. The effective electrical length is a function of the relative dielectric permittivity of the material on which the microstrip transmission line is fabricated. The electrical length depends on the inverse square root of ϵ_r . Building the transmission lines for 1 GHz operation on FR4 standard PCB material with a relative dielectric constant of 4 will mean that each quarter wave line will be approximately 1.48 inches in length. This would shrink to approximately 0.33 inches by using a high dielectric material with relative permeability of approximately 80. The use of a hybrid module assembly employing high dielectric material could be implemented to significantly decrease the size of the solution.

15 D. Use of Stepped DC Supply Voltage

In another alternative, the DC control voltage may be modified to achieve peak efficiency at lower discrete power states. An additional aspect of the class E amplifiers used in this scheme is that they retain their efficiency for a given load network better than all other topologies as the DC supply voltage is dropped. This is caused by the variation in output impedance as the supply decreases, and degradation in the output match for the power amplifier. In the class E configuration, wide tolerance on the exact capacitance value induces some variation in AM/PM characteristics, but does not significantly affect the efficiency. Thus, the DC supply voltage may be controlled in fixed increments so that the DC level can control the absolute average power level, keeping the phase drive and envelope modulation the same for the input drive. As with the previous embodiments, the variation in the AM/PM with DC supply voltage will require some phase predistortion, but the efficiency is maintained at peak levels down to very low powers.

30 Of course, it should be understood that a wide range of changes and modifications can be made to the preferred embodiments described above. For example, different technologies can be used for the switching device

shown in the circuits of the preferred embodiments above to exploit the capabilities and different functionality of each component. Such substitutions, taking into account the performance trade-offs of using either the upper or lower switch for modulating the envelope will be different for each case.

5 Thus, it is intended that the foregoing detailed description be regarded as illustrative rather than limiting, and that it be understood that it is the following claims, including all equivalents, which are intended to define the scope of this invention.

CLAIMS

1. An amplifier circuit comprising:
at least three class E amplifiers receiving separated amplitude
and phase information from at least one signal source;
5 at least one first impedance adjustment device linked between
said at least one signal source and the inputs to at least two of said amplifiers;
and
a plurality of second impedance adjustment devices linked to the
outputs of said amplifiers to combine said outputs into an output of said
10 circuit.
2. The amplifier circuit of claim 1 wherein said circuit is configured
to allow one of said amplifiers to saturate prior to saturation of others of said
amplifiers.
3. The amplifier circuit of claim 2 wherein said signal source further
15 comprises a digital signal processor producing output signals.
4. The amplifier circuit of claim 3 wherein said class E amplifiers
further comprise a first, a second and a third amplifier, said first amplifier
functioning as a carrier amplifier receiving a first amplitude-modulated
baseband signal from said digital signal processor, said second and said third
20 amplifiers receiving a shared amplitude-modulated baseband signal from said
digital signal processor.
5. The amplifier circuit of claim 4 wherein each of said class E
amplifiers is configured to utilize an envelope signal to adjust its individual
output power level.
6. The amplifier circuit of claim 5 wherein said impedance
25 adjustment devices further comprise quarter-wave transformer lines.
7. The circuit of claim 6 further comprising:

a control device for at least one of said amplifiers for receiving amplitude information or phase information from a primary waveform, and a plurality of switching devices in communication with said control device and said at least one amplifier, said switching devices each having a different current resistance;

5 wherein said control device uses said information to select an active switching device to create a secondary waveform for input to the matching network of said at least one amplifier.

8. The circuit of claim 7 wherein said switching devices are transistors each having a gate, and said control device controls said switching devices by providing said information at the gate of said switching device.

9. The circuit of claim 3 further comprising:
a feedback loop for sensing VSWR reflection from an antenna in communication with the outputs of said amplifiers, said feedback loop in communication with said digital signal processor;

15 wherein said digital signal processor adjusts its output signals to correct for said VSWR reflection.

10. The circuit of claim 1 wherein at least two of said amplifiers have different output power ratings.

11. An amplifier circuit comprising:
at least one signal source producing a plurality of digital amplitude modulation signals and a digital phase modulated signal;
a first class E carrier amplifier linked to receive one of said amplitude modulation signals and said phase modulation signal;

25 a first class E peaking amplifier linked to receive another of said amplitude modulation signals, said first peaking amplifier further receiving said phase modulation signal via one or more impedance adjusting devices;
a second class E peaking amplifier linked to receive another of said amplitude modulation signals, said second peaking amplifier further

30

receiving said phase modulation signal via one or more impedance adjusting devices; and

a combining circuit linking the outputs of said amplifiers via one or more impedance adjusting devices.

5 12. The circuit of claim 11 further comprising envelope adjustment circuitry to adjust the power level for each amplifier in said circuit.

13. The circuit of claim 11 wherein said signal source further comprises at least one digital signal processor producing at least one output signal.

10 14. The circuit of claim 11 further comprising means for modulating the input to at least one of said amplifiers.

15 15. The circuit of claim 11 further comprising a third class E peaking amplifier linked to receive another of said amplitude modulation signals, said third peaking amplifier further receiving said phase modulation signal via one or more impedance adjusting devices.

20 16. The circuit of claim 13 further comprising:
a feedback loop for sensing VSWR reflection from an antenna in communication with said amplifiers, said feedback loop in communication with said digital signal processor;
wherein said digital signal processor adjusts said at least one output signal to correct for said VSWR reflection.

17. The circuit of claim 11 wherein said carrier amplifier and said first peaking amplifier have different output power ratings.

25 18. A method of providing high-efficiency signal amplification, said method comprising the steps of:
providing a first digital amplitude waveform to a class E carrier amplifier;

providing a first digital phase waveform to a first class E peaking amplifier;

providing a second digital phase waveform to a second class E peaking amplifier;

5 providing a shared digital phase waveform to said carrier and peaking amplifiers; and

combining the outputs of said carrier and peaking amplifiers via one or more impedance adjusting devices to produce an amplified signal output.

10

19. The method of claim 18 further comprising the step of adjusting the impedance of the shared digital phase waveform via one or more impedance adjustment devices before providing said waveform to said peaking amplifiers.

15

20. The method of claim 19 further comprising the step of providing a third digital phase waveform to a third class E peaking amplifier.

20

21. The method of claim 18 further comprising the steps of:
sensing VSWR reflection from an antenna in communication with said signal output; and
adjusting at least one of said waveforms before providing said waveforms to said carrier and peaking amplifiers to correct for said VSWR reflection.

25

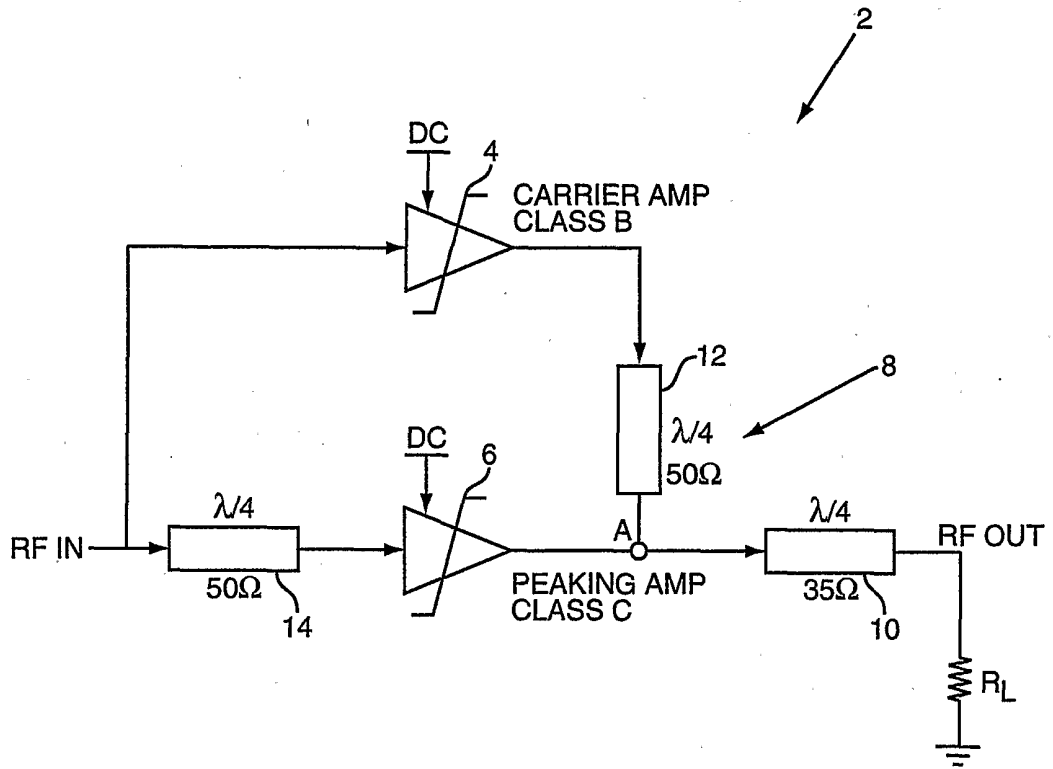


FIG. 1
(PRIOR ART)

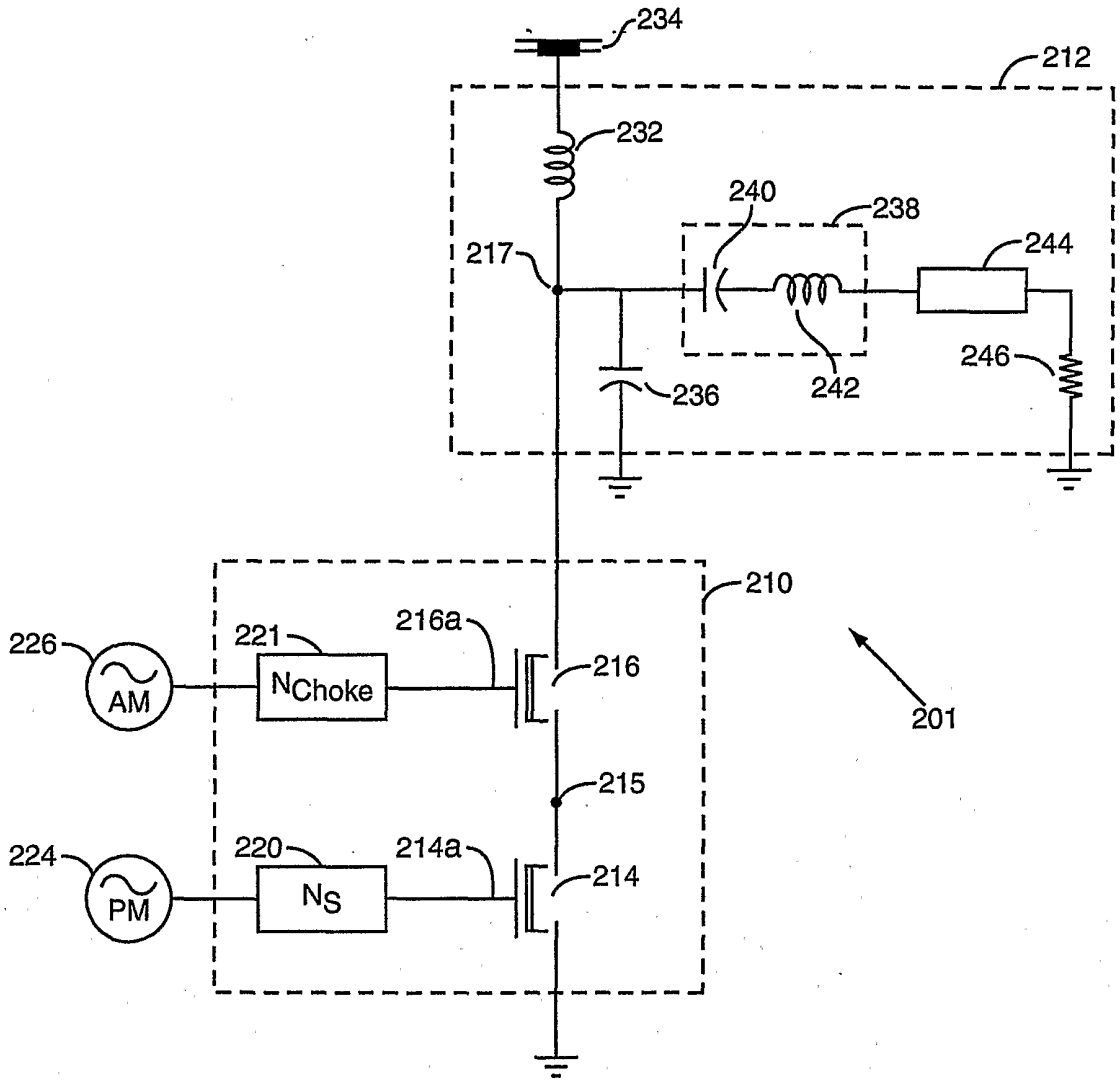
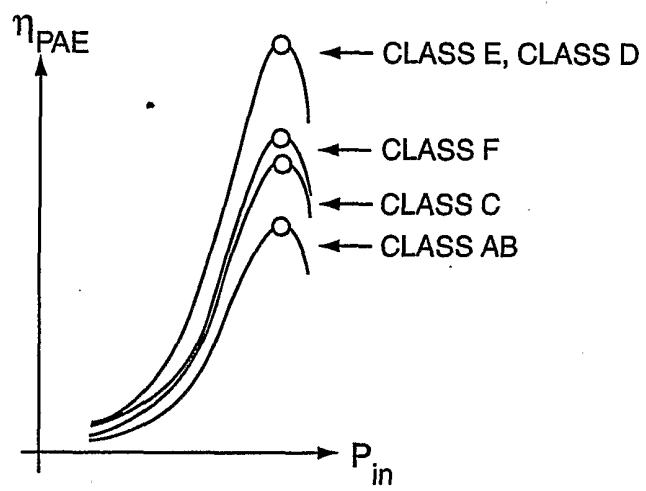


FIG. 2



THEORETICAL PEAK EFFICIENCY OF PA
ACCORDING TO TOPOLOGY

FIG. 3

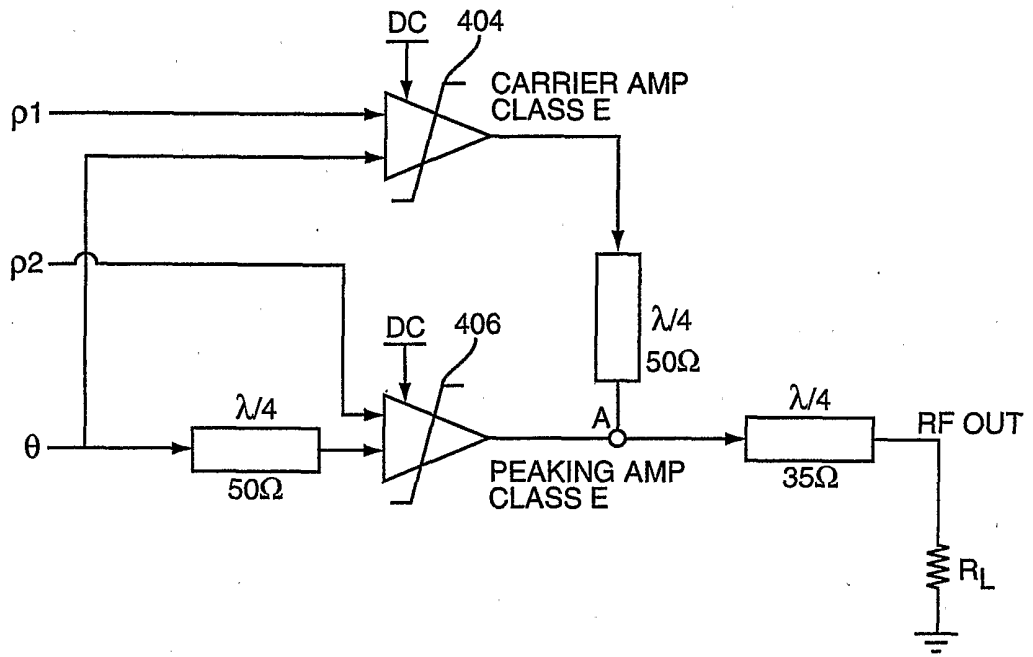


FIG. 4

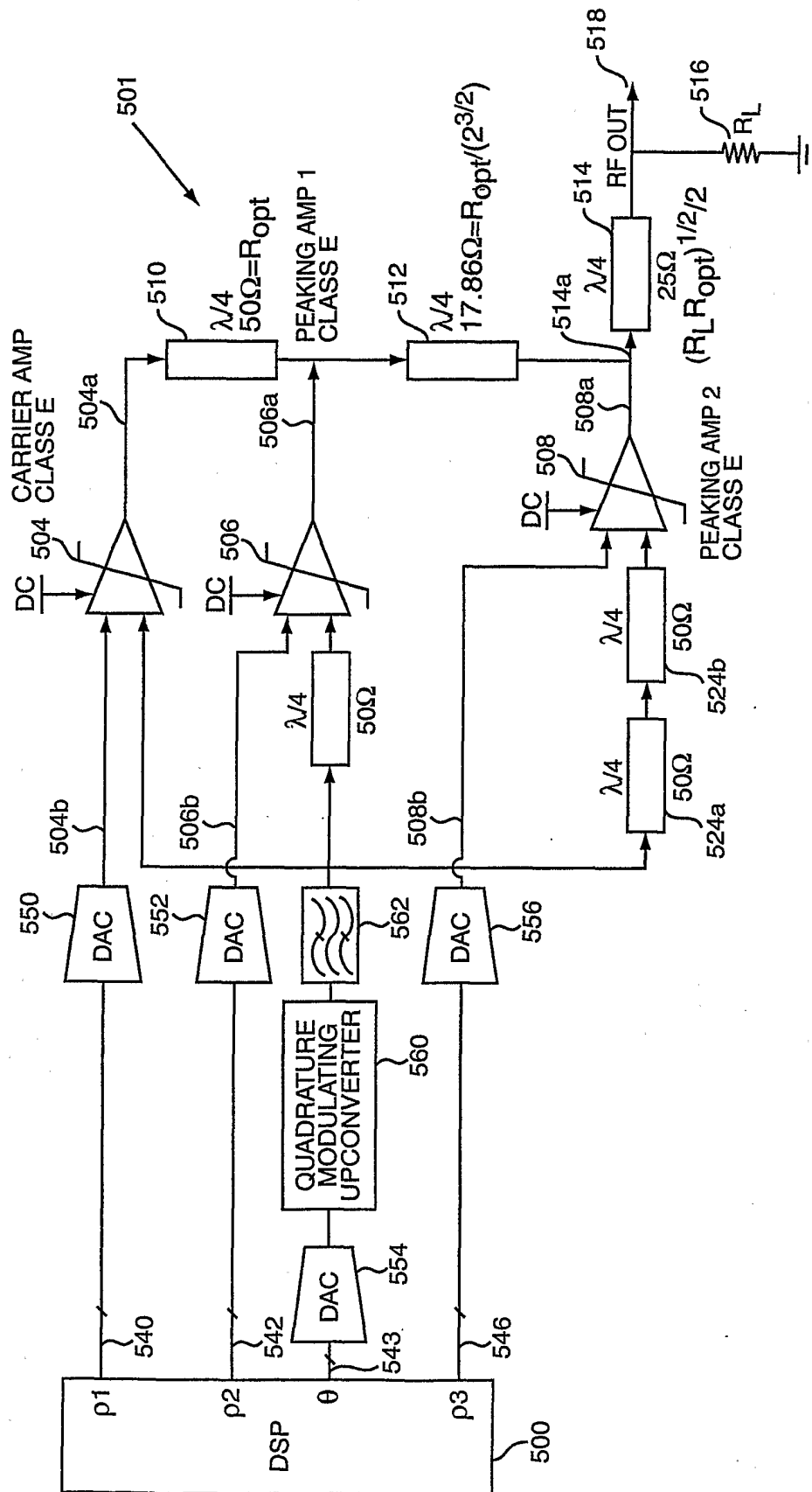


FIG. 5

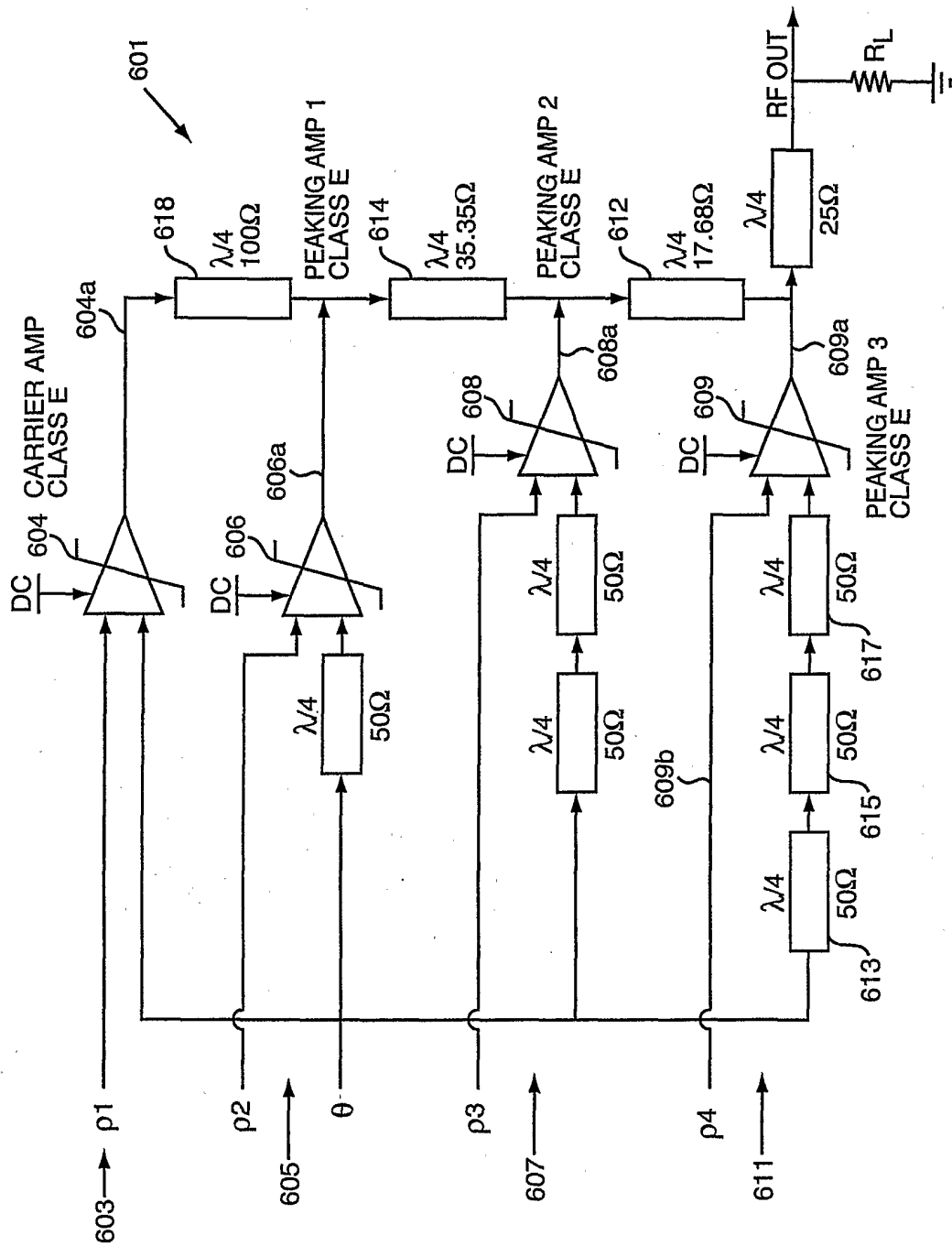


FIG. 6

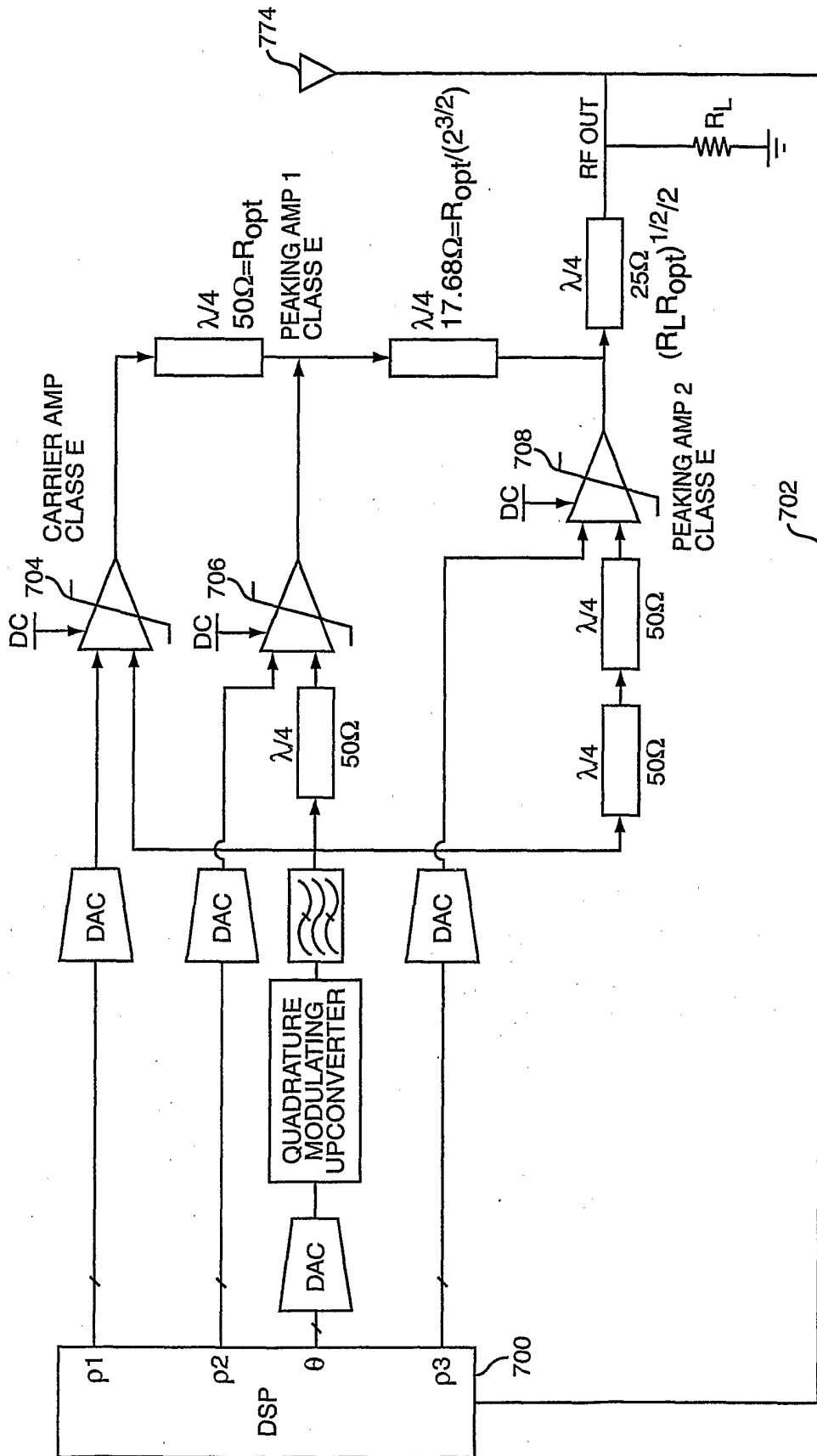


FIG. 7

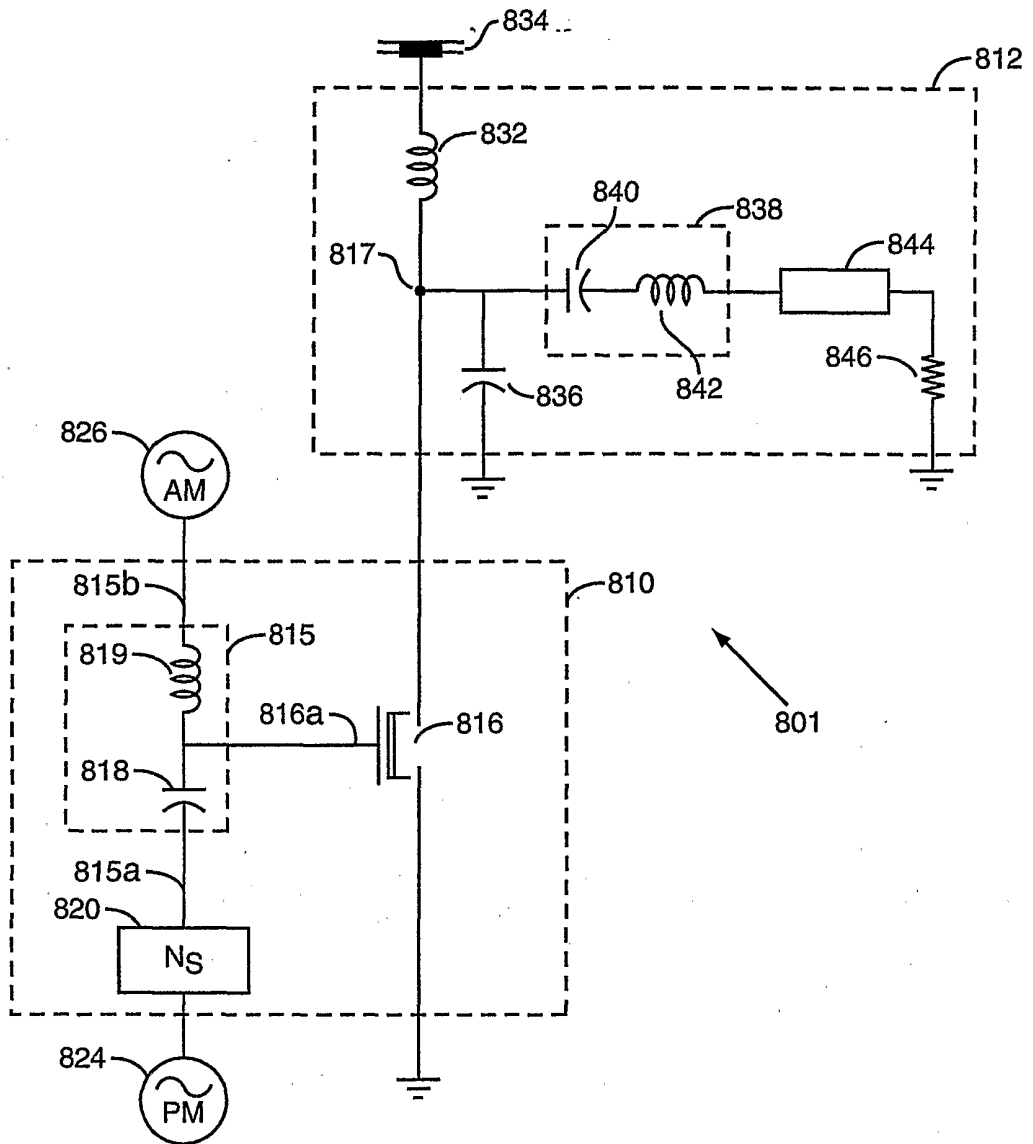


FIG. 8

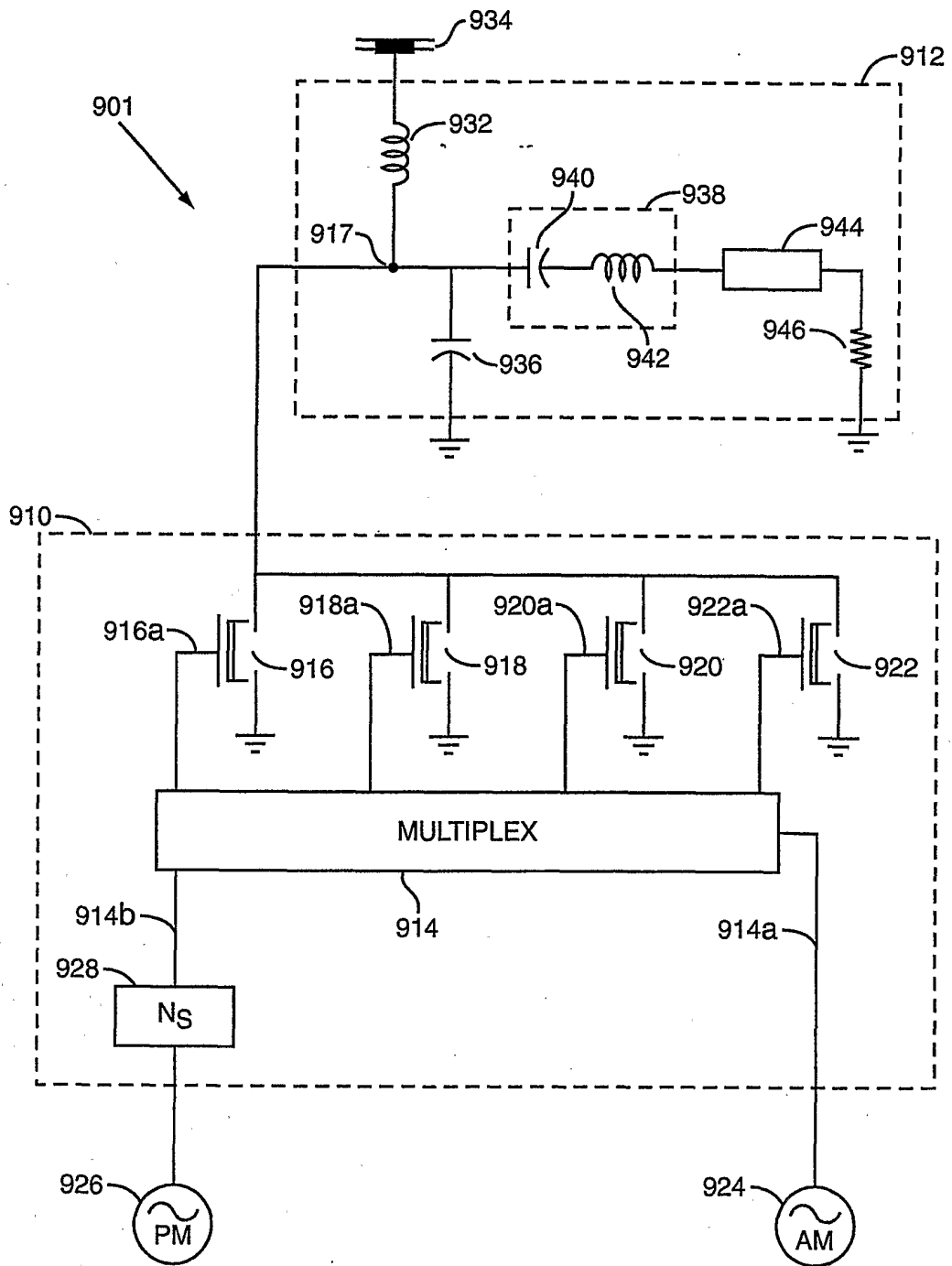


FIG. 9