United States Patent [19]

Cook et al.

[11] **3,882,465**

[45] **May 6, 1975**

[54] **REMOTE CONTROL SYSTEM HAVING COMMAND AND ADDRESS SIGNALS**

[75] Inventors: **Charles W. Cook; James T. Odom,** both of Huntsville, Ala.

[73] Assignee: **Avco Corporation,** Huntsville, Ala.

[22] Filed: **Dec. 5, 1973**

[21] Appl. No.: **421,901**

[52] **U.S. Cl.** ..... **340/147 R;** 340/163

[51] **Int. Cl.** **H04q 9/00**

[58] **Field of Search** ..... 340/147 R, 167 A, 151, 340/152 R, 163, 164 R

[56] **References Cited**

UNITED STATES PATENTS

3,518,628	6/1970	Giel	340/163 X
3,634,824	1/1972	Zinn	340/167 A
3,806,872	4/1974	Odom	340/167 A

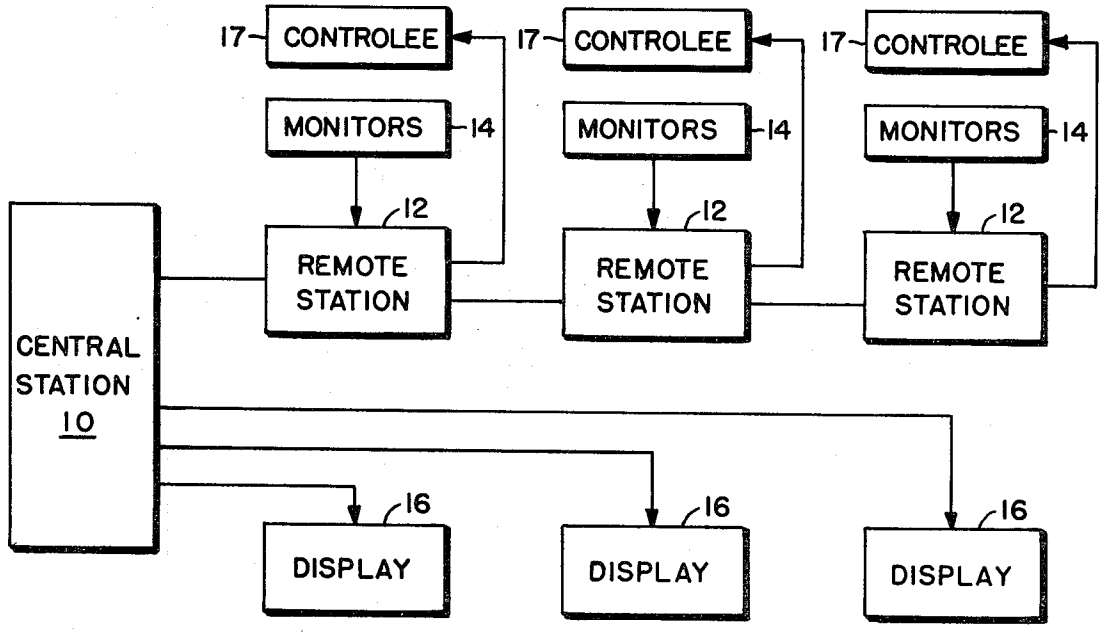
Primary Examiner—Harold I. Pitts

Attorney, Agent, or Firm—Charles M. Hogan; Irwin P. Garfinkle

[57] **ABSTRACT**

A signaling system located at a central station sequentially interrogates a plurality of remotely located transponders. Means are provided for interrupting the normal addressing sequence and for commanding the operation of any one of eight relays at any selected remote station.

12 Claims, 12 Drawing Figures



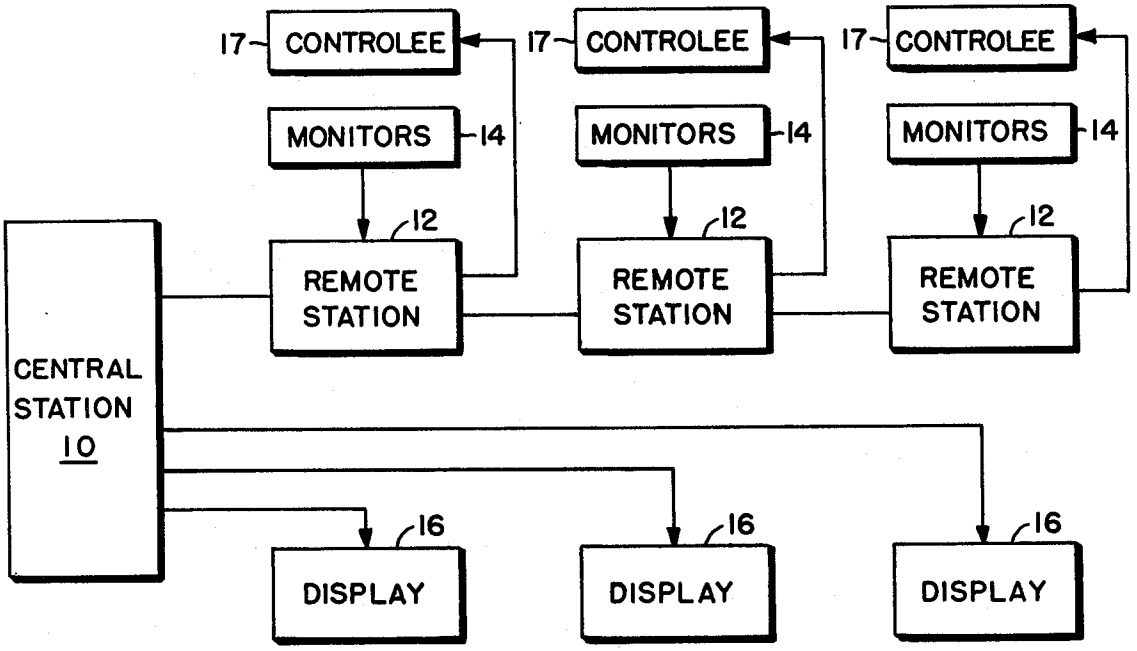


Fig 1

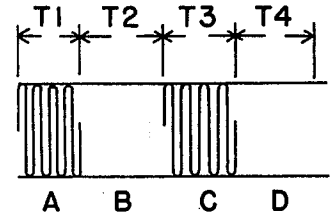


Fig 2a

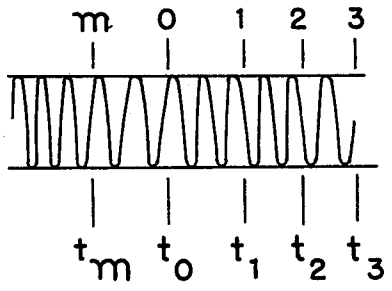


Fig 3

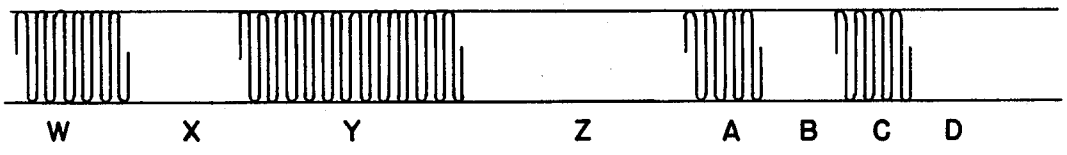


Fig 2b

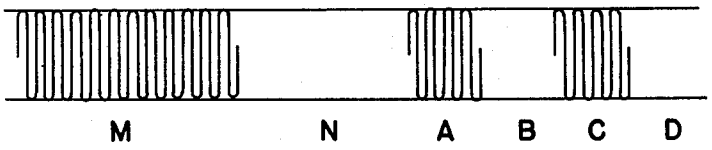


Fig 2c

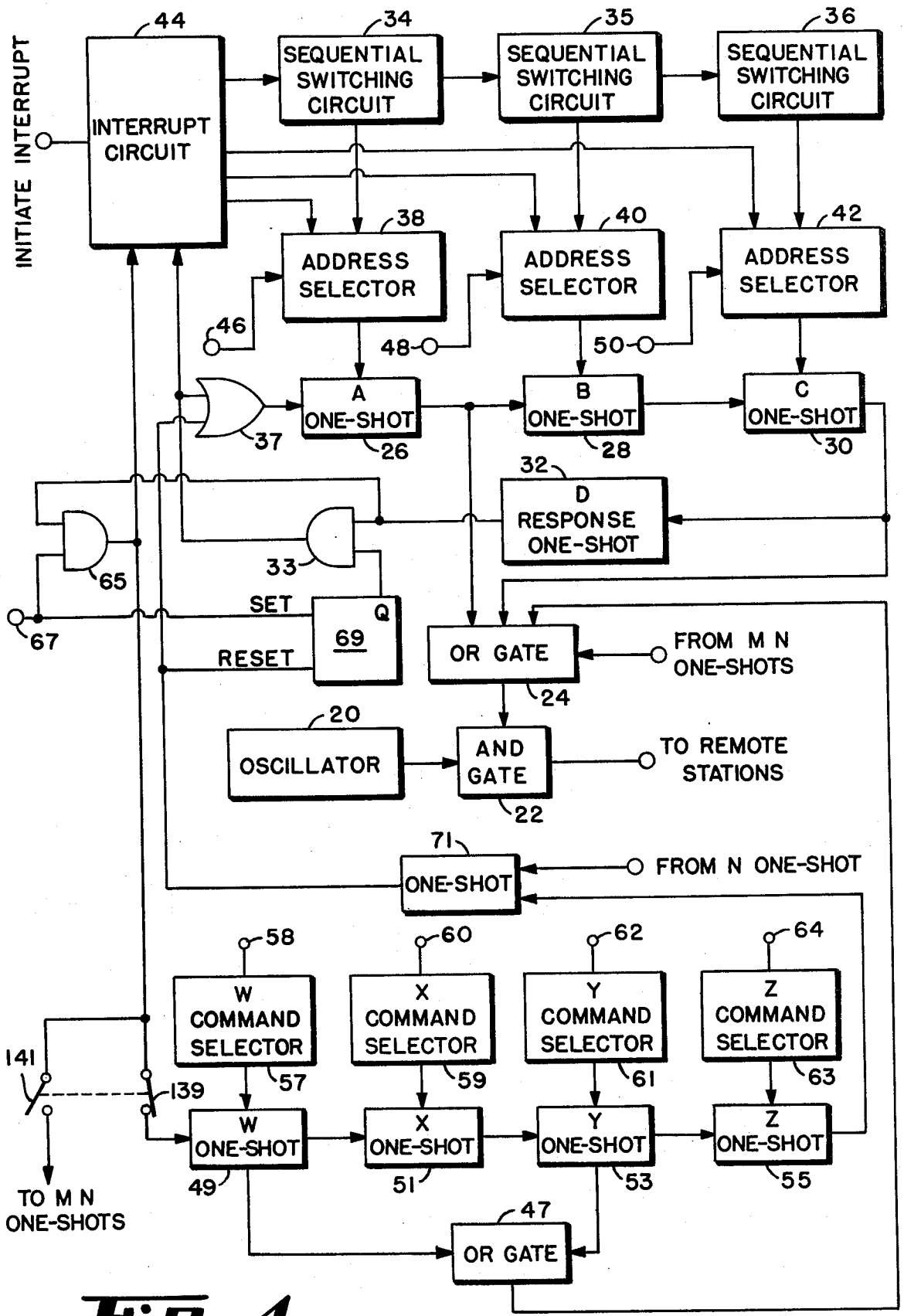

INITIATE INTERRUPT
44
INTERRUPT CIRCUIT
34
SEQUENTIAL SWITCHING CIRCUIT
35
SEQUENTIAL SWITCHING CIRCUIT
36
SEQUENTIAL SWITCHING CIRCUIT
38
ADDRESS SELECTOR
40
ADDRESS SELECTOR
42
ADDRESS SELECTOR
46
48
50
37
A ONE-SHOT
26
B ONE-SHOT
28
C ONE-SHOT
30
32
D RESPONSE ONE-SHOT
65
33
67
SET
RESET
69
Q
OR GATE
FROM M N ONE-SHOTS
24
20
OSCILLATOR
AND GATE
22
TO REMOTE STATIONS
71
ONE-SHOT
FROM N ONE-SHOT
58
60
62
64
W COMMAND SELECTOR
X COMMAND SELECTOR
Y COMMAND SELECTOR
Z COMMAND SELECTOR
57
59
61
63
141
139
W ONE-SHOT
X ONE-SHOT
Y ONE-SHOT
Z ONE-SHOT
49
51
53
55
TO M N ONE-SHOTS
47
OR GATE

Fig 4

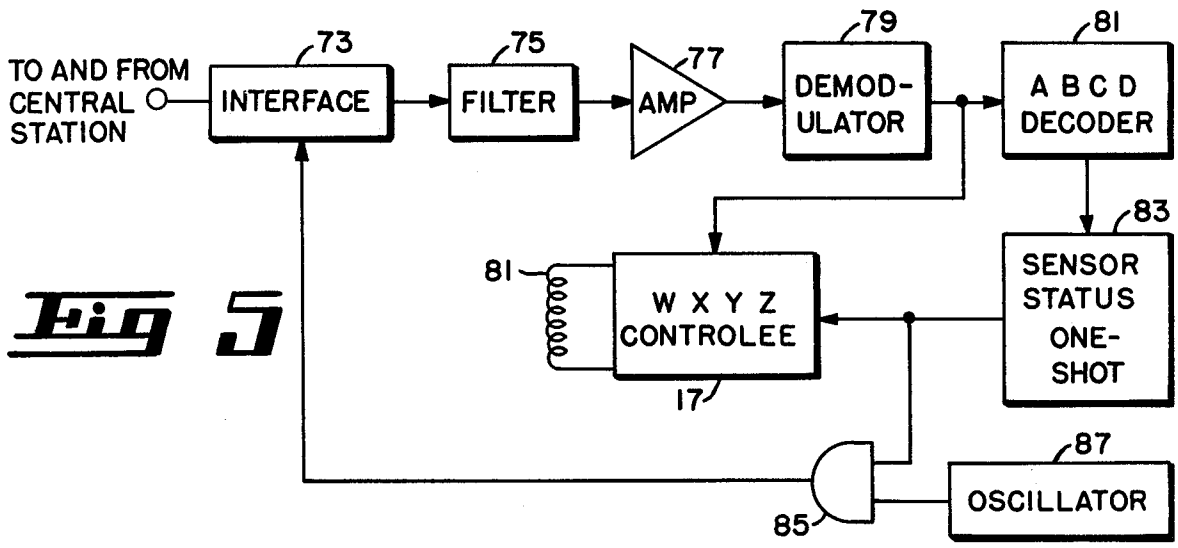

TO AND FROM CENTRAL STATION
73
INTERFACE
75
FILTER
77
AMP
79
DEMOD-ULATOR
81
A B C D DECODER
83
SENSOR STATUS ONE-SHOT
81
W X Y Z CONTROLEE
17
87
OSCILLATOR
85

Fig 5

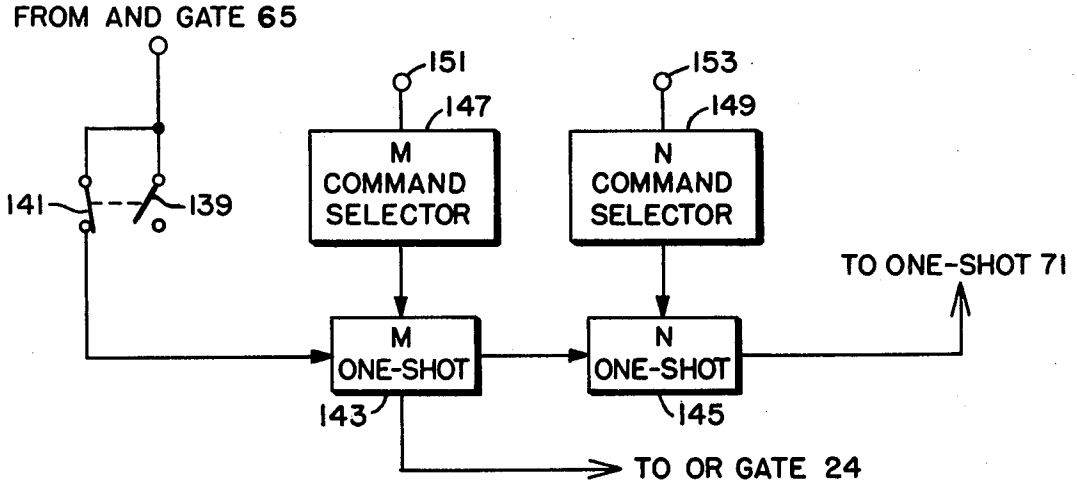

FROM AND GATE 65
151
147
M COMMAND SELECTOR
153
149
N COMMAND SELECTOR
141
139
TO ONE-SHOT 71
M ONE-SHOT
143
N ONE-SHOT
145
TO OR GATE 24

Fig 9

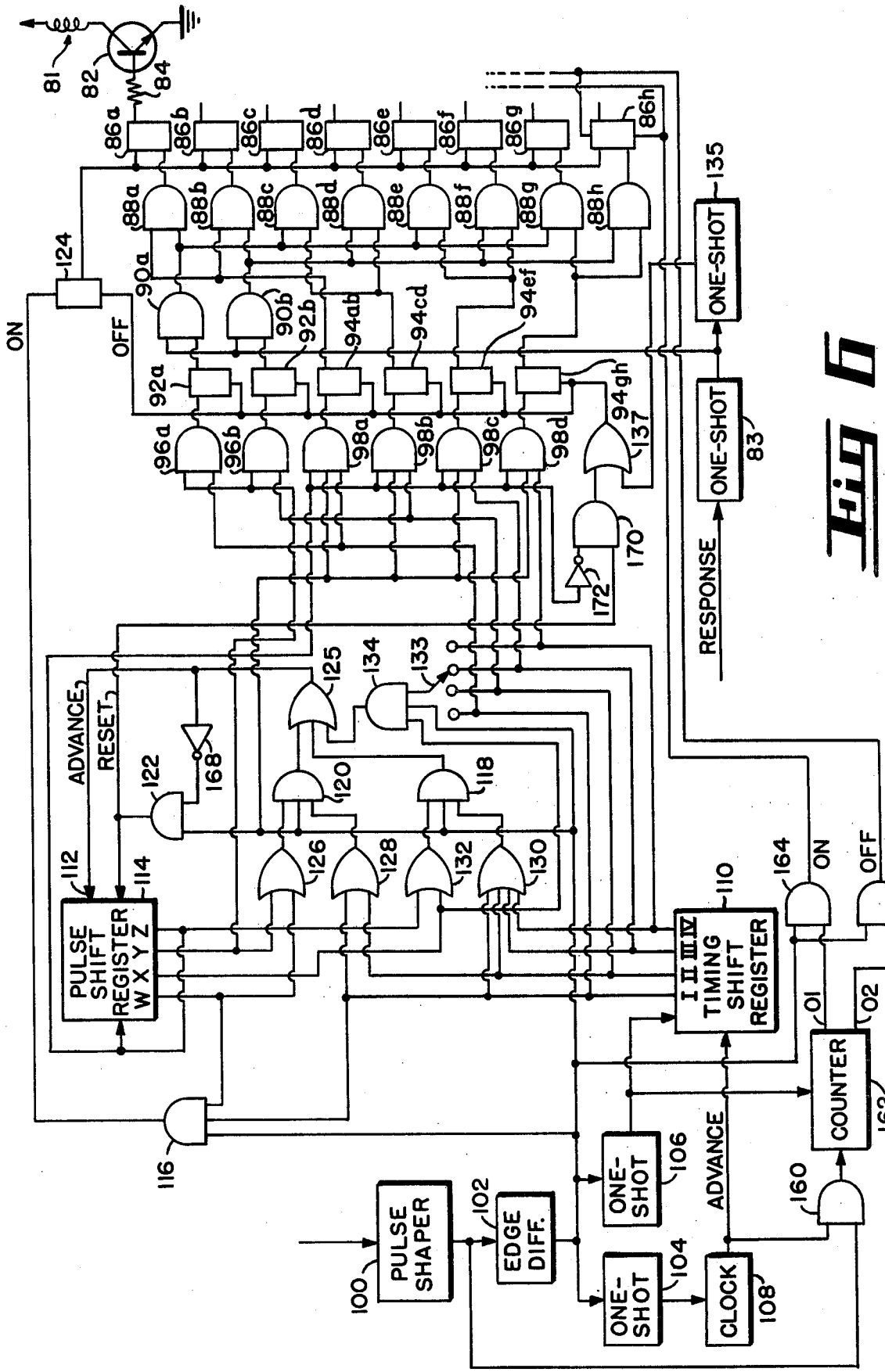

81
82
84
86a
86b
86c
86d
86e
86f
86g
86h
88a
88b
88c
88d
88e
88f
88g
88h
124
ON
OFF
90a
90b
92a
92b
94ab
94cd
94ef
94gh
96a
96b
98a
98b
98c
98d
137
170
172
135
ONE-SHOT
83
ONE-SHOT
RESPONSE
125
134
133
ADVANCE
RESET
122
168
120
118
126
128
132
130
112
114
PULSE SHIFT REGISTER W X Y Z
110
I II III IV TIMING SHIFT REGISTER
164
166
ON
OFF
01
02
COUNTER
162
116
160
ADVANCE
106
ONE-SHOT
104
ONE-SHOT
CLOCK
108
102
EDGE DIFF.
100
PULSE SHAPER

Fig 6

Fig 7

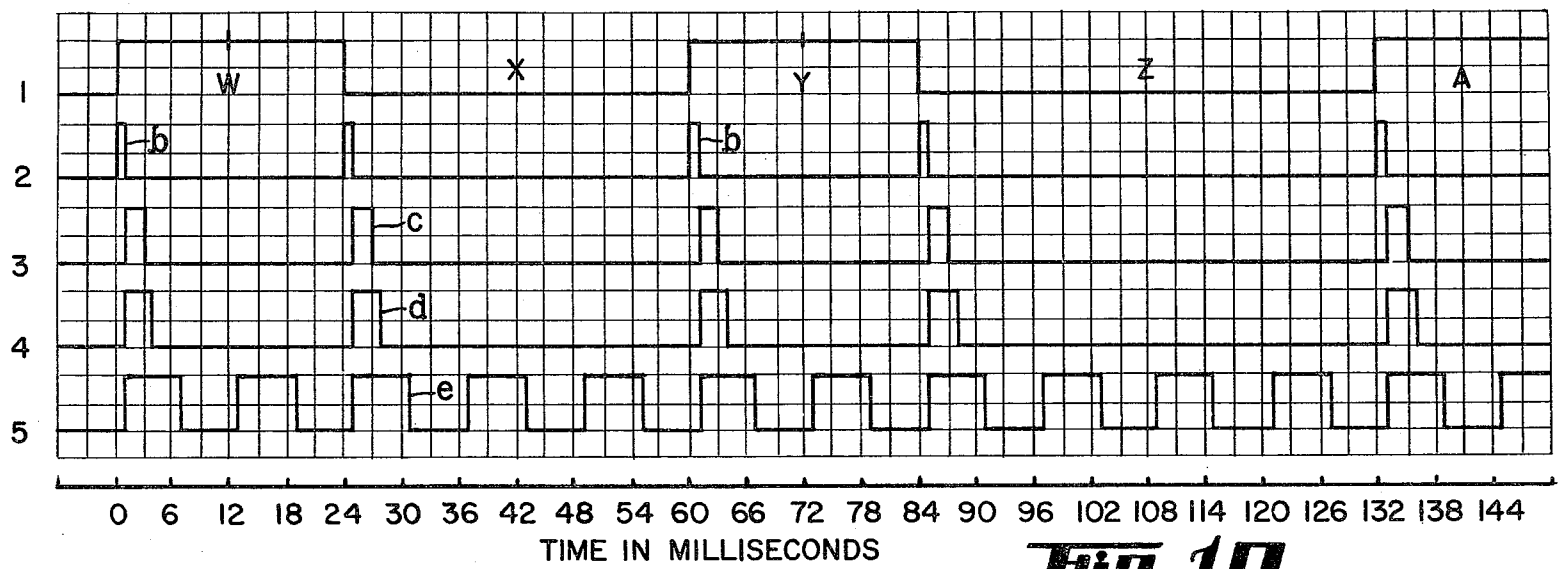


Fig 8

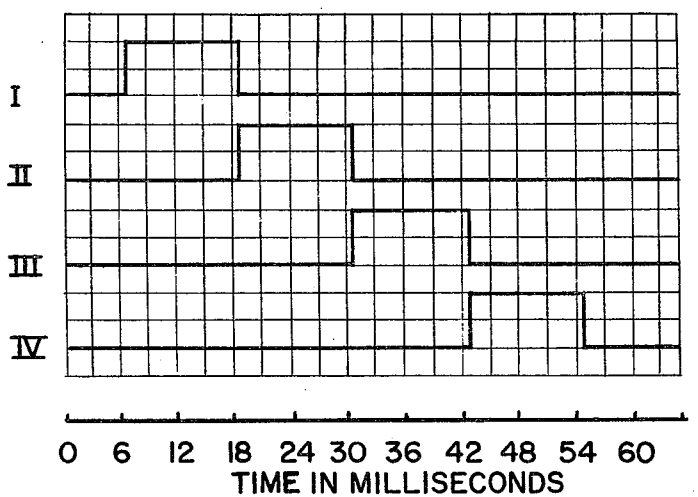
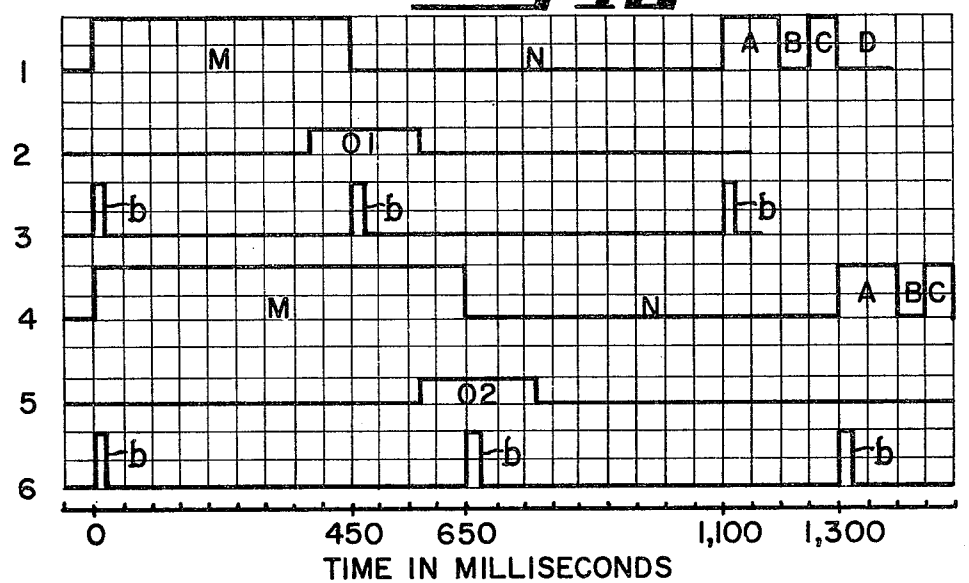


Fig 10



REMOTE CONTROL SYSTEM HAVING COMMAND AND ADDRESS SIGNALS

BACKGROUND OF THE INVENTION

The invention involves a transponder security system of the type disclosed in U.S. Pat. No. 3,634,824 and which includes a signaling system having a plurality of remote stations and a central station. The central station has the capability of interrogating the remote stations in sequence, the addresss of the remote stations being time coded into the interrogating pulse transmissions. This invention provides means for interrupting the normal sequence and then commanding the operation of any one of eight or all relays at a selected station. The invention is an improvement utilizing the teachings of Zinn et al. in U.S. Pat. No. 3,634,824 and of Odom in U.S. Pat. application Ser. No. 358,862.

SUMMARY OF THE INVENTION

This invention provides for the electronic alteration of an address code in a transponder-type security system to remotely control equipment at the transponder location. In a previously existing system an address signal, herein sometimes called the ABCD address, causes a transponder to transmit its existing status back to the central station. This invention provides simple means that permits the performance of various functions at the remote station. This is accomplished by altering the address signal by inserting a command code ahead of it. We sometimes herein refer to the command code as the WXYZ command or the MN command.

The normal ABCD address comprises a burst of pulses A, a space B, a burst of pulses C, and a space D. Similarly, the WXYZ command is made up of a burst of pulses W, a space X, a burst of pulses Y and a space Z, while the MN command is made up of an M pulse and an N space. When demodulated, the various signals are square waves and for convenience are sometimes described as such.

When the transponder or other auxiliary device at a remote location decodes a proper command and when it decodes a proper address, a relay will open or close. The auxiliary device added at the remote transponder is referred to in this specification as a controlee. Each controlee has eight relays associated with it and depending on the command code, any one or all of the eight relays can be energized or some other function can be performed. Four controlees can be selectively controlled. The widths of the pulses and spaces of the address and command codes are chosen such that the command decoder will not be acted on by the ABCD pulses, and the address decoder will not be acted on by WXYZ or MN pulses.

THE DRAWINGS

FIG. 1 is a block diagram showing a transponder system in which the disclosed invention is utilized;

FIGS. 2*a*, 2*b*, and 2*c* are curves showing the nature of the coded transmitted address signal and command signals;

FIG. 3 is a curve showing the nature of the coded transponded signal;

FIG. 4 is a block diagram showing the interrupter system disclosed in Odom application Ser. No. 358,862, and modified for use in accordance with this invention except that for the purpose of simplification, it does not embody the means for generating the MN command;

FIG. 5 is a block diagram showing the transponder with the addition of a controlee;

FIG. 6 is a block diagram of the controlee;

FIG. 7 is a series of curves illustrating the operation of the controlee;

FIG. 8 is a series of curves showing the operation of the timing shift register;

FIG. 9 shows the system for generation of the MN command; and

FIG. 10 is a series of curves showing the operation of the MN command portion of the system.

The overall system is shown schematically in FIG. 1. A central station 10 sends to the remote stations 12 a series of tone pulses which represent the remote station address. Each of the particular remote stations 12 (of which there may be any number within the time capabilities of the system) responds to a particular interrogation by transmitting back to the central station tone pulses of lengths that are determined by the status and changes of status of the respective monitors 14 connected to it. Having received the responses from the remote station, the central station decodes the response, processes the information and displays it in displays 16 in a manner described in U.S. Pat. No. 3,634,824, and in U.S. Pat. application Ser. No. 359,238. In addition each remote station 12 is provided with a controlee 17 which functions, on command from the central station, to perform a pre-wired function, for example, to activate or deactivate a particular monitor equipment.

The addresses of the remote stations are contained in a fixed frequency signal of the type shown in FIG. 2*a*. As shown, the central station transmits a first fixed frequency signal A having a duration T1. This is followed by a space B which occurs for a period T2. The space B is then followed by another signal C of the same fixed frequency and having a time period T3 which is then followed by a space D having a period T4. The address of the remote station is coded into the transmission by varying each of the time periods T1, T2, and T3. The time period T4 is a fixed period during which the remote station transponds. Theoretically the number of addresses may be multiplied by adding additional time periods, all of which may be variable. In a practical system, only the times T1 and T2 were variable to provide a combination of 25 addresses. When a function is to be performed by a controlee 17, the normal address sequence is interrupted, the address signal is delayed, and a WXYZ command signal is transmitted. As shown in FIG. 2*b*, the command signal precedes the address signal.

As indicated in FIG. 1, each of the remote stations may contain a number of monitors 14. Certain of the monitors may, for example, be arranged to detect the opening of a window, the breaking of a window, the walking on a floor, a fire, or the opening of a door. Each of these conditions is given a priority level. As shown in FIG. 3, a remote station transmits a single frequency back to the central station and it will have a duration determined by the highest level alarm that is causing a transmission. The first period t_m of the transmission occurs at every interrogation to give a positive indication that the transponder is operative. A level 0 priority alarm has a duration t_0, a level 1 priority alarm will have a duration t_1, and so forth, so that the highest level alarm signal will dominate all transponded signals. The means for generating an alarm is described in de-

tail in U.S. Pat. application of Odom, Ser. No. 358,862 and is not repeated here.

When an indication appears at the central station that an alarm is being transmitted by the remote station, it is desirable to interrupt the normal sequence, and re-interrogate the station from which an alarm is indicated and then display or otherwise read out the particular cause of the alarm. The block diagram in FIG. 4 shows schematically how the addresses to the remote stations are sequentially coded and transmitted, and also how the normal sequence is interrupted. As will also be seen, the interruption of the normal signal provides the means for delaying the ABCD address and preceding it with a WXYZ command or an MN command.

As shown in FIG. 4, the transmission system includes a fixed frequency oscillator **20** which transmits a signal to the remote stations whenever its associated AND gate **22** is enabled. The AND gate **22** is enabled only when it receives the output from an OR gate **24** in addition to the output signal from the oscillator **20.**

To control the output from the OR gate **24,** and therefore to permit the introduction of the appropriate addresses for the remote stations, a plurality of one-shots **26, 28, 30,** and **32** are connected in series, that is, the one-shots are arranged so that the trailing edge of one triggers the next. It will be noted that the response one-shot **32** is coupled to the one-shot **26** through an AND gate **33** and an OR gate **37.** The output of each of the one-shots is a square wave having a duration determined by the time constants which are set in. The one-shot **32,** referred to as the response one-shot, has a fixed time constant so that the duration T4 of its output remains fixed. The time constants of the one-shots **26, 28,** and **30** are alterable, sequentially or manually, and the durations of the outputs from these one-shots determine the time periods T1, T2 and T3 shown in FIG. 2*a*. These four one-shots provide the ABCD address code.

Under normal conditions, the time constants of the one-shots **26, 28,** and **30** are changed by sequentially and cyclically introducing different values of resistance into their respective R-C circuits. This is accomplished by means of conventional sequential switching circuits **34, 35,** and **36.**

The sequential switching circuits **34, 35,** and **36** have a number of stages, each one of which sequentially connects a different resistor value into a respective one-shot R-C network through an associated address selector circuit **38, 40,** and **42.** The update clock for the sequential switching circuit **34** is the output pulse from the response one-shot **32.** After the last stage of the switching circuit **34** is activated, the next update pulse resets it to the first stage and updates sequential switching circuit **35.** Similarly, the resetting of the sequential switching circuit **35** updates the switching circuit **36.** This means that if there are five stations in each switching circuit, there is a possibility of having **125** different addresses. In a system as reduced to practice, there were five stages in the circuit **34** and five stages in the circuit **35** and only a single stage in the circuit **36,** so that a total of **25** addresses were possible. The particular resistor selected by the switching circuit **34** is connected into the one-shot **26** through address selector **38,** the resistor selected by the circuit **35** is connected to one-shot **28** through the address selector **40,** and the resistor selected by the switching circuit **36** is connected into the one-shot **30** by the address selector **42.** As described in detail in said Odom application, the response one-shot **32** provides the update pulse for the sequential switching circuit **34** through an interrupt circuit **44.** For reasons hereinafter explained, the output from the response one-shot is developed through the AND gate **33.** It is applied to the one-shot **26** through the OR gate **37.**

A particular ABCD address is selected by manually setting certain time constants into the address selectors **38, 40,** and **42** through terminals **46, 48,** and **50** and interrupting the sequencing of the switching circuits **34,** 35, and **36.** As explained in detail in the Odom application, a preselected resistor establishes the time constants of the one-shots **26, 28,** and **30** to code the selected address for transmission.

To transmit a command to a selected address, this invention provides for the delay of the ABCD address signal and for the insertion of a WXYZ command. The same oscillator **20,** AND gate **22,** and OR gate **24** used to generate the ABCD address are also used to generate the WXYZ command. However, for the purpose of generating the command, the OR gate **24** is also controlled by a series of one-shots **49, 51, 53,** and **55.** The output of one-shot **49** provides the W pulse which is applied to the OR gate **24** through OR gate **47.** The one-shot **51** provides the X space. The one-shot **53** provides the Y pulse which is applied to the AND gate **22** through the OR gates **47** and **24.** The one-shot **55** provides the Z space. The time constant for each of the one-shots **49, 51, 53,** and **55** is provided, respectively, by command selectors **57, 59, 61,** and **63,** the particular command being set in at the terminals **58, 60, 62,** and **64.** The command system operates in the same manner as the address system, that is to say, the output of each of the one-shots is a square wave having a duration determined by the time constants which are set in and each is connected in series, that is, they are arranged so that the trailing edge of one triggers the next.

As previously noted, the ABCD address is delayed so that the WXYZ command can be inserted ahead of it. For this purpose we provide an AND gate **65** having an input terminal **67** to which an initiate command is applied in the form of a direct voltage. The second input terminal of AND gate **65** is supplied with the output of the response one-shot **32.**

The initiate command pulse is also applied to a latch **69,** the Q output of which is normally a logical 1. Upon the application of the initiate command pulse to the set input terminal of latch **69,** the Q output terminal of the latch **69** is changed to a logical 0. No output can then be developed from the AND gate **33** when it receives the next output pulse from the response one-shot **32.** When the AND gate **33** has a logical 0 at one of its input terminals, the output from the response one-shot **32** cannot update the one-shot **26,** so that any address which has been inserted into the address selectors **38,** 40, and **42** cannot be transmitted.

Since the output pulse of the response one-shot **32** is also applied to the second input terminal of the AND gate **65,** an output pulse is developed at the output terminal of the AND gate **65.** This pulse is applied to the interrupt circuit **44** so that the normal address switching is interrupted. The same pulse is also applied to the W one-shot **49** so that a WXYZ command signal is initiated and transmitted from the oscillator **20** through the AND gate **22** to the remote stations.

The trailing edge of the output of the Z one-shot **55** triggers a one-shot **71** which is connected to the reset terminal of latch **69**, thereby re-establishing a logical 1 at the Q output and in addition is applied through the OR gate **37** to the one-shot **26** to begin the cycling of the address one-shots **26, 28, 30,** and **32.** Upon the completion of that cycle the response one-shot recycles the system through the normal sequence switching cycles.

The operation of the remote stations is shown generally in FIG. **5.** The signal from the central station is applied from the telephone lines through an interface **73,** and filter **75** and an amplifier **77.** The signal from amplifier **77** comprises the series of pulses shown in FIG. **2***a* if no command is given or in FIG. **2***b* if a command is included. The signal is then applied to a demodulator **79,** the output of which is a square wave of the envelope of the curves shown in FIGS. **2***a* or **2***b*. In the absence of the WXYZ command signal, the decoder **81** serves to decode the ABCD address signal, and as described in the aforesaid Odom application, enables the generation of an output pulse from status one-shots **83.** The outputs from the status one-shots **83** will be a pulse having a duration depending upon the status of the various sensor inputs applied to the various input terminals **0, 1, 2,** and *n*. This pulse provides one input to an AND gate **85,** the other input of which is supplied by an oscillator **87.** The output from the AND gate **85** is therefore a burst of pulses having a duration representing the level of the sensor which is providing an input for transmission back to the central station through the interface **73.** If an WXYZ command appears in the output of the demodulator **79,** then it is decoded ahead of the ABCD address in the controlee **17** to control the energiation of any of a group of eight relays **81.**

The controlee for selectively operating any one or all of eight relays is shown in FIG. **6.** Each of the relays **81** is represented as a relay coil **81** in the collector-emitter circuit of a transistor **82,** the base of which is biased by a binary voltage applied through a resistor **84.** While only one relay coil and transistor is shown, it will be understood that eight such sets are provided, one connected to each of a group of eight flip-flops **86***a–h*. The relays are turned on or off by selectively setting or resetting any one or all eight of the flip-flops **86***a–h*.

The flip-flops **86***a–h* are selectively set by the outputs from a set of AND gates **88***a–h*. When a particular AND gate **88***a–h* is enabled, a respective flip-flop changes state to energize or de-energize a relay.

A second set of AND gates **90***a* and **90***b* are each used to enable half of the AND gates **88***a–h*. That is to say, when the AND gate **90***a* is enabled, a logical 1 is applied to one input terminal of each of the AND gates **88***a, c, e,* and *g*, and when the AND gate **90***b* is enabled, a logical 1 is applied to one of the input terminals of each of the AND gates **88***b, d, f,* and *h*.

The AND gates **90***a* and **90***b* are enabled by two inputs, one from the outputs of flip-flops **92***a* and **92***b*, respectively, the other from the output of a one-shot **83** (also see FIG. **5**). If the AND gate **90***a* is enabled, then each of the four AND gates **88***a, c, e,* and *g* has a logical 1 on one of its inputs. One of those four is selected by the flip-flops **94***ab*, **94***cd*, **94***ef*, or **94***gh*. For example, if a logical 1 is developed on the output of **94***ab* at the same time that a logical 1 is developed at the output of AND gate **90***a*, the AND gate **88***a* will be enabled and the flip-flop **86***a* will change state. On the other hand, if the flip-flop **92***b* changed state, the AND gate **90***b* would be enabled by the output of the one-shot **83** and hence the AND gates **88***b, d, f,* and *h* would be enabled, depending on the status of the four flip-flops **94***ab* to *gh*.

The logic of the WXYZ code as applied to this system is as follows: Every W pulse has a duration of one or two time units. Every X space has a duration of 1, 2, 3, or 4 time units. Every Y pulse has a duration of one or two time units, and every Z pulse has a duration of 1, 2, 3, or 4 time units. In a practical system each unit of time was equal to 12 milliseconds, and for purposes of convenience that duration will be discussed in the following examples.

The purpose of the W pulse is to arrange the logic of the flip-flops **86***a–h* so that on completion of the command, a relay which is on can be turned off, or a relay which is off can be turned on. The purpose of the X space is to select one of four controlees, in this case controlee No. **3.** The purpose of the Y pulse is to enable either an AND gate **96***a* or an AND gate **96***b*, depending on the duration of the Y pulse. The AND gates **96***a* and **96***b* set either the flip-flop **92***a* or **92***b* which in turn enables AND gates **90***a* or **90***b* to supply a logical 1 to four of the gates **88***a–h*. The purpose of the Z pulse is to select a particular one of the four.

The received WXYZ command and ABCD address are applied to a pulse shaper **100.** The wave train envelope at the output of pulse shaper **100** of the transmitted pulses is developed, as shown in FIG. **7.** The output of the pulse shaper **100** is then applied to an edge differentiator **102** which develops a series of leading and trailing edge pulses *b*. The pulses *b* provide the logic for the operation of the gates.

The pulses *b* are applied to one-shots **104** and **106** which develop output pulses *c* and *d*. The output pulses *c* are supplied to a clock **108** which is designed to operate at a **12** millisecond rate; i.e., the clock generates a 6-millisecond pulse followed by a 6-millisecond space (pulse *e*, FIG. **7**). The pulses *c* serve to synchronize the operation of the clock with the WXYZ command. The pulses *e* are used to advance a timing shift register **110.** The pulses *d* from the one-shot **106** are used for resetting the timing shift register **110.**

The timing shift register **110** contains conventional binary circuits which serve to generate sequential output timing pulses I, II, III, and IV (see FIG. **8**) at the output of its stages **1, 2, 3,** and **4,** respectively. Each positive going timing pulse *e* lasts 6 milliseconds. The pulse at output terminal **1** occurs 6 milliseconds after reset by pulse *d*. The pulses II, III, and IV sequentially follow the pulse I. For example, in the illustrated WXYZ command, the W pulse is 24 milliseconds, and therefore a 12-millisecond output pulse will be developed at terminal **1** and then at terminal **2.** Further, since space X is 48 milliseconds, 12-millisecond output pulses will be developed sequentially at terminals **1, 2,** 3, and **4,** the pulse I extending from 6–18 milliseconds, the pulse II from 18–30 milliseconds, the pulse III from 30–42 milliseconds, and the pulse IV from 42–54 milliseconds. (The times above stated ignore the width of the *b* pulses.)

The output pulses *b* from the edge differentiator **102** are also applied through a series of gates (to be described) to the input terminal **112** of a pulse shift register **114.** Initially (i.e., after reset) the pulse shift register has an output at stage W. Each pulse *b* applied to the

input terminal **112** advances the pulse shift register **114** once. Since the pulses *b* represent the beginnings and ends of the WXYZ command, a logical 1 will appear at the W stage during the generation of the W pulse, a logical 1 will appear at the X stage during the generation of the X space, a logical 1 will appear at the Y stage during the generation of a Y pulse, and a logical 1 will appear at the Z stage during the generation of the Z space. The end of the Z space (the beginning of the ABCD address) serves to reset the register **114** to its W stage.

To describe the system of gates and the relationship between the timing shift register **110** and the pulse shift register **114,** we will assume particular WXYZ commands. First, let us assume that a W pulse is one unit in width, or 12 milliseconds. In such a case the output pulses *b* from the edge differentiator **102** will provide a logical 1 to an input terminal of several AND gates **118, 120, 122** and **134.**

The AND gate **116** will be enabled only if its two other input terminals are provided with logical 1's. One of the input terminals will have a logical 1 if the timing shift register has a logical 1 at its first terminal. Such a condition will occur if the trailing edge of the W pulse occurs 12 milliseconds after the leading edge. The other terminal will be provided with an enabling pulse from the W stage of the pulse shift register if the register has not otherwise been advanced. This means that if the W pulse is 12 milliseconds long, the AND gate **116** will be enabled and it will provide an output pulse to the "on" terminal of a flip-flop **124** causing the flip-flop **124** to change state, enabling the flip-flops **86***a–h* so that the pulse output of one of the gates **88***a–h* can turn one of the relays **81** on, if it has been off.

Assume now that the W pulse is 24 milliseconds, or 2 units long. As before, the pulse *b* occurring at the trailing edge of the W pulse provides a logical 1 for one input of AND gate **116.** In addition, since the pulse shift register **114** is in its initial W state, the gate **116** is provided with a second logical 1. However, since the W pulse is 24 milliseconds long, the timing shift register **110** will have been advanced to its second output terminal so that the third input terminal of AND gate **116** is not enabled, and an output pulse is not developed from the AND gate **116.** This means that the flip-flop **124** remains in its initial state, and therefore the next enabling pulses to one of the gates **88***a–h* will serve to turn a particular relay off, if it has been on.

The pulse *b* occurring at the trailing edge of the W pulse is applied to an AND gate **120.** If AND gate **120** is otherwise enabled, then it develops an output pulse through an OR gate **125** which supplies a pulse to the input terminal **112** and advances the shift register **114** to the X stage. The AND gate **120** is enabled at one of its input terminals through an OR gate **126** with logical 1 existing at the W stage of the pulse shift register **114.** Another terminal of the AND gate **120** is enabled through the OR gate **128** with the logical 1 output of the first stage (if the W pulse is one unit) or the second state (if the W pulse is two units) of the timing shift register **110.** Thus, upon the occurrence of the pulse *b* at the trailing edge of the W pulse, the pulse shift register **114** is advanced to the X stage. The pulse *c* generated at the trailing edge of the W pulse resets the timing shift register to **0.**

Next assume that the X space is **36** milliseconds. (It could also be **12, 14,** or **48** milliseconds, but this illustrated system can only decode an X pulse if it is 36 milliseconds, because the switch **133** is connected to stage **3** of the timing shift register.) A 36-millisecond X space will cause the timing shift register **110** to advance to its third stage and a logical 1 is applied through the switch **133** to one input terminal of the AND gate **134.** The second terminal of the AND gate **134** is connected directly with the logical 1 output from the X stage of the pulse shift register **114.** Therefore, the pulse *b* occurring at the leading edge of the pulse Y passes through the enabled AND gate **134** and the OR gate **124** to the input terminal **112** of the pulse shift register **114,** thereby advancing the pulse shift register to the Y stage. The output pulse *c* occurring at the leading edge of the Y pulses resets the timing shift register to **0** so that the system is now ready to analyze the Y pulse. (Note that with the switch **133** rotated to connect to any other stage of register **110,** it could not have decoded a 36-millisecond X space.)

Now assume that the Y pulse is **24** milliseconds. The clock **108** advances the timing shift register **110** to its second stage from which a logical 1 is supplied to one input terminal of AND gate **96***b*. Moreover, the logical 1 appearing at the Y stage of the pulse shift register **114** is also applied to the AND gate **96***a*. Thus, AND gate **96***b* is enabled to change the state of the flip-flop **92***b* to provide a logical 1 output for one input terminal of the AND gate **90***b*. Had the W pulse been 12 milliseconds, the AND gate **96***a* would have been enabled and the flip-flop **92***a* would have changed state to provide a logical 1 for the AND gate **90***a*.

The logical 1 at the second stage of the timing shift register **110** is also supplied through the OR gate **128** to one terminal of the AND gate **120.** A second terminal of the AND gate **120** is supplied through the OR gate **126** with the logical 1 from the Y stage of the pulse shift register **114.** The pulse *b* occurring at the trailing edge of the Y pulse passes through the AND gate **120** and the OR gate **125** to the input terminal **112** of the pulse shift register **114** so that the register is advanced to its Z stage. At the same time the *c* pulse resets the timing shift register **110** to **0** and the system is now prepared to analyze the Z space.

Now if the Z pulse is 48 milliseconds (it could also be 12, 24, or 36 milliseconds), a logical 1 appears at the fourth stage of the timing shift register **110** and a logical 1 is supplied through the OR gate **130** to one input of the AND gate **118.** Moreover, the logical 1 at the Z stage of the pulse shift register **114** is applied through OR gate **132** to a second input terminal of AND gate **118.** The Z output stage also supplies a logical 1 to one terminal of each of the AND gates **98***a–d*. A second terminal of each of the AND gates **98***a–d* is also supplied with the logical *b*'s, pulses I, II, III, and IV appearing sequentially at each of the stages of timing shift register **110.** The occurrence of a pulse *b* at the end of the Z space coincides with pulse IV and therefore the leading edge of the ABCD address passes through both the AND gate **118** and the AND gate **98***d*. This changes the state of flip-flop **94***gh* to provide a logical 1 for one terminal of AND gate **88***h*. It also advances the pulse shift register **114** to its W stage.

Now, upon the occurrence of a response from a proper ABCD address, as described in detail in the Odom application, a response pulse is generated in the one-shot **83.** This pulse passes through AND gate **90***b* and **88***h* to change the state of flip-flop **86***h* and turn its

associated relay on or off. Following the pulse from the one-shot **83**, a second one-shot pulse is generated by a one-shot **135**. This pulse is applied through an OR gate **137** to the off terminal of the flip-flop **124**, which is now ready for a new command.

The MN command serves to turn one or all of the relays on each controlee on or off simultaneously. FIG. **9** when added to FIG. **4** shows the means for generating the MN command pulse. As shown, the system incorporates two switches **139** and **141** which selectively connect the "initiate command" pulse at terminal **67** through the AND gate **65** to either the WXYZ one-shots, or the MN one-shots. With the switches **139** and **141** in the position shown in FIG. **4**, the OR gate **24** is controlled by the WXYZ one-shots **49, 51, 53,** and **55**. With the switches in the position shown in FIG. **9**, the OR gate **24** is controlled by MN one-shots **143** and **145**.

The output of the one-shot **143** provides the M pulse which is applied directly to OR gate **24**. The one-shot **145** provides the N space which is applied to one-shot **71**. The time constant for the one-shots **143** and **145** is provided, respectively, by command selector **147** and **149**, the particular command being set in at terminals **151** and **153**. The output of each of the one-shots is a square wave having a duration determined by the time constants which are set in and the trailing edge of the M pulse from the one-shot **143** triggers the N one-shot **145**. The MN command then functions in the same manner as WXYZ command, and is transmitted to the remote stations ahead of the ABCD address. However, the controlee is independent of the ABCD address, and the relays operate independently of a response to an address code.

The M pulse may have one or two widths, for example 450 and 650 milliseconds. If it is 450 milliseconds, it may be used to close one or more of the relays **81**, and it will also close similar relays of other controlees. If it is 650 milliseconds, it is used to open each of the relays **81**. The N space is 650 milliseconds. While these particular times were used in a practical application of the invention, it will be recognized that other times may also be used so long as they do not provide a conflict with the WXYZ pulses or with the ABCD pulses.

The MN pulses are ahead of the delayed ABCD pulses and are applied to the pulse shapers **100** at the remote stations (see FIG. **6**). The square wave output of the pulse shaper **100** (see the curves **1** and **2** in FIG. **10**) is applied to one input of an AND gate **160**, the other input of which is supplied with the 6-millisecond pulses of the clock **108**. The output from the AND gate **160** is applied to a counter **162**. The counter **162** has two output stages **01** and **02**. The logic of the counter is such that a logical 0 is on its output terminal **01** except during the time interval from 384–576 milliseconds when it is a logical 1 (see curve 2 in FIG. **10**). Similarly, a logical 0 is at the output terminal **02** except during the interval from 577–768 milliseconds (see curve 5 in FIG. **10**). The output at stage **01** is applied to AND gate **164** while the output at stage **02** is applied to AND gate **166**.

The output from the pulse shaper **100** is also applied to the edge differentiator **102** which, as before, produces pulses *b* at the leading and trailing edges of the M and N pulses (see curves 3 and 6 in FIG. **10**). The pulses *b* are applied to both AND gates **164** and **166**. If a pulse *b* occurs when a logical 1 is present at output stage **01**, an on pulse is gated through AND gate **164** to one or more of the flip-flops **86***a–h*. If a *b* pulse occurs when a logical 1 is present at stage **02**, then an "off" pulse is applied through the AND gate **166** to one or more of the flip-flops **86***a–h*. Note that while only one such flip-flop **86***h* is shown connected to the on-off lines, the invention contemplates the connection of one or more of the flip-flops **86***a–h* across such lines so that all of the relays **81** may be turned on or off simultaneously.

The MN pulses generated for the purpose of turning all the relays on or off are not decoded in the WXYZ decoder, since the pulses *b* do not occur at the programmed times and the WXYZ decoder is automatically reset without activating any of the relays **81**. Upon the generation of the first pulse *b*, the pulse shift register is at its W stage and it cannot be shifted until the end of the M pulse when a second pulse *b* is generated. Since the logic of the WXYZ decoder is such that a W pulse must occur within 24 milliseconds, this means that there will be no logical 1 in the timing shift register that will be applied to either of the OR gates **128** and **130**, and therefore no advance pulse can be developed for the pulse shift register **114**. The absence of an advance pulse means there will be a logical 0 at the input of an inverter **168**, and the output of the inverter **168** supplies a logical 1 to the input of AND gate **122**. The occurrence of pulse *b* when applied to the other input of AND gate **122** develops a reset pulse for the pulse shift register so that the system is returned to its initial state (or maintained in its original state) if the timing of the WXYZ pulses is not as programmed.

Reset also occurs after a proper decoding and response. The same reset pulse applied to the pulse shift register is also applied to one input of an AND gate **170**. The other input of an AND gate **170** is supplied through an inverter **172** with the output from the Z state of the pulse shift register **114**. If the Z state is at logical 0, a logical 1 is therefore applied to the AND gate **170** through the inverter **172** and the occurrence of a reset pulse from the AND gate **122** is then applied through the OR gate **137** to the off input terminal of flip-flop **124**.

We claim:

1. In a signaling system having a central station and a plurality of remote transponding stations, the combination comprising:

signal transmitting means at said central station for transmitting coded address signal to said remote stations;

an address decoder at each of said remote stations for decoding a particular one of said coded address signals;

means responsive to the decoding of a particular one of said address signals for generating a response signal to said central station;

command means at said central station for transmitting a coded command signal ahead of a selected address signal;

a command decoder at each of said remote stations for decoding said command signals; and

means responsive to the decoding of said command signals and the generation of said response signal for generating a response to said command signal.

2. The invention as defined in claim **1** wherein said signal transmitting means transmits said coded address signals in a preestablished sequence; and

wherein said command transmitting means includes means for interrupting and delaying said sequence until the transmission of said command signal and a selected address signal are completed.

3. The invention as defined in claim **2** wherein said address and command signals are duration coded pulses, said command decoder comprising a plurality of gates, said plurality being equal to the number of command signals, said gates each having an output connected to a respective load and having first and second inputs, each of said first inputs being supplied with a pulse by only one decoded command signal, said second input being enabled by said response signal.

4. The invention as defined in claim **1** wherein said command signal and said address signal each comprises a plurality of pulses and spaces each having a coded duration, the first pulse of said address signal immediately following the last space of said command signal, and wherein said command decoder comprises:

means for generating a short duration pulse at the leading and trailing edges of each of said pulses;

a clock for generating timing pulses, said clock being synchronized by said short duration pulses;

a timing shift register having a plurality of outputs, each of said outputs representing one possible coded duration, said timing shift register being advanced by the timing pulses of said clock;

a pulse shift register having a plurality of outputs equal to the number of pulses and spaces of said command signal, said pulse shift register being advanced by each of said short duration pulses whereby each output represents a particular pulse or space; and

a system of gates, a selected one of said gates being enabled in response to one preselected combination of the outputs of said pulse shift register and said timing shift register, and a response to said address signal.

5. The invention as defined in claim **4** wherein said command decoder also comprises first and second gates, the outputs from said gates serving to initiate or terminate a function, said first gate being enabled when the duration of said command signal is equal to a first predetermined period of time substantially greater than said coded duration, said second gate being enabled when the duration of said command signal pulse is equal to a second such predetermined period of time, whereby a function may simultaneously be performed at all remote stations.

6. The invention as defined in claim **4** wherein said command decoder also comprises a counter, the output pulses from said clock being applied to said counter during the period of each command pulse, said counter having first and second outputs representing first and second periods of time, each substantially greater than said coded duration;

first and second AND gates, each having first and second inputs, said first inputs of said first and second AND gates being connected, respectively, to said first and second outputs of said counter, said second input of said first and second AND gates being supplied with said short duration pulses whereby an output is developed at the output of one of said first or second gates when a command pulse of said predetermined durations is counted by said counter, said output from said AND gates serving to provide first and second functions.

7. The invention as defined in claim **6** wherein said pulse shift register and said timing shift register are reset whenever said command pulses or spaces are different from said coded durations.

8. In a signaling system having signal transmitting means at a central station for transmitting coded address and command signals to remote stations, and a command signal decoder at each of said remote stations for decoding said command signals, said command signal and said address signals each comprising a plurality of signal pulses and spaces each having a coded duration, the first pulse of said address signal immediately following the last space of said command signal, said command decoder comprising:

means for generating a short duration pulse at the leading and trailing edges of each of said signal pulses;

means for generating a short duration pulse at the leading and trailing edges of each of said signal pulses;

a clock for generating timing pulses, said clock being synchronized by said short duration pulses;

a timing shift register having a plurality of outputs, each of said outputs representing one possible coded duration, said timing shift register being advanced by the timing pulses of said clock;

a pulse shift register having a plurality of outputs equal to the number of pulses and spaces of said command signal, said pulse shift register being advanced by each of said short duration pulses whereby each output represents a particular pulse or space; and

a system of gates, a selected one of said gates being enabled in response to one preselected combination of the outputs of said pulse shift register and said timing shift register, and a response to said address signal.

9. The invention as defined in claim **8** wherein said command decoder also comprises first and second gates, the output from said gates serving to initiate or terminate a function, said first gate being enabled when the duration of said command signal is equal to a predetermined period of time substantially greater than said first coded duration, said second gate being enabled when the duration of said command signal pulse is equal to a second such predetermined period of time, whereby a function may be performed at all remote stations simultaneously.

10. The invention as defined in claim **8** wherein said command decoder comprises a counter, the output pulses from said clock being applied to said counter during the period of each command pulse, said counter having first and second outputs representing first and second periods of time, each substantially greater than said coded duration;

first and second AND gates, each having first and second inputs, said first inputs of said first and second AND gates being connected, respectively, to said first and second outputs of said counter, said second input of said first and second AND gates being supplied with said short duration pulses whereby an output is developed at said first or second output when a command pulse of said predetermined durations is counted by said counter, the output from said AND gates serving to provide first and second functions.

11. The invention as defined in claim 10 wherein said pulse shift register and said timing shift register are reset whenever said command pulses or spaces are different from said coded durations.

12. In a signaling system having a central station and a plurality of remote stations, said central station having means for sequentially transmitting time coded address signals to each of said remote stations in a preestablished sequence, each of said remote stations transponding to said central station upon receipt of a respective time coded address signal, the combination comprising:

a fixed frequency oscillator having a fixed frequency output;

a gate having an output terminal and first and second input terminals, said fixed frequency output being applied to the first input terminal, said fixed frequency output being coupled to said remote stations through the output terminal of said gate when said gate is enabled, said gate being enabled when an enabling pulse is applied to said second terminal, the duration of each enabling pulse establishing said time coded address signals;

first enabling pulse generating means for sequentially generating enabling pulses of different durations, said durations representing said coded address signals, the output of said enabling pulse generating means being applied to said second terminal;

a first plurality of duration determining means connectable into said enabling pulse generating means for establishing the duration of said enabling pulse;

sequential switching means for sequentially connecting each of said duration determining means into said enabling pulse generating means for establishing the durations of said enabling pulse in said preestablished sequence;

a second plurality of selectable duration determining means;

second enabling pulse generating means for sequentially generating enabling pulses of different durations distinct from the durations of said coded address signals, said distinct durations repesenting a command signal;

means for interrupting said first enabling means and for applying said second enabling means to said second input terminal for transmitting a command signal to said remote station;

means after the transmission of said command for transmitting a coded address signal;

means at said remote stations for decoding said command signal;

means at said remote station for decoding said address signal; and

means responsive to the decoding of said address signal for generating a response to said command.

* * * * *