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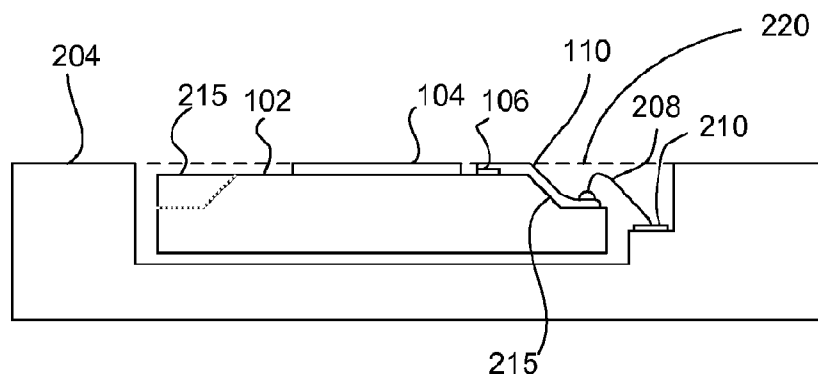


FIG. 2A

(57) **Abstract:** A sensor array package can include a sensor disposed on a first side of a substrate. Signal trenches can be formed along the edges of the substrate and a conductive layer can be deposited in the signal trench and can couple to sensor signal pads. Bond wires can be attached to the conductive layers and can be arranged to be below a surface plane of the sensor. The sensor array package can be embedded in a printed circuit board enabling the bond wires to terminate at other conductors within the printed circuit board.



SENSOR ARRAY PACKAGE

FIELD OF THE DESCRIBED EMBODIMENTS

[0001] The described embodiments relate generally to packaging for sensors, and more particularly, to low profile sensor array packages.

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BACKGROUND

[0002] Sensors and sensor arrays can be formed from customized integrated circuits. Sensor arrays are often used to sense environmental characteristics or can act as a user input for computing devices. Sensor arrays are often formed on a silicon wafer, using similar processing techniques to those used to fabricate other integrated circuits, such as memories, processors, field programmable gate arrays (FPGAs) and the like.

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[0003] Sensors, unlike some general purpose integrated circuits, can have unique packaging and mounting requirements. Typical integrated circuits, for example, can have related silicon bonded out, and then packaged. The bonding out steps can couple signals on the silicon to pins or balls on the package. The packaging step can include encapsulating the silicon die in a package (typically plastic or ceramic). The packing can support and protect the otherwise fragile silicon die. However, since sensors are meant to interface with the environment, the packaging steps are often different.

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[0004] Sensors are often outward facing, and generally exposed to a user environment. Instead of having the silicon die protected by a package, the die is often times exposed on the surface of a supporting element. While such configurations permit the sensor to function, these configurations can be bulky and can take up a relatively large amount of volume, increasing the size of a user device that the sensor is ultimately used.

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[0005] Therefore, what is needed is a sensor, sensors, and/or sensor arrays which overcome these and other drawbacks.

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SUMMARY OF THE DESCRIBED EMBODIMENTS

[0006] One embodiment of a low profile sensor array assembly can include a sensor disposed on a first side of a substrate. Signal trenches can also be formed on the first side of the substrate and can be near sensor signal pads and extend to one edge of the substrate. A conductive layer can be deposited in the signal trench and couple to sensor signal pads.

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Bond wires can attach to the conductive layer and can couple signals from the sensor to external pads.

[0007] Another embodiment of a low profile sensor array assembly can include a sensor disposed on a first side of a substrate. The substrate can include a shaped feature on a first edge positioned near a signal pad of the sensor. The shaped feature can be configured to support a wire bond ball below a surface plane relative to the sensor. A conductive layer can be deposited on the substrate coupling the signal pad and the wire bond ball. A bond wire can be coupled to the wire bond ball and be arranged to remain below the surface plane relative to the sensor.

[0008] According to another embodiment of the invention, a low profile integrated circuit assembly includes at least one integrated circuit, a substrate including a first side, wherein the integrated circuit is disposed on the first side, at least one signal trench, formed on the first side of the substrate, proximate to an integrated circuit signal pad and extending to one edge of the substrate, a conductive layer disposed in the signal trench and coupling to the integrated circuit signal pad, and a bond wire configured to couple the conductive layer to an external pad wherein the bond wire, signal trench and conductive layer are maintained below a surface plane of the integrated circuit.

[0009] According to another embodiment of the invention, a low profile circuit assembly includes an integrated circuit, a substrate including a first side, wherein the integrated circuit is disposed on the first side, a shaped feature on a first edge of the substrate disposed proximate to an integrated circuit signal pad and arranged to support a wire bond ball below a surface plane of the integrated circuit, a conductive layer disposed on the first side of the substrate and configured to couple the integrated circuit signal pad to the wire bond ball, and a bond wire coupled to the wire bond ball and configured to remain below the surface plane of the integrated circuit.

[0010] According to another embodiment of the invention, a low profile assembly includes a first substrate, a second substrate, larger than the first substrate, wherein the first substrate is disposed on a first side of the second substrate, and at least one signal trench disposed on the first side of the second substrate and configured to support bond wires connections to the first substrate below a surface plane of the first substrate.

[0011] According to another embodiment of the invention, a method of forming a low profile assembly includes forming at least one signal trench in a substrate, depositing a barrier layer over the substrate proximate the at least one signal trench, depositing a seed layer of metal in the at least one signal trench, masking the substrate, barrier layer, and at least one signal trench, depositing additional metal over the masked substrate, and removing the mask and seed layer to form a final conductive layer in the at least one signal trench.

[0012] Other aspects and advantages of the invention will become apparent from the following detailed description taken in conjunction with the accompanying drawings which illustrate, by way of example, the principles of the described embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The described embodiments and the advantages thereof may best be understood by reference to the following description taken in conjunction with the accompanying drawings. These drawings in no way limit any changes in form and detail that may be made to the described embodiments by one skilled in the art without departing from the spirit and scope of the described embodiments.

[0014] FIGS. 1A and 1B are simplified diagrams of a low profile sensor, in accordance with one embodiment of the invention.

[0015] FIGS. 2A -2D illustrate side views of exemplary embodiments of a low profile sensor.

[0016] FIGS. 3A – 3D illustrate possible shape profiles for signal trenches.

[0017] FIGS. 4A – 4G illustrate steps that can be used to form a signal trench.

[0018] FIG. 5 is a flow chart of method steps for forming signal trenches in a substrate.

[0019] FIG. 6 is a side view of signal trench, in accordance with one embodiment of the specification.

[0020] FIG. 7 shows another embodiment of a low profile sensor.

[0021] FIG. 8 shows a side view of one embodiment of a way of forming multiple low profile sensors.

[0022] FIG. 9 illustrates optional features that can be applied to a low profile sensor assembly embedded in a PCB.

[0023] FIGS. 10A and 10B illustrate another embodiment of a low profile sensor.

[0024] FIGS. 11A – 11E illustrate steps that can be used to mount a low profile sensor on a substrate.

[0025] FIG. 12 is a flow chart of method steps for mounting a low profile sensor on a substrate.

[0026] FIG. 13 is a top view of yet another embodiment of a low profile sensor.

[0027] FIG. 14 illustrates a cross-sectional view of a low profile sensor according to some embodiments.

[0028] FIG. 15A illustrates a cross-sectional view of a low profile sensor, according to some embodiments.

[0029] FIG. 15B illustrates a detailed cross-sectional view of a low profile sensor, according to some embodiments.

[0030] FIG. 16 illustrates a cross-sectional view of a low profile sensor, according to some embodiments.

DETAILED DESCRIPTION OF SELECTED EMBODIMENTS

[0031] Representative applications of methods and apparatus according to the present application are described in this section. These examples are being provided solely to add context and aid in the understanding of the described embodiments. It will thus be apparent to one skilled in the art that the described embodiments may be practiced without some or all of these specific details. In other instances, well known process steps have not been described in detail in order to avoid unnecessarily obscuring the described embodiments. Other applications are possible, such that the following examples should not be taken as limiting.

[0032] In the following detailed description, references are made to the accompanying drawings, which form a part of the description and in which are shown, by way of illustration, specific embodiments in accordance with the described embodiments. Although these embodiments are described in sufficient detail to enable one skilled in the art to practice the described embodiments, it is understood that these examples are not

limiting; such that other embodiments may be used, and changes may be made without departing from the spirit and scope of the described embodiments.

[0033] Sensors and sensor arrays are often fabricated on a silicon die and then supported with a structure underneath the die. To protect the surface of the sensor, often a clear cover is applied. However, some embodiments require little if any cover over the sensor, to increase sensor sensitivity. Furthermore, the support structure can be bulky and in turn increase the size of a product design including the sensor.

[0034] One embodiment of a low profile sensor can include a sensor disposed on a silicon die. The silicon die, in turn, can be embedded in a printed circuit board (PCB) structure. The low profile sensor can include signal trenches formed in the silicon to allow bond wires to couple to the sensor, while remaining substantially below a surface plane of the sensor. Bond wires can couple the sensor directly to other embedded devices, or to one or more conductive layers in the PCB.

[0035] Signal trenches can be formed by removing substrate material such as with a saw or grinder, or signal trenches can be formed by selectively etching the substrate. After forming the signal trench, a conductive material can be deposited into the trench forming a conductive path between a sensor pad and the trench. Finally, a bond wire can be attached to the conductive material and can be used to couple signals from the sensor to external devices or other components.

[0036] FIGS. 1A and 1B are simplified diagrams of a low profile sensor 100, in accordance with one embodiment of the specification. FIG. 1A shows a top view of the low profile sensor 100. Low profile sensor 100 can include a substrate 102 and a sensor 104 disposed on a first surface of substrate 102. Substrate 102 can be silicon or any other technically feasible material such as gallium arsenide, gallium nitride or the like. Sensor 104 can be a single sensor or an array of sensors. Sensor 104 can be used to detect user input such a touch (pressure), heat or capacitive sensor. In other embodiments, sensor 104 can be any other feasible integrated circuit. Such integrated circuits can be formed on any technically feasible substrate such as silicon, gallium arsenide or the like. In other words, the mounting techniques described herein can be applied equally to any integrated circuit, not only sensors. Throughout this specification, reference will be made to a sensor in the description, but it is understood that any integrated circuit can be substituted for the sensor. Also disposed on the first surface are pads 106 that can be electrically coupled to

signals in sensor 104. FIG. 1A also shows a top view of a signal trench 108. A layer of metal 110 (or other conductor) can be deposited in signal trench 108 and couple to pad 106. This is described in greater detail below in conjunction with FIG. 4. FIG. 1B is a side view of low profile sensor 100. This view shows some detail of a possible shape of signal trench 108 within substrate 102. The shape of the signal trench 108 is indicated with dashed lines.

[0037] FIGS. 2A-2D illustrate side views of exemplary embodiments of a low profile sensor. FIGS. 2A and 2B show low profile sensor 100 embedded in a PCB. FIGS. 2C and 2D show low profile sensor 100 mounted on a thin substrate, such as a flex circuit. These figures are not drawn to scale, but are meant to show relationships between low profile sensor 100 and PCB or low profile sensor 100 and thin substrate. These figures are not meant to be exhaustive and show every possible configuration, but rather illustrate exemplary approaches. Persons skilled in the art can appreciate that other approaches exist. FIG. 2A illustrates a first bonding approach 200 between substrate 102 and PCB 204. Substrate 102 can include a sensor 104 disposed on a first side. Signal trenches 215 are shown in side view. Metal layer 110 can be formed in signal trenches 215 and can couple to pad 106. Wire bond 208 can couple metal layer 110 to a pad 210 that can be on any layer within PCB 204. Wire bonds 208 can be implemented to be below the surface plane 220 of sensor 104. A surface plane can be an imaginary plane that extends in all directions and is co-planar with the highest surface of sensor 104. Surface plane 220 is denoted with a dashed line.

[0038] FIG. 2B illustrates a second bonding approach 250 between substrate 102 and PCB 204. Sensor 104 is mounted on substrate 102 and includes pad 106. Signal trenches 215 can be formed in substrate 102 and can include metal layer 110 coupled to pad 106. Substrate 102 and separate device 252 can be embedded together in PCB 204. In some embodiments, two or more separate devices 252 can be embedded in PCB 204. Device 252 can be a separate integrated circuit that can be used to provide additional functionality to sensor 104. For example, device 252 can be a signal processing device used to preprocess signals from sensor 104. Device 252 can include at least one pad 254 to couple to signals within device 252. Wire bond 208 can couple metal layer 110 to device 252. Wire bond 208 can be maintained below surface plane 220.

[0039] FIG. 2C illustrates a third bonding approach 260 between substrate 102 and thin substrate 225. In one embodiment, thin substrate 225 can be a flexible circuit (flex circuit). Substrate 102 can be affixed to thin substrate 225 with an adhesive, such as a glue, epoxy or tape adhesive. Sensor 104 can be disposed on substrate 102. Signal trenches 215 can be formed on substrate 102 and can support metal layer 110 over pad 106. A bond wire 208 can couple metal layer 110 to a pad 210. In this embodiment, bond wire 208 can be maintained below surface plane 220.

[0040] FIG. 2D illustrates a fourth bonding approach 270 between multiple substrates and thin substrate 225. As shown, a first substrate 102A and a second substrate 102B are affixed to thin substrate 225. Bond wire 208 can be used to couple metal layers 110 from two or more substrates. In FIG. 2D, bond wire 208 can couple signals from first substrate 102A to second substrate 102B. In this manner, two or more substrates 102A, 102B can be linked together.

[0041] FIGS. 3A – 3D illustrate possible shape profiles for signal trench 215. In one embodiment, the shape profile of the signal trench can affect signal integrity of the signals carried within the signal trenches 215. For example, some common metal deposition techniques (i.e., filament evaporation or electron beam evaporation) can have poor coverage on vertical or near vertical surfaces. Other metal deposition techniques can have improved coverage on vertical or near vertical surfaces, but may have other associated costs (i.e., sputter deposition). In other words, certain shape profiles can be preferred over others depending on a selected metal deposition method. Other shape profiles can be possible beyond the exemplary shapes described below.

[0042] FIG. 3A illustrates a vertical profile 301 for signal trench 215. In this embodiment, trench 215 can have a substantially rectilinear profile 301. The rectilinear profile 301 can be formed by many methods, including saw blade and deep reactive ion etch techniques. In some embodiments, two or more shaping methods can be combined to create vertical profile 301. As shown, vertical profile 301 can include at least one substantially vertical section 302. In some embodiments, vertical or near vertical sections may not have relatively even metal coverage. An uneven metal layer can include voids or other irregularities that could result in a discontinuity in the metal.

[0043] FIG. 3B illustrates a ramp profile 303 for signal trench 215. The ramp profile 303 can be formed a number of ways. In one embodiment a saw blade can be used to

form and shape signal trench 215. In another embodiment, ramp profile 303 can be formed, at least in part, by wet etching with potassium hydroxide (KOH). Etching with potassium hydroxide can have the advantage that, by virtue of the reactant, a ramp angle is naturally produced. One advantage of ramp profile 303 is that the profile includes no substantially vertical portions. Thus, the shape of the profile can enable the deposition of relatively even metal layers 110.

[0044] FIG. 3C illustrates an engineered curve profile 305. Engineered curve profile 305 can be formed with a shaped saw blade, or by etching. In some embodiments, two or more shaping methods can be combined to create engineered curve profile 305. One advantage of engineered curve profile 305 is that the profile does not include any sharp bends or curves. Sharp bends or curves can become stress points within the substrate 102. These stress points can become starting points for fractures and cracks. Another advantage of engineered curve profile 305 is that the profile does not include any substantially vertical portions, therefore the profile can support the formation of relatively even metal layers.

[0045] FIG. 3D illustrates a bowl shaped profile 307. This profile can be formed with a saw or with etching methods. One advantage of the bowl shaped profile 307 is the inherent strength of the profile. Substrate area near bowl shaped profile 307 can be relatively stronger when compared to areas near other profiles such as rectilinear profile 303. A drawback of the bowl shaped profile 307 is that it can include a relatively vertical region 308. As described above, vertical regions can develop discontinuities and voids when certain metal deposition techniques are used.

[0046] FIGS. 4A – 4G illustrate steps that can be used to form signal trench 215. These illustrations are cross sectional views of the trench, with the surrounding areas not drawn to clarify the drawing. FIG. 4A shows a possible beginning state including substrate 102. Pad 106 and sensor 104 are disposed on a first side of substrate 102. FIG. 4B shows substrate 102 with signal trench 215 formed into the substrate 102. Sensor 104 and pad 106 remain on the surface of substrate 102. Signal trench 215 can be formed in the shape of any technically feasible profile. Exemplary profiles are described above in FIG. 3. Ramp profile 303 is selected as the exemplary profile in this figure. Ramp profile 303 can be formed using a potassium hydroxide etch process, for example. FIG. 4C shows a barrier layer 405 deposited on the substrate 102. In one embodiment, barrier layer

405 can be formed with techniques similar to forming passivation layers. In one embodiment, barrier layer 405 can help protect sensor 104.

[0047] FIG. 4D shows substrate 102, pad 106 and sensor 104. In this view, a metal seed layer 410 has been deposited over the substrate 102, barrier layer 405 and pad 106.

5 As shown, seed layer 410 can be deposited in the regions of the signal trench 215 where a final conductive channel is desired. In one embodiment, seed layer 410 can be deposited by sputtering a conductive metal, such as aluminum. FIG. 4E shows substrate 102, pad 106 and sensor 104 with a mask 415 selectively applied to the first surface. Mask 415 can be used to define regions where additional metal can be deposited over the seed layer 410.

10 In one embodiment mask 415 can be a liquid photoimageable mask. FIG. 4F shows metal 420 deposited over substrate 102, pad 106, seed layer 410 and mask 415. During the metal deposition process, metal can be non-selectively deposited over the entire substrate 102. In FIG. 4G shows substrate 102 after the mask 415 and excess metal seed layer 410 is removed. In one embodiment, metal seed layer 410 can be removed with a wet etch process. Removal of the mask 415 and metal seed layer 410 can define the final shape of the metal layer 420 in signal trench 215.

[0048] FIG. 5 is a flow chart of method steps for forming signal trenches 215 in a substrate 102. The method begins in step 502 where the trench profile is formed in the substrate. The trench profile can be selected from one of the profiles described in FIG. 3, or any other technically feasible profile. In step 504, a barrier layer can be formed and deposited over the substrate 102. The barrier layer can help protect the substrate 102 after trenches are formed in substrate 102. In step 506, a seed layer of metal can be deposited in the formed trench and can couple to the pad 106. In step 508, a mask can be selectively placed on the substrate. In one embodiment, the mask can be a liquid photoimageable mask. The mask 405 can be used to determine the areas on the substrate 102 where the metal within the signal trench 215 will be positioned. In step 510, additional metal can be deposited over substrate 102. In one embodiment, metal can be sputtered. The metal sputtered in step 510 may include aluminum, copper, or any other metal or metal alloy. In some embodiments, step 510 may include sputtering an alloy of aluminum and copper (AlCu), having 0.5% copper concentration. Further according to some embodiments, step 30 510 may include depositing a protective layer over the metal layer deposited. Accordingly, the protective layer may include depositing a titanium nitride (TiN) layer on

top of the metal layer. In some embodiments, the protective layer may include pure titanium or any other titanium alloy, such as titanium-tungsten. In step 512, the mask 405 and excess seed layer can be removed, forming the final conductive layer in the signal trench and the method ends.

5 [0049] Formation of the signal trenches 215 can provide access to signals from sensor 104 while maintaining connections below the surface plane 220 of sensor 104. In order to fan out the signals to other devices, wires can be bonded to the metal deposited in the signal trenches 215. After a wire is bonded, the wire can be routed to a pad or other conductor. Care can be taken to maintain the path of the wire to be below the surface
10 plane 220 of sensor 104, thereby allowing a low profile mounting of the sensor 104 and substrate 102. In one embodiment, a wire bond 208 can be formed by depositing a wire bond ball in the signal trench 215 on metal layer 206. The wire can be guided within the signal trench 215.

[0050] In some embodiments, to enhance the bonding of a bonding wire to the metal deposited in step 510, step 512 may include depositing a bond enhancing layer. A bond enhancing layer may include ENEPIG, which stands for electroless nickel, electroless palladium, and immersion gold. Accordingly, depositing a bond enhancing layer may include forming an ENEPIG layer on top of the metal deposited in step 510. For example,
15 in some embodiments forming an ENEPIG layer in step 512 may include dipping the stack formed up to step 510 in an electroless solution including at least one of nickel and palladium. Furthermore, step 512 may include immersing the stack formed up to step 510 in a solution including gold, to form an ENEPIG layer. In some embodiments, step 512 may further include forming a passivation layer adjacent to the additional metal deposited over the masked substrate.
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25 [0051] FIG. 6 is a side view 600 of signal trench 215, in accordance with one embodiment of the specification. The side view 600 includes substrate 102, pad 106 and metal layer 110. Depth 602 of signal trench 205 can be a function of the elements that can be included within signal trench 215. Wire bond ball 604 can be bonded to metal layer 110 in the bottom of signal trench 215. The height 606 of wire bond ball 604 can vary.
30 Common heights can range from 5 – 15 μm . Diameter 608 of wire can vary by application; current carrying wires (power) can be thicker than wires only carrying signals. A typical wire diameter 608 can be 25 μm . Finally, bend radius 610 can affect the depth

602. In one embodiment depth 602 can be determined, at least in part by the sum of the wire bond ball height 606 plus wire diameter 608 plus bend radius 610.

[0052] The width 612 of the bottom of signal trench 215 can be determined, at least in part, by elements that are included in the bottom of the signal trench 215. A typical diameter 615 of wire bond ball can be 50 μm . The distance 617 from the wire bond ball to the edge of the substrate 102 can be 20 μm . This distance can be reduced, however, since edge chipping can occur, yield of the device can be reduced if the distance is reduced too much. The distance 618 from the wire bond ball to the inside edge of the bottom of signal trench 15 can be between 5 to 10 μm . In some embodiments, the distance 618 can be influenced by a tool used for wire bonding. Thus, in one embodiment, width 612 can be determined, at least in part, by the sum of wire bond ball diameter 615, plus distance to substrate edge 617 plus distance to inside edge 618.

[0053] FIG. 7 shows another embodiment of a low profile sensor 700. In this embodiment, signal trenches 215 can be replaced by shaped features disposed on the edge of the substrate. Substrate 702 includes pad 106 disposed on a first side of substrate 702. Shaped feature 706 can be formed on one corner of substrate 702. Metal layer 704 can be disposed on pad 106 and can also be disposed on shaped feature 706. Wire bond ball 604 can be positioned on shaped feature 706 such that wire 708 can be maintained below surface plane 220 of sensor 104.

[0054] FIG. 8 shows a side view 800 of one embodiment of a way of forming multiple low profile sensors. Multiple low profile sensors can be formed on a silicon wafer with each individual low profile sensor formed on an individual die on the wafer. Prior to separating the individual dice, a grinding wheel 802 or shaped saw blade can form signal trenches 215 across two or more dice, with a relatively continuous grind or cut. In the example shown in FIG. 8, grinding wheel 802 can form signal trenches 215 in first and second low profile sensors 805 and 807 respectively. In a later operation, a saw can separate the dice forming a saw cut 810.

[0055] FIG. 9 illustrates optional features that can be applied to a low profile sensor assembly 901 embedded in a PCB 204. The low profile sensor assembly 901 can include sensor 104 and substrate 102. After the low profile sensor assembly 901 is embedded in PCB 204, empty voids 902, especially in the areas of signal trench 215, can be filled with an epoxy, resin or other like material to strengthen the bond between low profile sensor

assembly 901 and PCB 204 and form a relatively planar surface. In another embodiment, components 904 can be disposed on PCB 204, on the side facing away from sensor 104. Components 904 can be passive components such as resistors, inductors, capacitors or the like. Components 904 can be coupled to sensor 104 or other devices.

5 [0056] FIGS. 10A and 10B illustrate another embodiment of a low profile sensor 1000. In this embodiment, individual signal trenches can be replaced with a single trench 1010 that can be formed on edge of substrate 102. Sensor 104 can be disposed on one surface of substrate 102. Pad 106 can be disposed on the same planar surface as sensor 104. Metal layer 1015 can couple pad 106 to at least one region of single trench 1010. In
 10 another embodiment, pads can be positioned within single trench 1010 region as shown with pad 1020. Metal layer 1025 can be deposited over pad 1020 and be positioned in single trench 1010. FIG. 10B shows a side view of low profile sensor 1000. Pad 106 is shown planar to sensor 104. Metal layer 1015 can be deposited on pad 106 and into single trench 1010. In another embodiment, pad 1020 can be positioned in single trench 1010.
 15 Metal layer 1025 can be deposited on pad 1020 and into single trench 1010.

[0057] FIGS. 11A – 11E illustrate steps that can be used to mount a low profile sensor on a substrate. In one embodiment, the substrate can be a thin substrate 1110, such as a flexible cable. FIG. 11A shows an initial state of thin substrate 1110 and pads 1120. Adhesive 1130 can be deposited on thin substrate 1110. Adhesive 1130 can be an epoxy,
 20 glue, adhesive tape or other similar article. In FIG. 11B, substrate 1140 including sensor 1145 can be positioned on adhesive 1130. In FIG. 11C, wire bond balls 1150 can be attached to substrate 1140 in preparation for bond wire attachment. In FIG. 11D, bond wires 1160 can be attached to wire bond balls 1150 and can couple signals from sensor 1145 to pad 1120. In one embodiment, optional wire bond balls 1165 can be coupled to
 25 pad 1120. In FIG. 11E bond wires 1160 can be encapsulated to protect them in an epoxy 1170, resin or similar material.

[0058] FIG. 12 is a flow chart of method steps for mounting a low profile sensor on a substrate. In one embodiment, the substrate can be a thin substrate such as a flexible circuit. The method begins in step 1210 where an adhesive is applied to a substrate. The
 30 adhesive can be a liquid adhesive such as an epoxy or can be a tape based adhesive. In step 1220, the sensor/substrate combination can be bonded to the substrate. In step 1230, bond wire balls can be attached to the substrate. In one embodiment, the bond wire balls

can be coupled to metal layers on the substrate enabling access to the signals in the sensor. In step 1240, bond wires can be attached to bond wire balls and pads disposed on the substrate. In step 1250, bond wires can be encapsulated. Encapsulation can help protect fragile bond wires from damage.

5 [0059] FIG. 13 is a top view of yet another embodiment of a low profile sensor 1300. This embodiment can include both individual single trenches as described in FIG. 1 and multiple signal trenches that can include more than one signal as described in FIG. 10. Low profile sensor 1300 can include substrate 102 and sensor 104. Pads 106 can be disposed outside of a trench. For example, pad 106 is disposed beyond multiple signal
10 trench 1310 and beyond single signal trench 1311. In another embodiment, the pad can be disposed inside the trench region. For example, pad 1020 can be disposed within multiple signal trench 1310 or within single trench 1311. Metal layers 1015 can couple to pads 106 beyond signal trenches 1310 and 1311. Alternatively, metal layers 1025 can couple to pads 1020 within signal trenches 1310 and 1311. In some embodiments, multiple signal
15 trenches 1310 can provide greater signal densities, while in some embodiments, single signal trenches 1311 can provide greater strength to substrate 102. Low profile sensor 1300 includes advantages of both the signal and multiple signal trench systems.

[0060] FIG. 14 illustrates a cross-sectional view of a low profile sensor 1400 according to some embodiments. Low profile sensor 1400 includes trench 1415 formed
20 on a first substrate 1402A adjacent to a second substrate 1402B. In some embodiments, first substrate 1402A may be silicon (e.g., substrate 102, cf. FIGS. 1A and 1B), or any other suitable semiconductor material, such as Gallium Arsenide (GaAs), Gallium Nitride (GaN), and the like. Second substrate 1402B may be an oxide such as silicon oxide. In some embodiments substrate 1402A and 1402B may be the same. Low profile sensor
25 1400 includes a bonding pad 1406, similar to bonding pad 106 described in detail above (cf. FIGS. 1A-1B). Low profile sensor 1400 may also include a seal ring 1408. Seal ring 1408 may surround the periphery of low profile sensor 1400 to provide protection and a barrier for the circuitry inside (e.g., bonding pad 1406). In some embodiments, a material layer 1460 may be formed above seal ring 1408 and portions of bonding pad 1406, to
30 provide protection. An oxide layer 1450 provides electrical insulation to elements on substrates 1402A and 1402B from a conductive layer 1410. Conductive layer 1410 may be made of aluminum, copper, or some other conductive element. Accordingly, in some

embodiments conductive layer 1410 is formed of an alloy of aluminum and copper (AlCu). In some embodiments, the AlCu alloy may have a 0.5% Cu content. Conductive layer 1410 provides electrical coupling between low profile sensor 1400 and circuitry on a PCB board (e.g., PCB board 204, cf. FIG. 2A).

5 [0061] FIG. 15A illustrates a cross-sectional view of a low profile sensor 1500, according to some embodiments. Low profile sensor 1500 includes a bond enhancing layer 1550, among other material layers described in detail above, with regard to FIG. 14. Bond enhancing layer 1550 facilitates the adhesion and electrical coupling of a bonding wire to conductive layer 1410. A bonding wire may be as bonding wire 208 described in
10 detail above (cf. FIGS. 2A-2D). Bond enhancing layer 1550 may also provide corrosion resistance to conductive layer 1410. In some embodiments, bond enhancing layer 1550 may include materials and material combinations such as ENEPIG. ENEPIG is a combination of electroless nickel, electroless palladium, immersion gold layer.

[0062] FIG. 15B illustrates a detailed cross-sectional view of a low profile sensor
15 1500, according to some embodiments. FIG. 15B illustrates in more detail an exemplary composition of bond enhancing layer 1550. Bond enhancing layer 1550 may include a first conductive layer 1551, a second conductive layer 1552, and a third conductive layer 1553. Accordingly, in embodiments where bond enhancing layer 1550 includes ENEPIG, first conductive layer 1551 may include a layer of nickel. Also in an embodiment
20 including ENEPIG, second conductive layer 1552 may include a layer of palladium, and third conductive layer 1553 may include a layer of gold. Accordingly, in some embodiments first conductive layer 1551 may have a thickness between 1 to 3 μm , second conductive layer 1552 may have a thickness between 0.1 to 0.3 μm , and third conductive layer 1553 may have a thickness between 0.05 to 0.1 μm . For example, in some
25 embodiments first conductive layer 1551 may have a thickness of about 1.5 μm . In some embodiments, second conductive layer 1552 may have a thickness of about 0.2 to about 0.25 μm . In further embodiments, third conductive layer 1553 may have a thickness of about 0.1 μm .

[0063] FIG. 16 illustrates a cross-sectional view of a low profile sensor 1600,
30 according to some embodiments. Low profile sensor 1600 may include a passivation layer 1610 adjacent to portions of conductive layer 1410. Passivation layer 1610 may include an oxide material, such as aluminum oxide, or some other protective material. In some

embodiments, conductive layer 1410 may include a protection layer. The protection layer may include materials such as titanium nitride (TiN), or other materials such as pure titanium, and other titanium alloys such as titanium-tungsten. In some embodiments, the protection layer may be deposited as a second step in the deposition of layer 1410 prior to patterning of layer 1410. Accordingly, passivation layer 1610 may be deposited over the patterned layer 1410 including the protection layer. Passivation layer 1610 may form openings over some portions of conductive layer 1410. In some embodiments, a bond enhancing layer 1550 may be formed adjacent to conductive layer 1410 in the openings formed by passivation layer 1610, as shown in FIG. 16.

[0064] The various aspects, embodiments, implementations or features of the described embodiments can be used separately or in any combination. Various aspects of the described embodiments can be implemented by software, hardware or a combination of hardware and software. The described embodiments can also be embodied as computer readable code on a computer readable medium for controlling manufacturing operations or as computer readable code on a computer readable medium for controlling a manufacturing line. The computer readable medium is any data storage device that can store data which can thereafter be read by a computer system. Examples of the computer readable medium include read-only memory, random-access memory, CD-ROMs, HDDs, DVDs, magnetic tape, and optical data storage devices. The computer readable medium can also be distributed over network-coupled computer systems so that the computer readable code is stored and executed in a distributed fashion.

[0065] The foregoing description, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the described embodiments. However, it will be apparent to one skilled in the art that the specific details are not required in order to practice the described embodiments. Thus, the foregoing descriptions of specific embodiments are presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the described embodiments to the precise forms disclosed. It will be apparent to one of ordinary skill in the art that many modifications and variations are possible in view of the above teachings.

CLAIMS

What is claimed is:

1. A low profile integrated circuit assembly, the assembly comprising:

at least one integrated circuit;

5 a substrate including a first side, wherein the integrated circuit is disposed on the first side;

at least one signal trench formed on the first side of the substrate, proximate to an integrated circuit signal pad and extending to one edge of the substrate;

10 a conductive layer disposed in the signal trench and coupling to the integrated circuit signal pad; and

a bond wire configured to couple the conductive layer to an external pad wherein the bond wire, signal trench and conductive layer are maintained below a surface plane of the integrated circuit.

15 2. The assembly of claim 1, wherein the at least one signal trench is configured to have a ramp profile.

3. The assembly of claim 2, wherein the bond wire is further configured to attach to a slope portion of the ramp profile.

20

4. The assembly of claim 1, wherein the at least one integrated circuit is a sensor.

5. The assembly of claim 2, further comprising a flexible printed circuit assembly configured to bond to a second side of the substrate, the second side being disposed
25 opposite the first side.

6. The assembly as in any one of claims 1 through 5, wherein the at least one signal trench includes at least two bond wires configured to couple conductive layers to external pads wherein the bond wires, signal trench and conductive layers are maintained below a
30 surface plane of the integrated circuit.

7. A low profile circuit assembly, the assembly comprising:

an integrated circuit;

a substrate including a first side, wherein the integrated circuit is disposed on the first side;

a shaped feature on a first edge of the substrate disposed proximate to an integrated circuit signal pad and arranged to support a wire bond ball below a surface plane of the integrated circuit;

a conductive layer disposed on the first side of the substrate and configured to couple the integrated circuit signal pad to the wire bond ball; and

a bond wire coupled to the wire bond ball and configured to remain below the surface plane of the integrated circuit.

8. The assembly of claim 7, wherein the shaped feature is configured to have a ramp profile.

9. The assembly of claim 8, wherein the bond wire is further configured to attach to a slope portion of the ramp profile.

10. The assembly of claim 7, wherein the integrated circuit is a sensor.

11. The assembly of claim 8, further comprising a flexible printed circuit assembly configured to bond to a second side of the substrate, the second side being disposed opposite the first side.

12. The assembly of any one of claims 7 through 11, wherein the shaped feature includes at least two bond wires configured to couple conductive layers to external pads, wherein the bond wires, shaped feature, and conductive layers are maintained below a surface plane of the integrated circuit.

13. A low profile assembly, comprising:

a first substrate;

a second substrate, larger than the first substrate, wherein the first substrate is disposed on a first side of the second substrate; and

at least one signal trench disposed on the first side of the second substrate and configured to support bond wires connections to the first substrate below a surface plane of the first substrate.

5 14. The assembly of claim 13, wherein the at least one signal trench is configured to have a ramp profile.

15. The assembly of claim 14, wherein the bond wire is further configured to attach to a slope portion of the ramp profile.

10

16. The assembly of claim 13, further comprising at least one integrated circuit disposed on the first substrate.

15 17. The assembly of claim 14, further comprising a flexible printed circuit assembly configured to bond to a second side of the second substrate, the second side being disposed opposite the first side.

20 18. The assembly of any one of claims 13 through 17, wherein the at least one signal trench can include at least two bond wires configured to couple conductive layers to external pads.

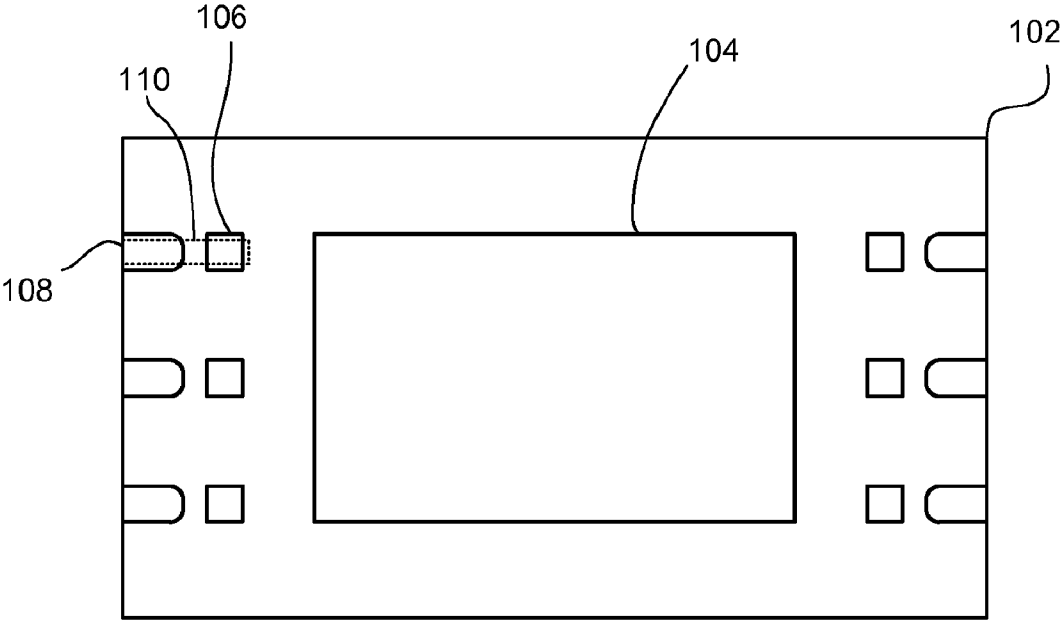
19. A method of forming a low profile assembly, comprising:
forming at least one signal trench in a substrate;
depositing a barrier layer over the substrate proximate the at least one signal
25 trench;
depositing a seed layer of metal in the at least one signal trench;
masking the substrate, barrier layer, and at least one signal trench;
depositing additional metal over the masked substrate; and
removing the mask and seed layer to form a final conductive layer in the at least
30 one signal trench.

20. The method of claim 19, wherein the barrier layer is configured to protect areas of the substrate proximate the at least one signal trench.

21. The method of claim 19, wherein masking the substrate comprises applying a liquid photoimageable mask over the substrate, barrier layer, and at least one signal trench.

5 22. The method of claim 21, wherein the applied photoimageable mask is configured to define areas on the substrate wherein metal within the at least one signal trench is positioned.

10 23. The method of claims 19 through 21, wherein depositing additional metal comprises sputtering metal on a plurality of areas wherein metal within the at least one signal trench is positioned.



100

FIG. 1A

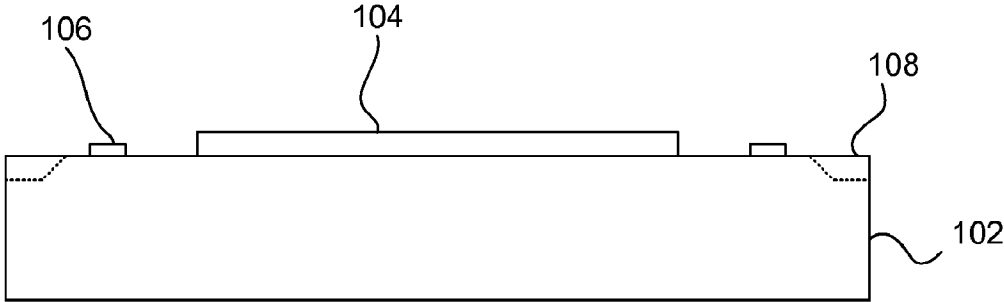


FIG. 1B

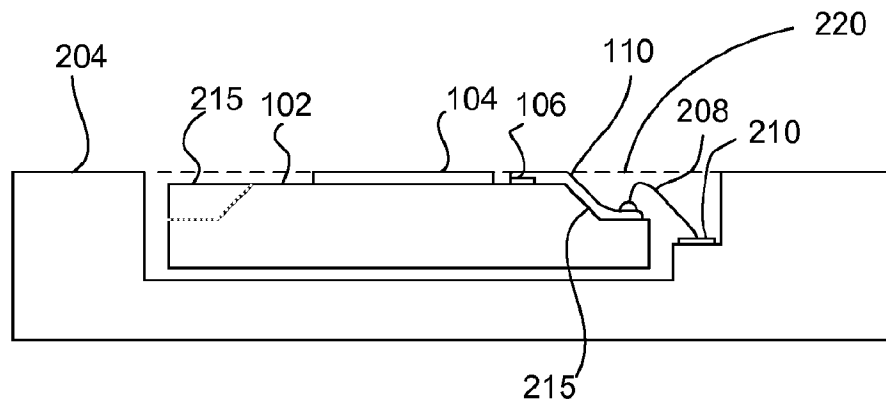


FIG. 2A

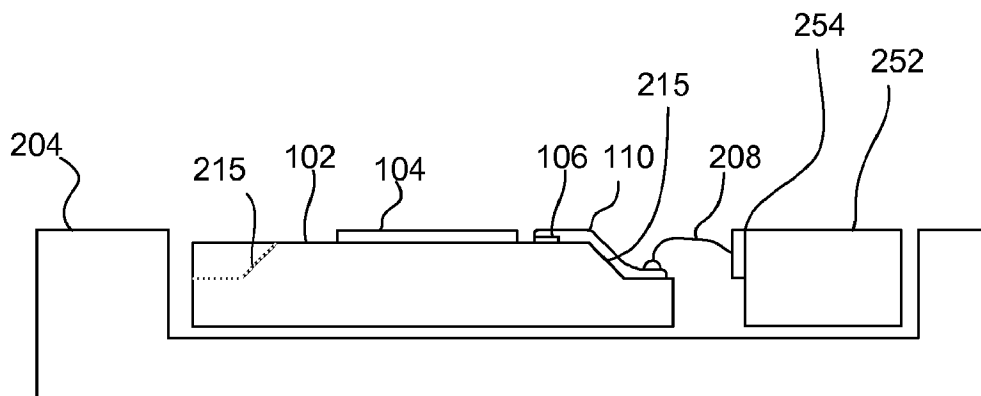


FIG. 2B



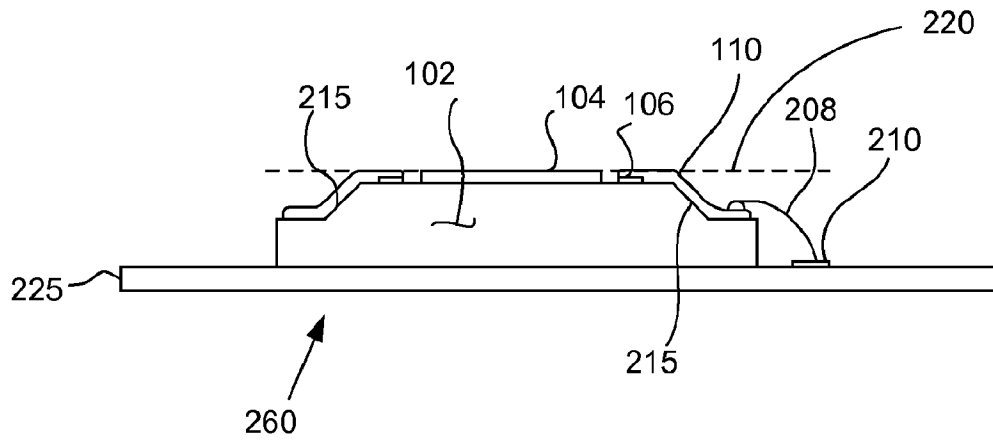


FIG. 2C

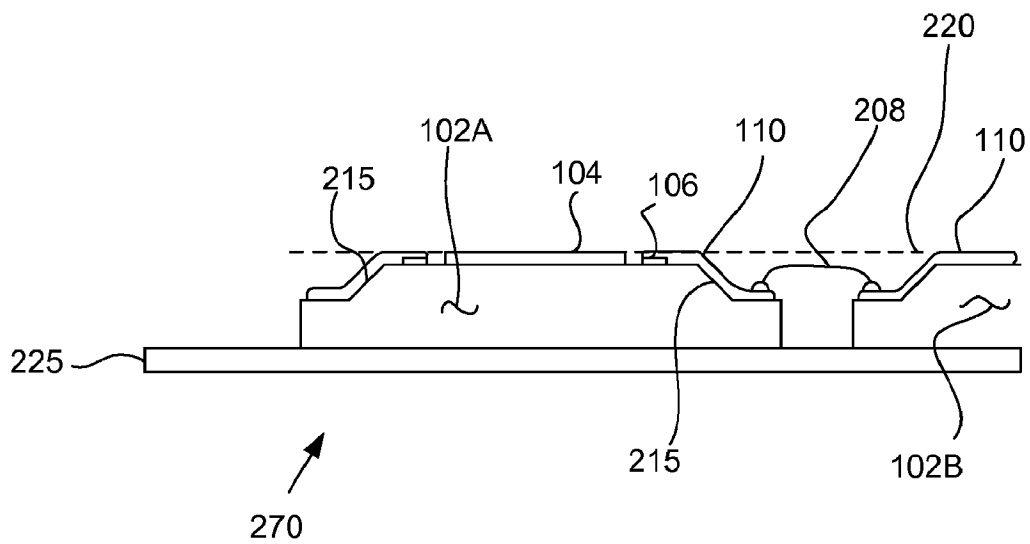


FIG. 2D

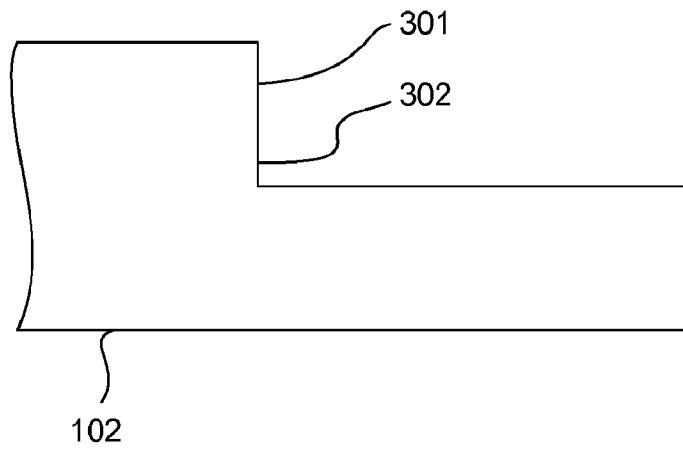


FIG. 3A

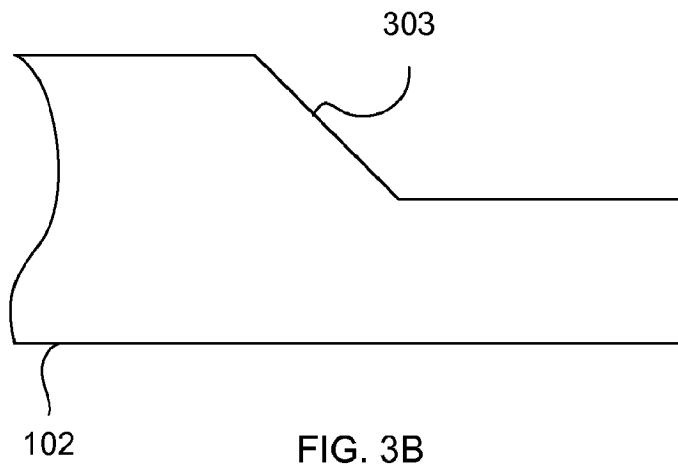


FIG. 3B

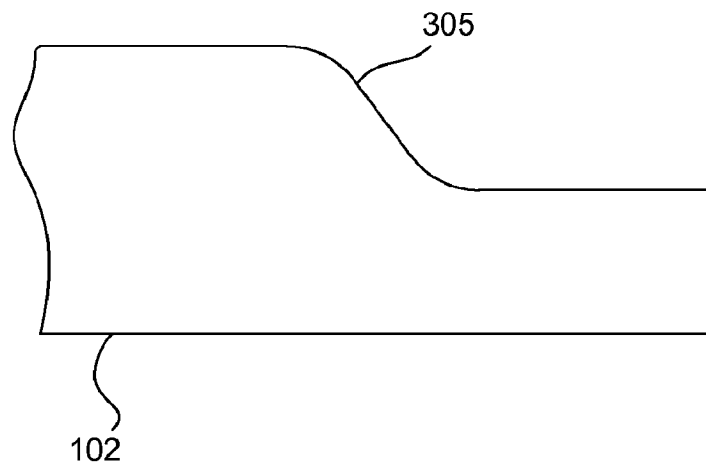


FIG. 3C

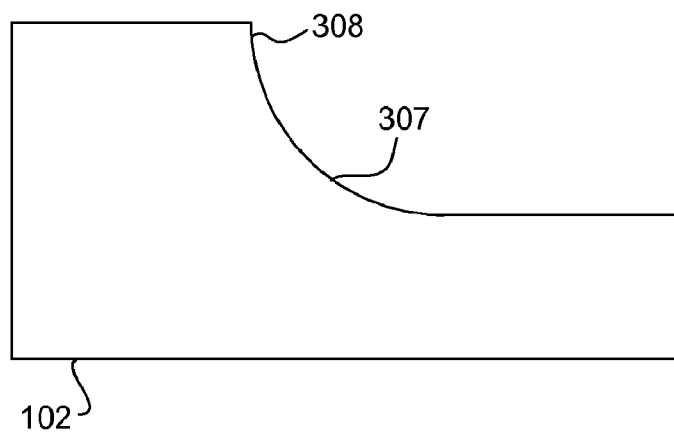


FIG. 3D

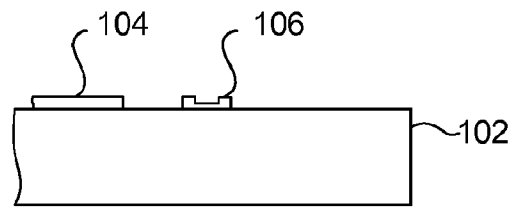


FIG. 4A

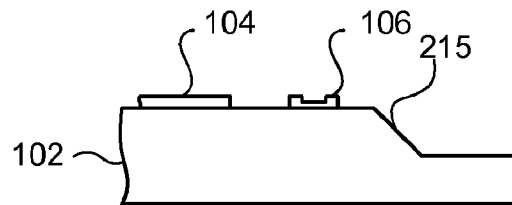


FIG. 4B

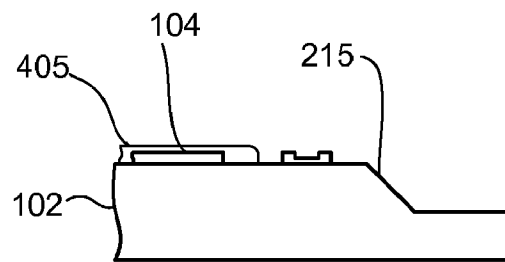


FIG. 4C

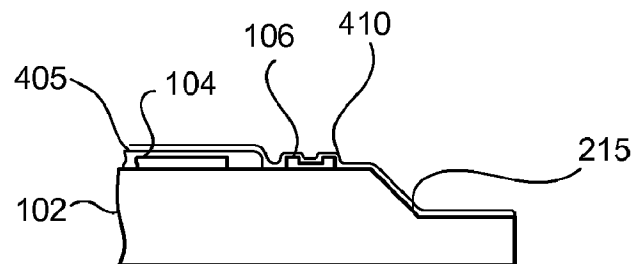


FIG. 4D

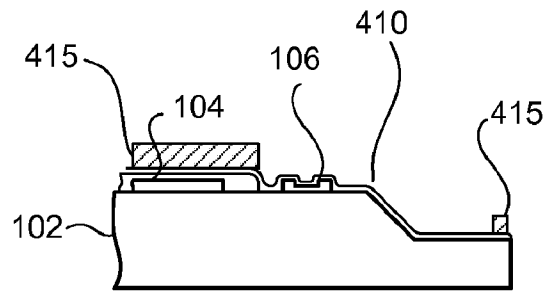


FIG. 4E

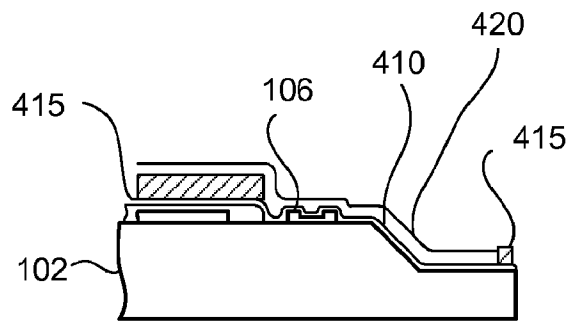


FIG. 4F

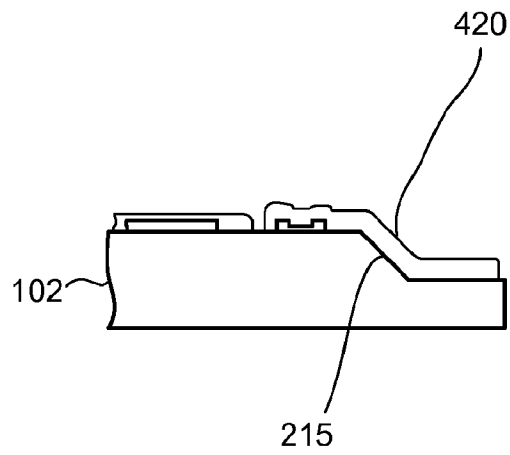


FIG. 4G

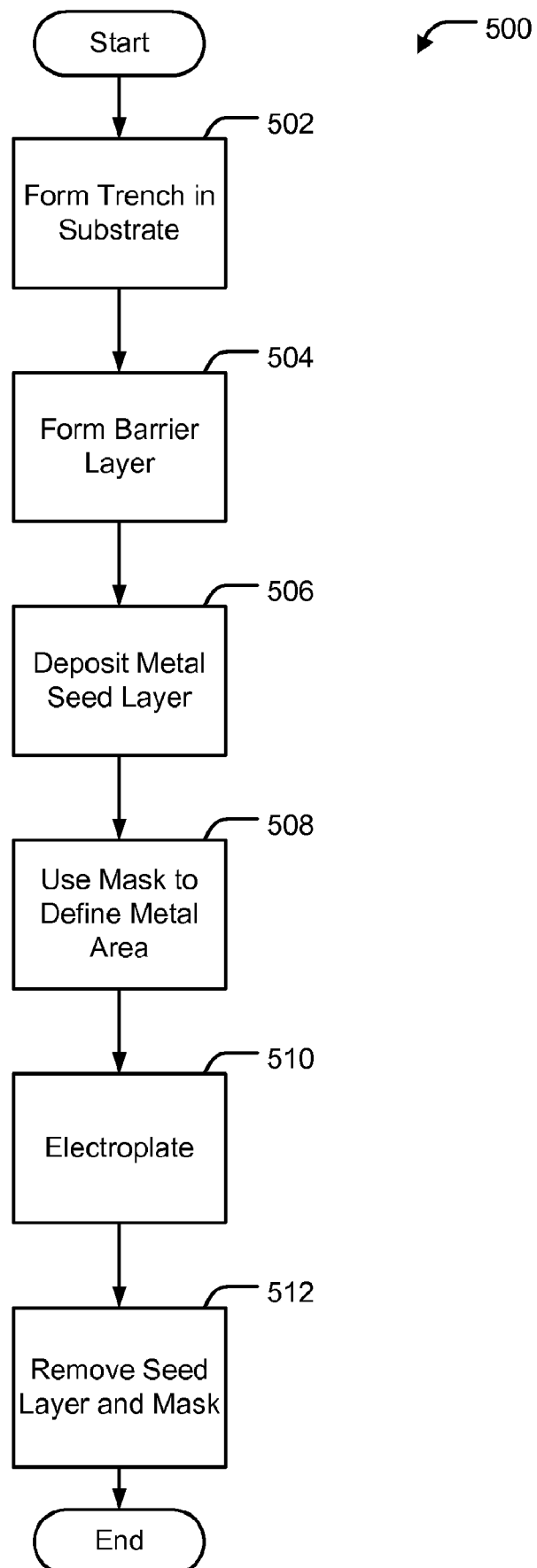


FIG. 5

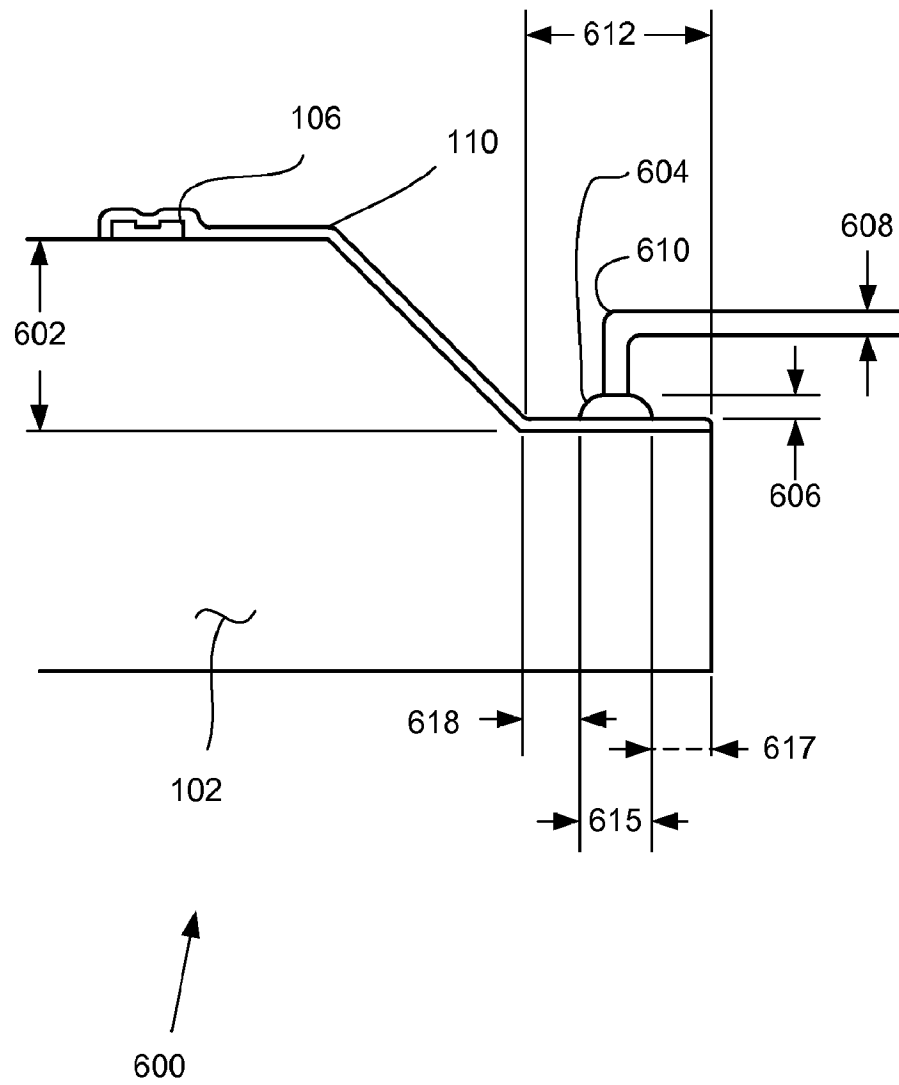


FIG. 6

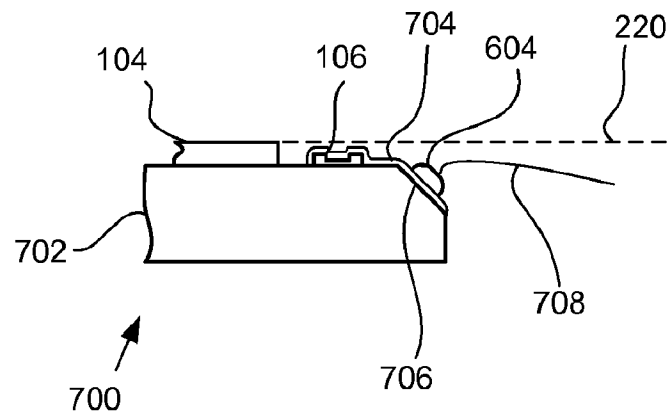


FIG. 7

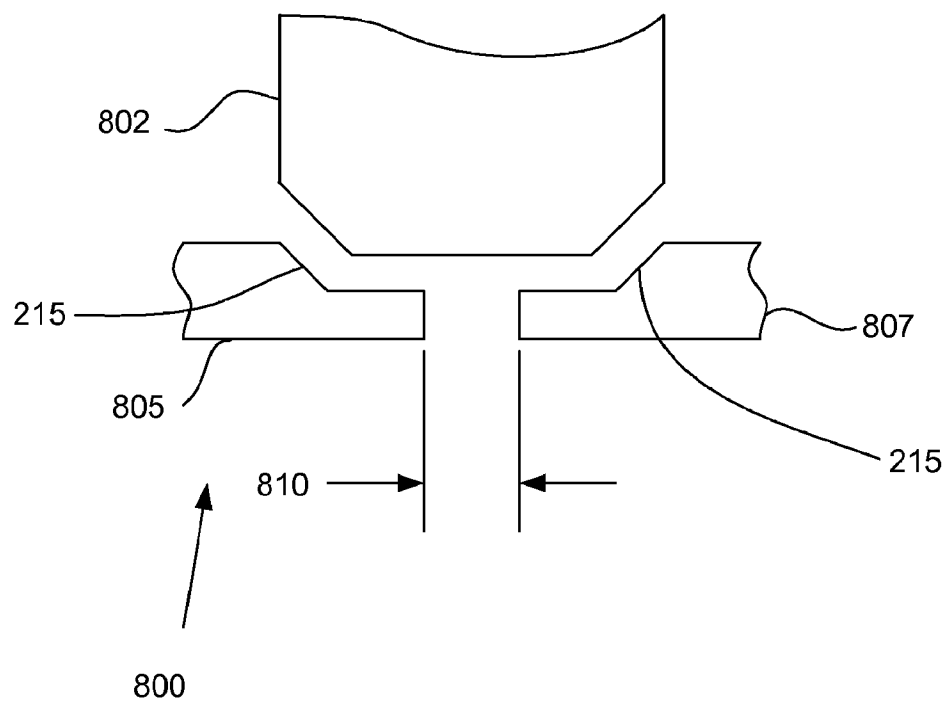


FIG. 8

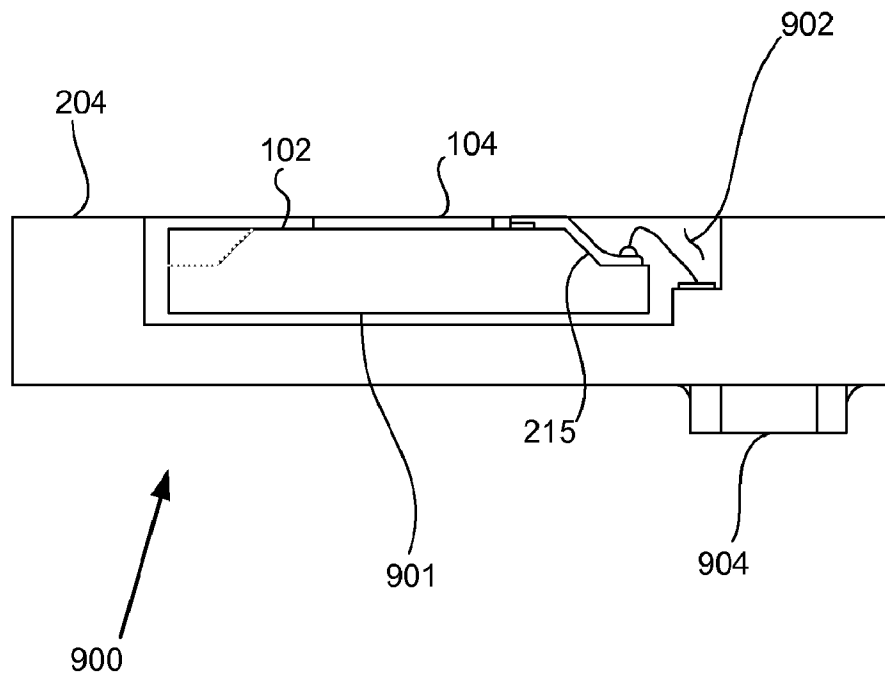
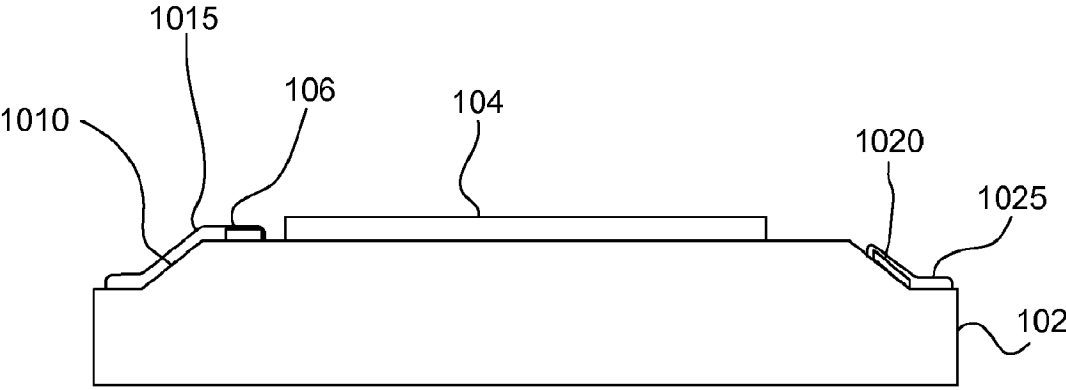
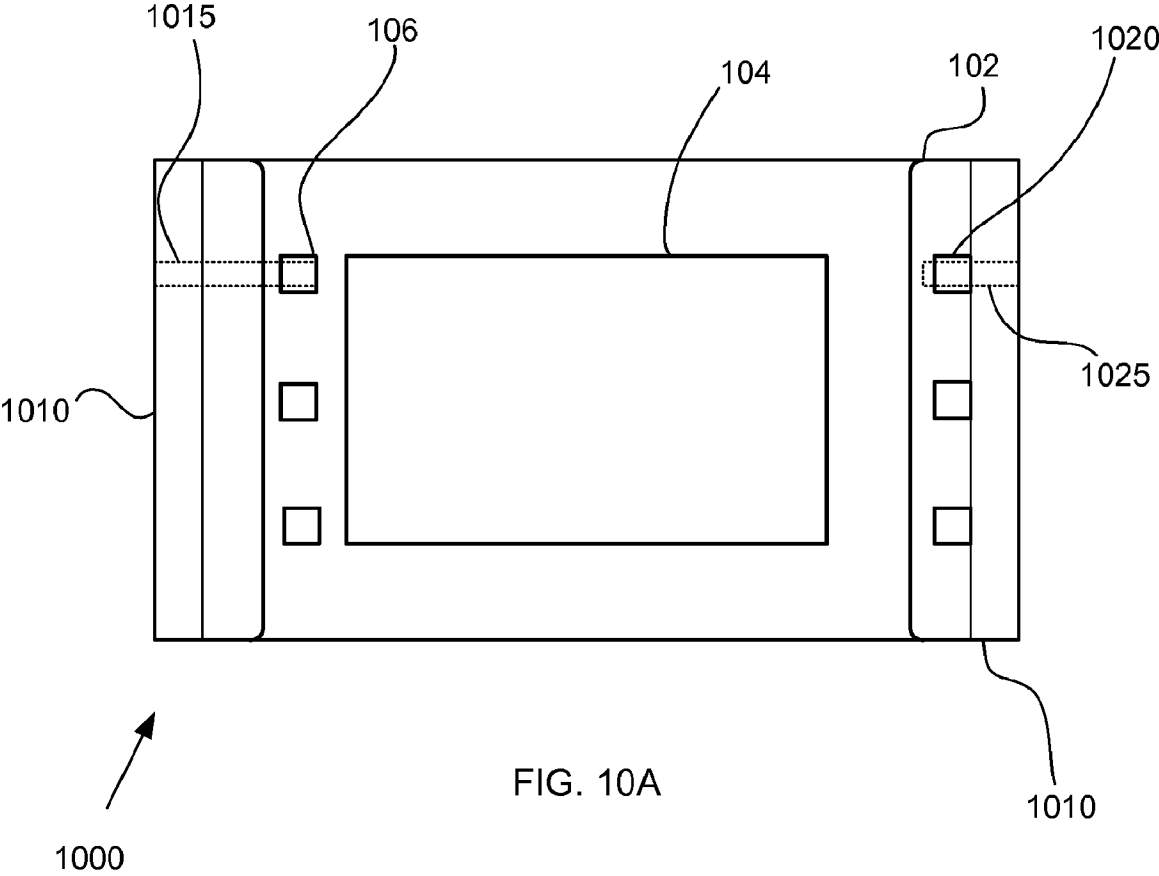


FIG. 9



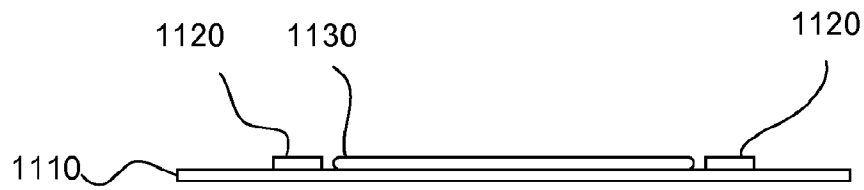


FIG. 11A

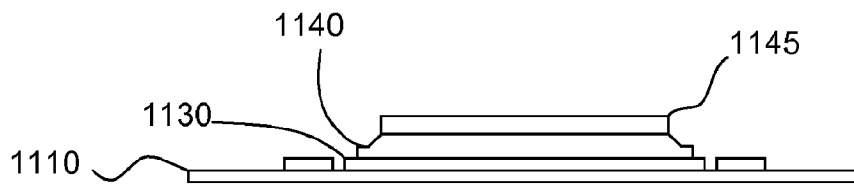


FIG. 11B

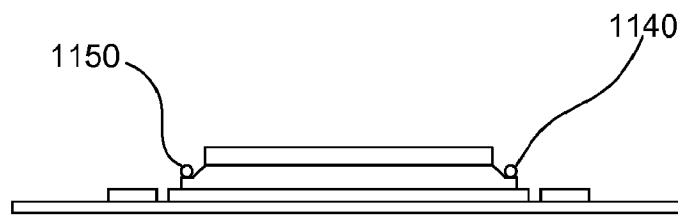


FIG. 11C



FIG. 11D

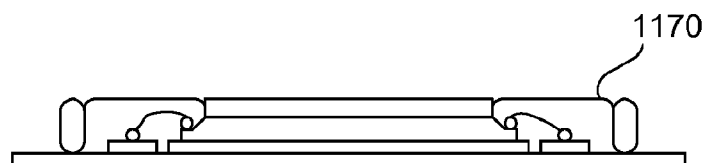


FIG. 11E

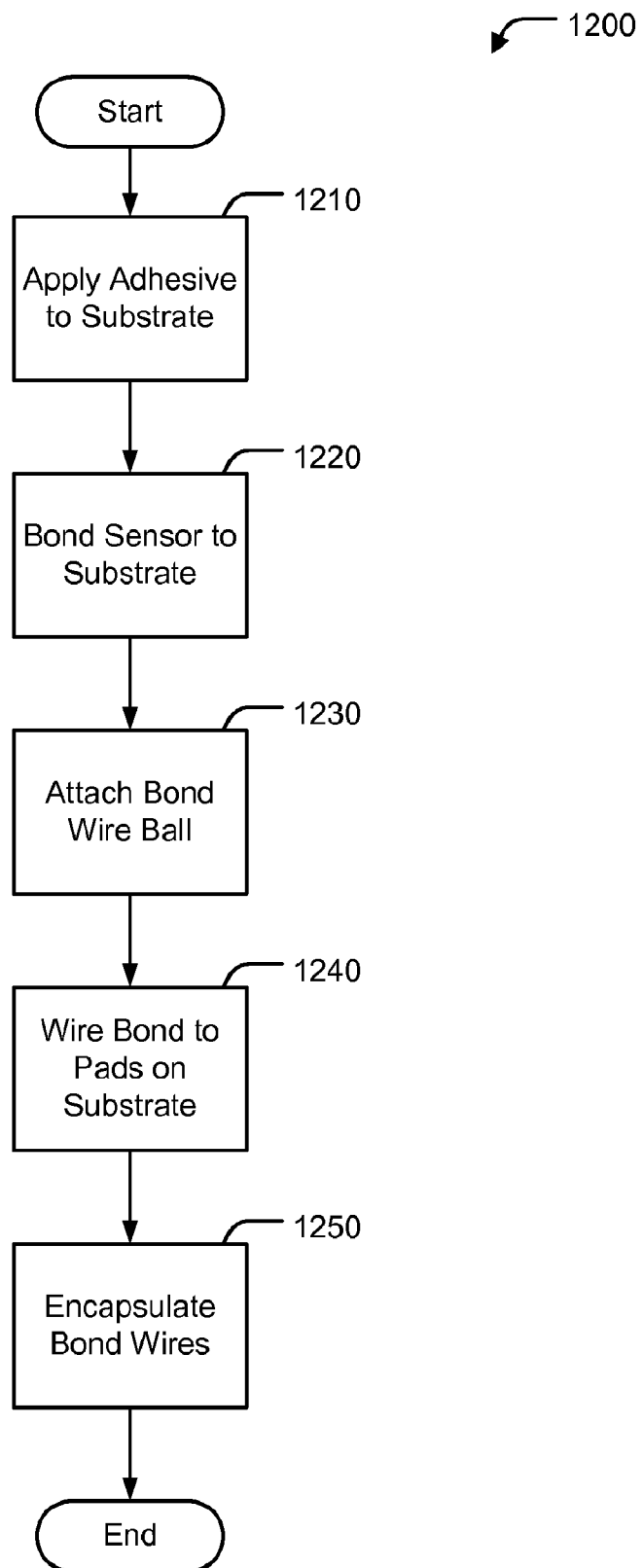


FIG. 12

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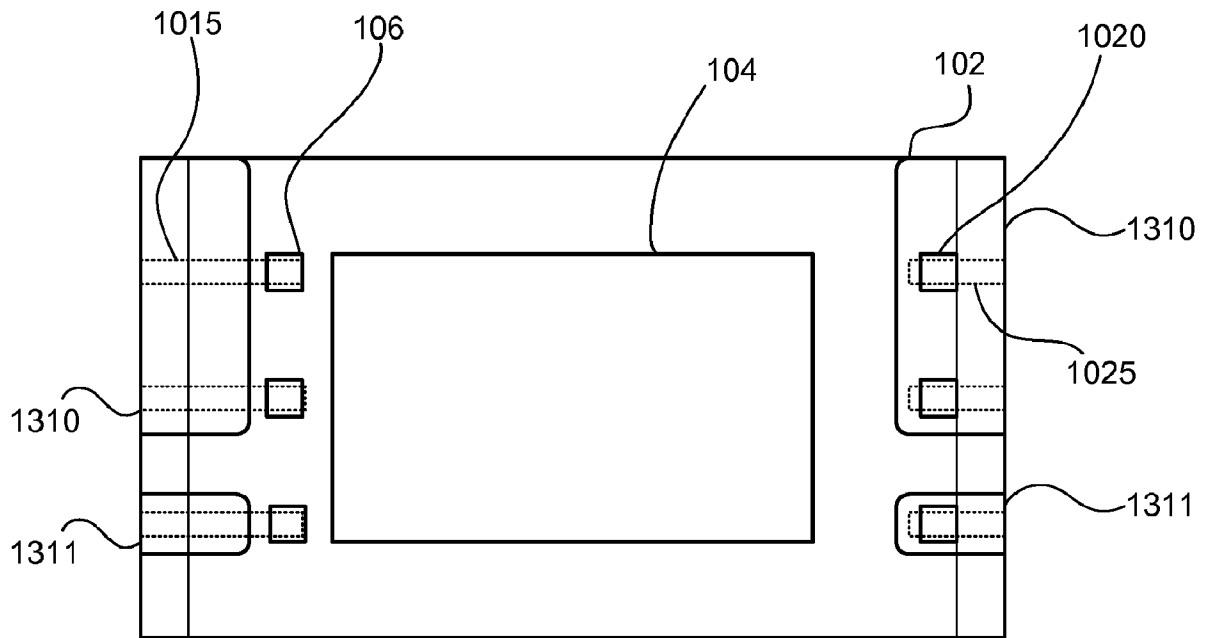


FIG. 13

1300

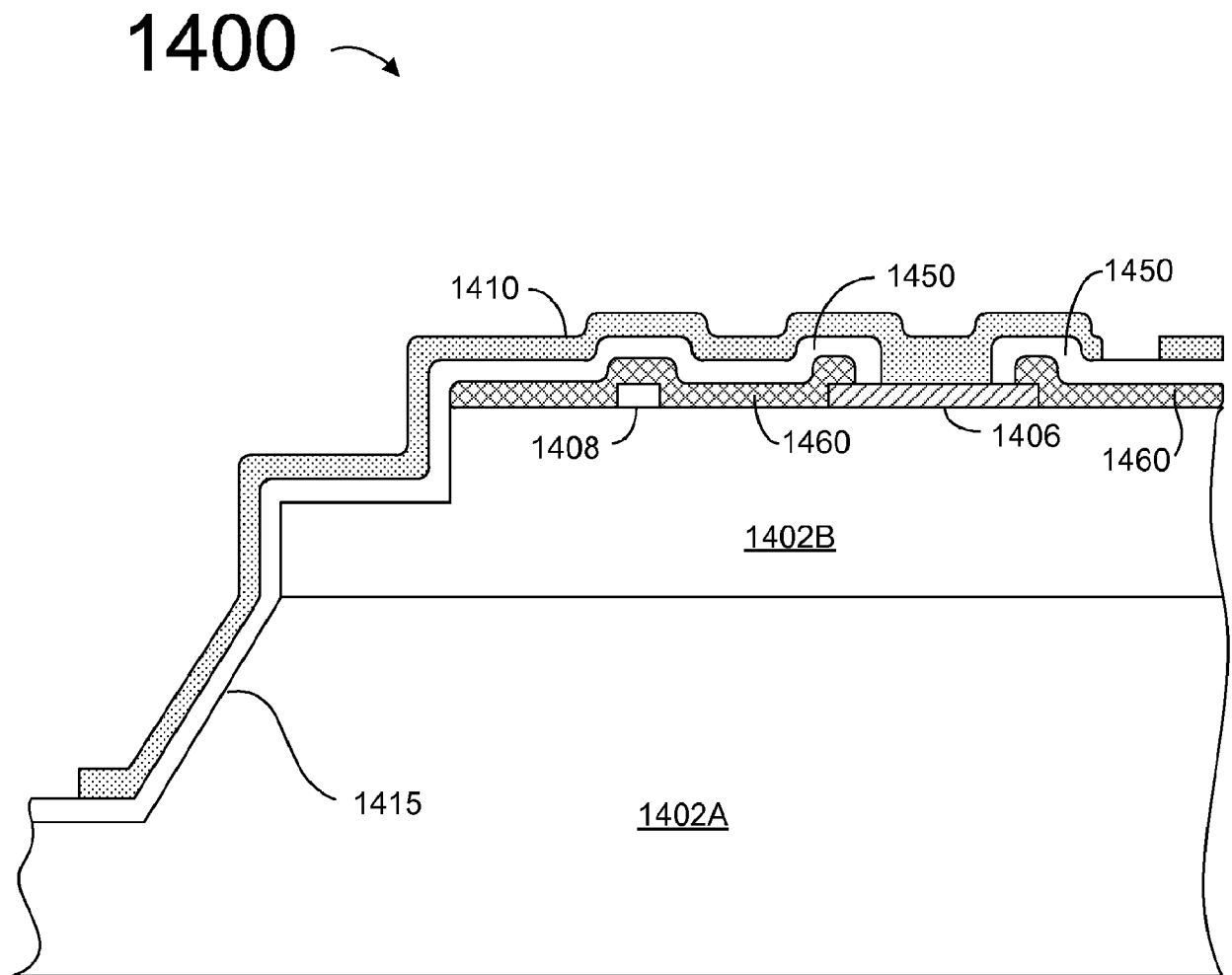


FIG. 14

1500 ↗

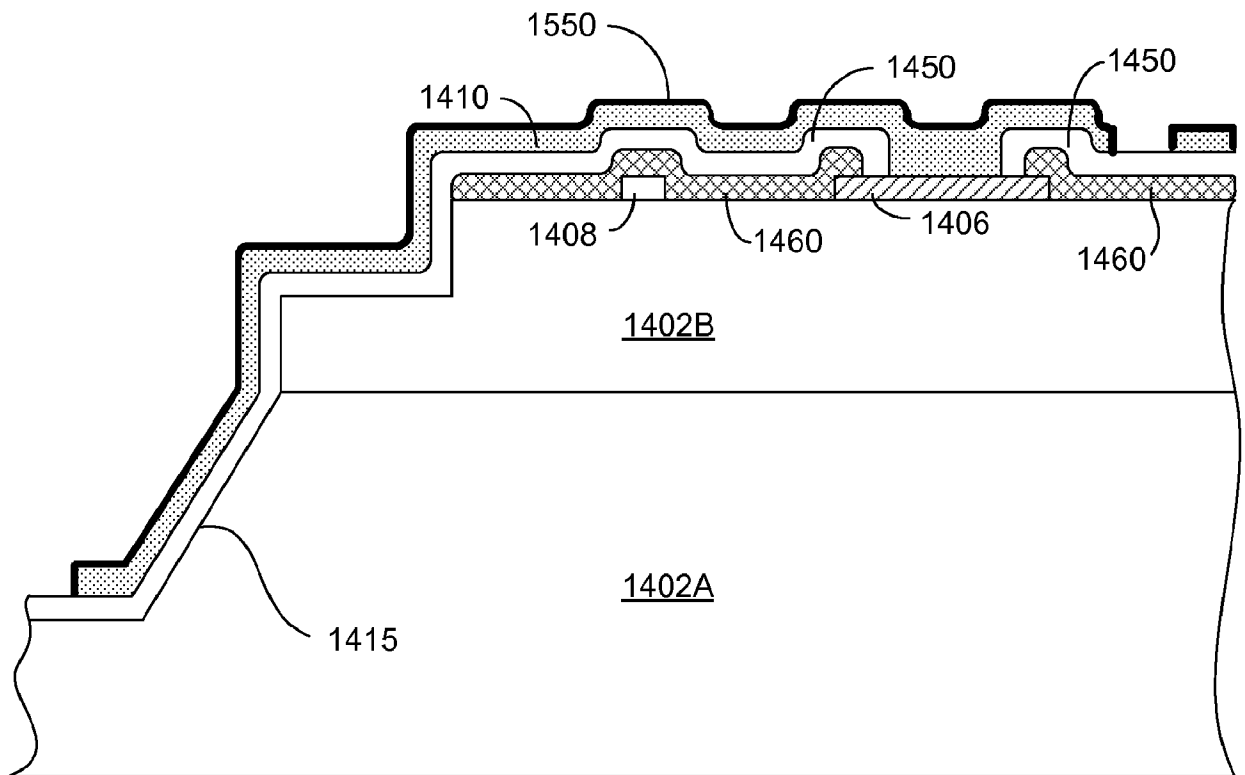


FIG. 15A

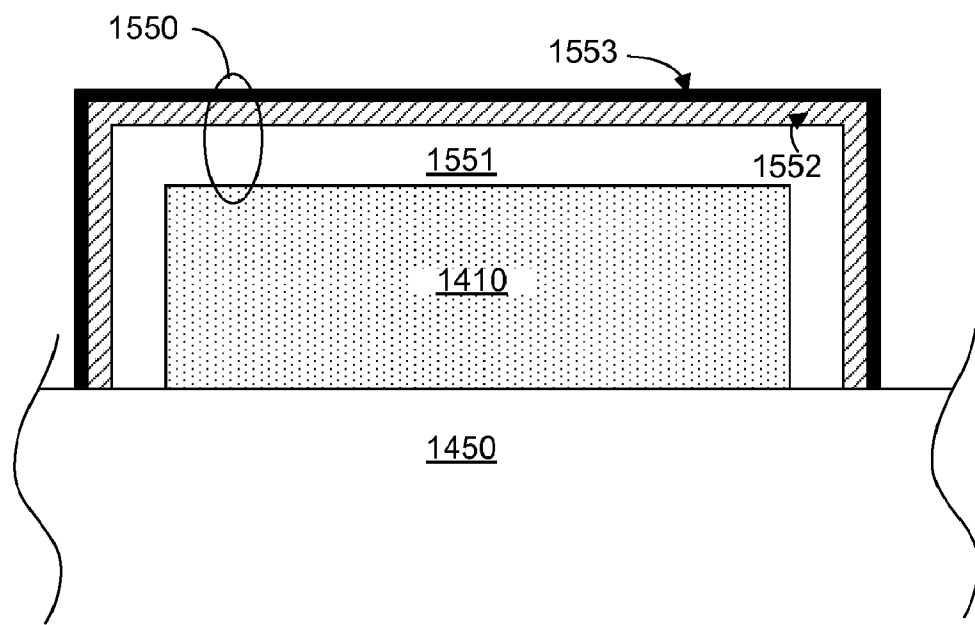


FIG. 15B

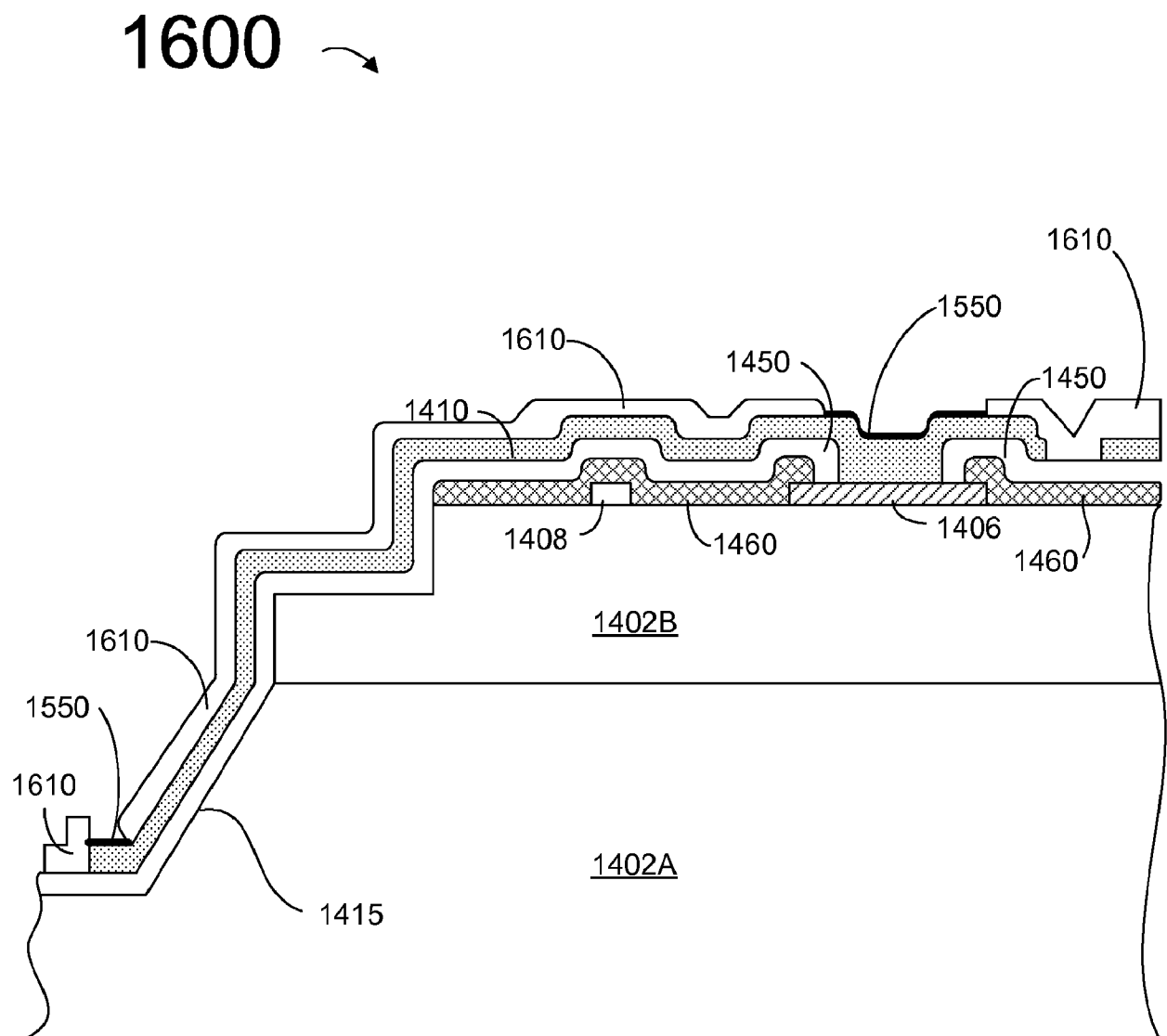


FIG. 16

A. CLASSIFICATION OF SUBJECT MATTER**H01L 23/49(2006.01)i, H01L 25/065(2006.01)i, H01L 25/16(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/49; H01J 31/50; H01L 23/02; H01L 29/06; H01L 23/12; H01J 40/14; H01L 21/08; H01L 31/0232; H01L 31/0203; H01L 25/065; H01L 25/16

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: wire, bonding, pad, low, profile, trench, slope

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7199345 B1 (THOMAS M. MEISEL et al.) 03 April 2007 See column 5, line 20 - column 6, line 58, claim 1 and figures 3a-3b.	1-12, 19-23
Y		13-18
Y	US 8089142 B2 (MICHAEL BROOKS) 03 January 2012 See column 2, line 58 - column 3, line 59, claim 1 and figure 2.	13-18
A	US 4622574 A (ENRIQUE GARCIA) 11 November 1986 See column 3, line 24 - column 4, line 26, claim 1 and figure 1.	1-23
A	US 7084474 B2 (CHIA-YU HUNG et al.) 01 August 2006 See column 10, lines 10-42, claim 7 and figures 6A-6B.	1-23
A	KR 10-2011-0039299 A (SANDISK CORPORATION) 15 April 2011 See paragraphs [0027]-[0035], claim 1 and figures 9-10.	1-23



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 June 2013 (26.06.2013)

Date of mailing of the international search report

01 July 2013 (01.07.2013)

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City,
302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

CHOI, Sang Won

Telephone No. 82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/035658

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		WO 2009-158533 A3	25.02.2010