ENGINEERING MULTIPLE THRESHOLD VOLTAGES IN AN INTEGRATED CIRCUIT

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ABSTRACT

An integrated circuit and method for forming an integrated circuit. There are at least three field-effect transistors with at least two of the field-effect transistors having the same electrically insulating material which is ferroelectric when unstrained or is capable of being ferroelectric when strain is induced. It is optional for the third field-effect transistor to have an electrically insulating material which is ferroelectric when unstrained or is capable of being ferroelectric when strain is induced. The at least three field-effect transistors are strained to varying amounts so that each of the three field-effect transistors has a threshold voltage, Vt, which is different from the Vt of the two other field-effect transistors.
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RELATED APPLICATION


FIELD OF THE INVENTION

[0002] The present invention relates to integrated circuits, and more particularly, to techniques for combining field-effect transistors (FETs) in an integrated circuit having different threshold voltage requirements from one another.

BACKGROUND OF THE INVENTION

[0003] Integrated circuits now commonly include a wide variety of different transistor types in combination with one another. By way of example, random access memory transistors, such as static random access memory (SRAM) or dynamic random access memory (DRAM) transistors, are in many configurations used in combination with a variety of logic transistors. A challenge, however, associated with integrating different transistors is that each type of transistor generally requires a threshold voltage (Vt) that is different from the other types of transistors required. For example, with integrated circuit configurations that combine SRAM and logic transistors, the SRAM transistors typically require a higher Vt than their logic counterparts. This Vt difference is due to the relatively lower power requirements of SRAM transistors as compared to logic transistors.

[0004] In conventional designs, these different Vt requirements may be addressed through doping. Specifically, extra doping steps are performed to alter the Vt of the SRAM transistors relative to the logic transistors, and vice versa. This approach, however, has a notable drawback. Since the Vt of the transistors is determined through doping, the doping must be consistent from one device to another to attain consistent Vt. Dopant fluctuations, which can occur in a significant number of devices produced, lead to variability in the transistors which leads to variability in the devices and thus affects device performance. As device feature sizes are scaled, the effects of dopant fluctuations and device variability become ever more pronounced.

[0005] Therefore, improved techniques for combining transistors having different Vt requirements would be desirable.

BRIEF SUMMARY OF THE INVENTION

[0006] The various advantages and purposes of the present invention as described above and hereafter are achieved by providing, according to a first aspect of the exemplary embodiments, an integrated circuit comprising: a first field-effect transistor having a gate stack comprising a first electrically insulating material that is ferroelectric and a first level of strain, S1, being induced in the first field-effect transistor gate stack by an element exterior to the first field-effect transistor, the first field-effect transistor having a first threshold voltage, Vt1; a second field-effect transistor having a gate stack comprising a second electrically insulating material that is ferroelectric and a second level of strain, S2, being induced in the second field-effect transistor gate stack by an element exterior to the second field-effect transistor, the second field-effect transistor having a second threshold voltage, Vt2; and a third field-effect transistor having a gate stack comprising a third electrically insulating material that is different from the first and second electrically insulating materials and a third level of strain, S3, the third field-effect transistor having a third threshold voltage, Vt3, wherein the third level of strain, S3, being induced in the third field-effect transistor gate stack; wherein the first and second electrically insulating materials are the same electrically insulating material and wherein the first and second electrically insulating materials and the first, second, and third levels of strain, S1, S2, and S3, are configured to shift at least one of the first, second, and third threshold voltages Vt1, Vt2, and Vt3 relative to each other by a predetermined amount such that Vt1, Vt2, and Vt3 are all set to different predetermined values, wherein S1, S2 and S3 are all greater than zero.

[0007] According to a second aspect of the exemplary embodiments, there is provided an integrated circuit comprising: a first field-effect transistor having a gate stack comprising a first electrically insulating material that is ferroelectric and a first level of strain, S1, being induced in the first field-effect transistor gate stack by an element exterior to the first field-effect transistor, the first field-effect transistor having a first threshold voltage, Vt1; a second field-effect transistor having a gate stack comprising a second electrically insulating material that is ferroelectric and a second level of strain, S2, being induced in the second field-effect transistor gate stack by an element exterior to the second field-effect transistor, the second field-effect transistor having a second threshold voltage, Vt2; and a third field-effect transistor having a gate stack comprising a third electrically insulating material that is different from the first and second electrically insulating materials and a third level of strain, S3, the third field-effect transistor having a third threshold voltage, Vt3, wherein the third level of strain, S3, being induced in the third field-effect transistor gate stack; wherein the first and second electrically insulating materials are the same electrically insulating material and wherein the first and second electrically insulating materials and the first, second, and third levels of strain, S1, S2, and S3, are configured to shift at least one of the first, second, and third threshold voltages Vt1, Vt2, and Vt3 relative to each other by a predetermined amount such that Vt1, Vt2, and Vt3 are all set to different predetermined values, wherein S1, S2 and S3 are all greater than zero.

[0008] According to a third aspect of the exemplary embodiments, there is provided an integrated circuit comprising: a first field-effect transistor having a gate stack comprising a first electrically insulating material that is ferroelectric when strain is induced to a first predetermined level, the first field-effect transistor having a first threshold voltage, Vt1; a second field-effect transistor having a gate stack comprising a second electrically insulating material that is ferroelectric when strain is induced to a second predetermined level, the second field-effect transistor having a second threshold voltage, Vt2; and a third field-effect transistor having a gate stack comprising a third electrically insulating material that is different from the first and second electrically insulating materials and a third level of strain, S3, the third field-effect transistor having a third threshold voltage, Vt3, wherein the first and second electrically insulating materials are the same electrically insulating material and wherein the first and second electrically insulating materials and the first, second, and third levels of strain, S1, S2, and S3, are configured to shift at least one of the first, second, and third threshold voltages Vt1, Vt2, and Vt3 relative to each other by a predetermined amount such that Vt1, Vt2, and Vt3 are all set to different predetermined values, wherein S1, S2 and S3 are all greater than zero.
or strained to below the second predetermined level so that the second electrically insulating material is not ferroelectric and wherein the first and second electrically insulating materials are configured to shift $V_1$, relative to $V_2$ and $V_3$, by a predetermined amount such that $V_1$, $V_2$, and $V_3$ are all set to different predetermined values.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The features of the invention believed to be novel and the elements characteristic of the invention are set forth with particularity in the appended claims. The Figures are for illustrative purposes only and are not drawn to scale. The invention itself, however, both as to organization and method of operation, may best be understood by reference to the detailed description which follows taken in conjunction with the accompanying drawings in which:

[0010] FIG. 1 is a cross sectional view of an integrated circuit having a gate stack including a ferroelectric material according to a first embodiment of the present invention.

[0011] FIG. 2 is a cross sectional view of an integrated circuit having a gate stack including a ferroelectric material according to a second embodiment of the present invention.

[0012] FIG. 3 is a cross sectional view of an integrated circuit having a gate stack including a ferroelectric material according to a third embodiment of the present invention.

[0013] FIG. 4 is a cross sectional view of an integrated circuit having a gate stack including a ferroelectric material according to a fourth embodiment of the present invention.

[0014] FIG. 5 is an enlarged cross sectional view of a semiconductor device having a gate stack according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] Disclosed herein are structures and a method of forming a circuit with semiconductor devices having a gate stack including a ferroelectric material. When ferroelectric materials are stressed to different stress levels, the different stress levels give rise to different strain levels which give rise to different polarization states and thus to different $V_t$ values.

[0016] The ferroelectric materials of the present invention are electrically insulating materials that exhibit ferroelectricity when unstrained or exhibit ferroelectricity when strain is induced above a certain threshold level. The ferroelectric materials of the present invention may have a $V_t$ value when they are not stressed and this $V_t$ value is shifted (i.e., changed) to a different $V_t$ value when the ferroelectric materials are strained. As noted above, $V_t$ varies depending on the stress level applied. Thus, as further explained in the following embodiments of the present invention, a range of $V_t$ values may be obtained by applying different levels of stress (and sometimes no stress) to the ferroelectric materials resulting in FETs having a spread of stabilized $V_t$ values that vary from each other by a predetermined amount. Electrically insulating materials useful in the present invention include, but are not limited to, triglycine sulfate (TGS), BaTiO$_3$, Pb(Zr$_x$Ti$_{1-x}$)O$_3$ (PZT), SrH$_2$TaO$_6$ (SHT), SrTiO$_3$ (STO), Ba$_{0.5}$SrTiO$_3$ (BST), PbTiO$_3$, EuTiO$_3$, CaMnO$_3$ (CMO) and BiFeO$_3$. Of these electrically insulating materials, SrTiO$_3$ (STO), EuTiO$_3$, and CaMnO$_3$ are not ferroelectric unless they are strained. When the latter metal compounds are stressed to a threshold level, typically between 100 MPa and several GPa, the electrically insulating materials are strained and become ferroelectric.

[0017] The strain may be induced by applying stress during device processing. This is referred to as process-induced strain. The induced strain may be tensile, compressive, substantially uniaxial or substantially biaxial. The stress may be applied, for example, by a liner layer or by epitaxial silicon germanium (SiGe) or carbon-doped silicon (Si:C) in the source and drain regions. In a preferred embodiment of the present invention, stress is applied to the electrically insulating materials substantially uniaxially by complementary metal-oxide-semiconductor (CMOS) technology-type techniques, so as to induce a strain that is substantially uniaxial. Substantially uniaxial stress is preferred because the stress level and direction can be chosen independently for different semiconductor devices in the integrated circuit. “Substantially uniaxial,” as used herein, describes a strain introduced in one direction of a surface, such as an x-direction or a y-direction. This is in contrast to, for example, a biaxial strained film that has strain introduced in two directions (x-y) along its surface. It should be understood, however, that “substantially uniaxially” may also describe strain primarily along one axis (e.g., the x-axis) with some minimal, “de minimis,” or non-zero strain component along the other axis. In addition, “CMOS technology-type” techniques as described herein may include, for example, source/drain silicon germanium (SiGe) or carbon-doped silicon (Si:C) regions adjacent a silicon channel region, nitride liner formation, and combinations thereof.

[0018] For purposes of illustration and not limitation, the induced strain shown in FIGS. 1 to 4 is compressive and substantially uniaxial.

[0019] The integrated circuits according to the present invention are formed on a semiconductor substrate made from a semiconductor material. The semiconductor material may be any semiconductor material including but not limited to group IV semiconductors such as silicon, silicon germanium or germanium, a III-V compound semiconductor, or a II-VI compound semiconductor.

[0020] In each of FIGS. 1 to 4 which illustrate a portion of an integrated circuit, there are shown only three semiconductor devices although it should be understood that in practice, the integrated circuit will have many more semiconductor devices.

[0021] Referring to the Figures in more detail, and particularly referring to FIG. 1, there is shown a first embodiment of an integrated circuit 10 which includes semiconductor devices 12, 14, 16 formed in semiconductor substrate 18. Semiconductor device 12 includes a gate stack 20, sidewall spacers 24 adjacent to the gate stack 20, source region 28 and drain region 30. The semiconductor device 12 may be formed between shallow trench isolation regions 26. The gate stack 20 includes an electrically insulating material 22 which is ferroelectric as shown in semiconductor device 12. A stress is imposed on the gate stack 20 as indicated by arrow 29 to result in an induced strain which gives rise to a polarization state as indicated by arrow 32. The stress may be imposed by any type of stress-induced means such as those mentioned above and is preferably substantially uniaxially applied. In the event of semiconductor device 12 in FIG. 1, the stress is imposed by silicon nitride layer 34.

[0022] Semiconductor device 14 is similar to semiconductor device 12 in that semiconductor device 14 includes a gate stack 20, sidewall spacers 24 adjacent to the gate stack 20, source region 28 and drain region 30. The semiconductor device 14 may be formed between shallow trench isolation
regions 26. The gate stack 20 includes an electrically insulating material 22 which is ferroelectric as shown in semiconductor device 14. In a most preferred embodiment of the present invention, the electrically insulating material 22 in semiconductor device 14 is the same as electrically insulating material 22 in semiconductor device 12. A stress is imposed on the gate stack 20 as indicated by arrow 31 to result in an induced strain which gives rise to a polarization state as indicated by arrow 38. There is a different level of stress imposed on gate stack 20 of semiconductor device 14 to result in a different polarization state as represented by the different size of arrow 38 compared to arrow 32 of semiconductor device 12. The stress may be imposed by any type of process-induced means such as those mentioned above and is preferably uniaxially applied. In the case of semiconductor device 14 in FIG. 1, the stress is imposed by silicon nitride layer 34.

The different levels of stress imposed on gate stack 20 of semiconductor device 12 and gate stack 20 of semiconductor device 14 result in different polarization states and hence different Vt values. A particular advantage of the present invention is that Vt values (Vt1 and Vt2, respectively) for semiconductor devices 12, 14 are less variable and more predictable when compared to other methods of varying Vt values between semiconductor devices.

Integrated circuit 10 further includes a semiconductor device 16 which includes a gate stack 40, sidewall spacers 24 adjacent to the gate stack 40, source region 28 and drain region 30. The semiconductor device 16 may be formed between shallow trench isolation regions 26. The gate stack 40 in one embodiment includes an electrically insulating material 44 that may be ferroelectric when unstrained or may become ferroelectric when strain is induced. The electrically insulating material 44 in gate stack 40 is different than electrically insulating materials 22 in gate stacks 20 in semiconductor devices 12, 14. The gate stack 40 in one preferred embodiment is stressed as indicated by arrow 39 to result in an induced strain which gives rise to a polarization state as indicated by arrow 42. The stress imposed on gate stack 40 is less than the stress imposed on gate stacks 20 in semiconductor devices 12, 14 to result in a different polarization state as indicated by the size of arrow 42. In one preferred embodiment of the invention, the stress imposed on semiconductor device 16 may be a very minimal amount or zero. In another preferred embodiment of the present invention, the semiconductor device 16 does not contain the electrically insulating material 44 so that the gate stack 40 may not have any ferroelectric properties.

Regardless of whether semiconductor device 16 has an electrically insulating material that is or can be ferroelectric, the semiconductor device 16 will have a Vt that is different from Vt1 for semiconductor device 12 and Vt3 for semiconductor device 14.

Referring to FIG. 2, there is shown a second embodiment of an integrated circuit 100 which includes semiconductor devices 112, 114, 116 formed in semiconductor substrate 118. Semiconductor device 112 includes a gate stack 120, sidewall spacers 124 adjacent to the gate stack 120, source region 128 and drain region 130. The semiconductor device 112 may be formed between shallow trench isolation regions 126. The gate stack 120 includes an electrically insulating material 122 which is ferroelectric. A stress is imposed on the gate stack 120 as indicated by arrow 129 to result in an induced strain which gives rise to a polarization state as indicated by arrow 132. The stress may be imposed by any type of process-induced means such as those mentioned above and is preferably substantially uniaxially applied. In the case of semiconductor device 112 in FIG. 2, the stress is imposed by silicon nitride layer 134. Semiconductor device 112 has a threshold voltage Vt1.

Semiconductor device 114 is similar to semiconductor device 112 in that semiconductor device 114 includes a gate stack 120, sidewall spacers 124 adjacent to the gate stack 120, source region 128 and drain region 130. The semiconductor device 114 may be formed between shallow trench isolation regions 126. The gate stack 120 includes an electrically insulating material 122 which is not ferroelectric as shown in semiconductor device 114. In a most preferred embodiment of the present invention, the electrically insulating material 122 in semiconductor device 114 is the same as electrically insulating material 122 in semiconductor device 112. However, gate stack 120 (and hence electrically insulating material 122) in semiconductor device 114 is unstressed. Semiconductor device 114 has a threshold voltage Vt2.

Due to the stress imposed on gate stack 120 of semiconductor device 112 and no stress (or at least very minimal stress) imposed on gate stack 120 of semiconductor device 114, Vt1 will be different from Vt2 by some predetermined amount which can be calculated from their different polarization values.

Integrated circuit 100 further includes a semiconductor device 116 which includes a gate stack 140, sidewall spacers 124 adjacent to the gate stack 140, source region 128 and drain region 130. The semiconductor device 116 may be formed between shallow trench isolation regions 126. The gate stack 140 in one embodiment includes an electrically insulating material 144 that may be ferroelectric or may become ferroelectric when stressed. The electrically insulating material 144 in gate stack 140 is different than electrically insulating materials 122 in gate stacks 120 in semiconductor devices 112, 114. The gate stack 140 in one preferred embodiment is unstressed (or at least very minimal stress). In another preferred embodiment of the present invention, the semiconductor device 116 does not contain the electrically insulating material 144 so that the gate stack 140 may not have any ferroelectric properties.

Regardless of whether semiconductor device 116 has an electrically insulating material that is or can be ferroelectric, the semiconductor device 116 will have a Vt that is different from Vt1 for semiconductor device 112 and Vt2 for semiconductor device 114.

Referring to FIG. 3, there is shown a third embodiment of an integrated circuit 200 which includes semiconductor devices 212, 214, 216 formed in semiconductor substrate 218. Semiconductor device 212 includes a gate stack 220, sidewall spacers 224 adjacent to the gate stack 220, source region 228 and drain region 230. The semiconductor device 212 may be formed between shallow trench isolation regions 226. The gate stack 220 includes an electrically insulating material 222 which is not ferroelectric until it is stressed above a certain level to induce ferroelectricity. A stress of sufficient magnitude is imposed on the gate stack 220 as indicated by arrow 229 to induce ferroelectricity in the electrically insulating material 222. The polarization state of the ferroelectric electrically insulating material 222 is indicated by arrow 232. The stress may be imposed by any type of process-induced means such as those mentioned above and is
Semiconductor device 214 is similar to semiconductor device 212 in that semiconductor device 214 includes a gate stack 220, sidewall spacers 224 adjacent to the gate stack 220, source region 228 and drain region 230. The semiconductor device 214 may be formed between shallow trench isolation regions 226. The gate stack 220 includes an electrically insulating material 222 which is not ferroelectric until it is stressed above a certain level to induce ferroelectricity. In a most preferred embodiment of the present invention, the electrically insulating material 222 in semiconductor device 214 is the same as electrically insulating material 222 in semiconductor device 212. However, gate stack 220 (and hence electrically insulating material 222) in semiconductor device 214 is unstressed or at least stressed at a low enough level that ferroelectricity is not induced in electrically insulating material 222. Semiconductor device 114 has a threshold voltage $V_{t1}$.

Due to the stress imposed on gate stack 220 of semiconductor device 212 and no stress or low stress below the ferroelectricity threshold imposed on gate stack 220 of semiconductor device 214, $V_{t1}$ will be different from $V_{t2}$ by some predetermined amount which can be calculated from their different polarization values.

Integrated circuit 200 further includes a semiconductor device 216 which includes a gate stack 240, sidewall spacers 224 adjacent to the gate stack 240, source region 228 and drain region 230. The semiconductor device 216 may be formed between shallow trench isolation regions 226. The gate stack 240 in one embodiment includes an electrically insulating material 244 that may be ferroelectric or may become ferroelectric when stressed. The electrically insulating material 244 in gate stack 240 is different than electrically insulating materials 222 in gate stacks 220 in semiconductor devices 212, 214. The gate stack 240 in one preferred embodiment is unstressed or at a stress insufficient to induce ferroelectricity in electrically insulating material 244. In another preferred embodiment of the present invention, the gate stack 240 having the electrically insulating material 244 is stressed sufficiently to induce ferroelectricity. In yet another preferred embodiment of the present invention, the semiconductor device 216 does not contain the electrically insulating material 244 so that the gate stack 240 may not have any ferroelectric properties.

Regardless of whether semiconductor device 216 has an electrically insulating material that is or can be ferroelectric, the semiconductor device 216 will have a $V_{t3}$ that is different from $V_{t1}$ for semiconductor device 212 and $V_{t2}$ for semiconductor device 214.

Referring now to FIG. 4, there is shown a fourth embodiment of an integrated circuit 300. Integrated circuit 300 is similar to integrated circuit 10 previously discussed with respect to FIG. 1 but differs in several respects. Electrically insulating material 44 of semiconductor device 16 is the same as electrically insulating materials 22 of semiconductor devices 12, 14. All of electrically insulating materials 22, 44 are ferroelectric. In addition, a process-induced stress is imposed on semiconductor device 16 as indicated by arrow 42. For purposes of illustration and not limitation, the process-induced stress is imposed on all of the semiconductor devices 12, 14, 16 by silicon nitride layer 34 as indicated as arrows 29, 31, 39, respectively, to result in different induced strain levels which gives rise to different polarization states 32, 38, 42, respectively. The process-induced stress is varied between the semiconductor devices 12, 14, 16 so that the most stress is imposed on semiconductor device 12, followed by the next most stress on semiconductor device 14 and then the least amount of stress on semiconductor device 16. The result is three different values of the threshold voltage, that is, $V_{t1}$, $V_{t2}$ and $V_{t3}$, corresponding to the three different levels of stress imposed on the semiconductor devices 12, 14, 16.

Referring now to FIG. 5, there is shown an enlarged cross section of a semiconductor device. For purposes of illustration and not limitation, the semiconductor device shown may be semiconductor device 12, 14, or 16 in FIG. 1 but is also representative of any of the semiconductor devices in FIGS. 1 to 4. FIG. 5 shows the gate stack 60 in more detail. On either side of the gate stack 60 are spacers 24. The gate stack may include an interfacial layer 50 of SiO$_2$, silicon oxynitride (SiON), or any other dielectric material. Interfacial layer 50 is often present during the formation of the gate stack but is not required for the present invention. The gate stack may further include electrically insulating material layer 56. In the embodiments of the present invention discussed previously, electrically insulating material layer 56 may be a ferroelectric in the unstrained state or an electrically insulating material that is capable of becoming a ferroelectric when stressed above a certain level. In certain embodiments of the present invention, for example certain embodiments of semiconductor device 16, electrically insulating material layer 56 may not be present. The gate stack 60 may include a dielectric layer 52. Lastly, gate stack 60 may further include a gate electrode layer 54 which may be a conductive material or a combination of conductive materials, for example, doped polycrystalline silicon, an elemental or compound metal, or combinations or multilayers thereof.

The semiconductor devices as described with respect to FIGS. 1 to 4 form an integrated circuit. Some of the semiconductor devices may be integrated devices and others of the semiconductor devices may be random access memory devices such as static random access memory (SRAM) or dynamic random access memory (DRAM). In one preferred embodiment of the present invention, all of the semiconductor devices may be field-effect transistors (FETs). An important aspect of the present invention is that the present inventors have disclosed a methodology for achieving multiple $V_{t}$ values so that the different $V_{t}$ requirements of logic and random access memory devices are addressed in a predictable way.

It will be apparent to those skilled in the art having regard to this disclosure that other modifications of this invention beyond those embodiments specifically described here may be made without departing from the spirit of the invention. Accordingly, such modifications are considered within the scope of the invention as limited solely by the appended claims.

We claim:

1. An integrated circuit comprising:
   a first field-effect transistor having a gate stack comprising a first electrically insulating material that is ferroelectric and a first level of strain, $S_1$, being induced in the first field-effect transistor gate stack by an element exterior to the first field-effect transistor, the first field-effect transistor having a first threshold voltage, $V_{t1}$;
a second field-effect transistor having a gate stack comprising a second electrically insulating material that is ferroelectric and a second level of strain, S2, being induced in the second field-effect transistor gate stack by an element exterior to the second field-effect transistor, the second field-effect transistor having a second threshold voltage, V_t2; and

a third field-effect transistor having a gate stack comprising a third electrically insulating material that is different from the first and second electrically insulating materials and a third level of strain, S3, the third field-effect transistor having a third threshold voltage, V_t3, wherein the third level of strain, S3, being induced in the third field-effect transistor gate stack;

wherein the first and second electrically insulating materials are the same electrically insulating material and wherein the first and second electrically insulating materials and the first, second, and third level of strain S1, S2, and S3, are configured to shift at least one of the first, second, and third threshold voltages V_t1, V_t2, and V_t3 relative to each other by a predetermined amount such that V_t1, V_t2, and V_t3 are all set to different predetermined values, wherein S1, S2 and S3 are all greater than zero.

2. The integrated circuit of claim 1 wherein the gate stack in the third field-effect transistor does not comprise an electrically insulating material that is ferroelectric in the third field-effect transistor or can become ferroelectric in the third field-effect transistor when strain is induced in the gate stack.

3. The integrated circuit of claim 1 wherein the gate stack in the third field-effect transistor comprises an electrically insulating material that is ferroelectric in the third field-effect transistor or can become ferroelectric in the third field-effect transistor when strain is induced in the gate stack.

4. The integrated circuit of claim 1 wherein the gate stack in the third field-effect transistor comprises an electrically insulating material that is ferroelectric in the third field-effect transistor only when strain is induced in the gate stack.

5. The integrated circuit of claim 1 wherein the strain induced in the gate stacks of the first, second and third field-effect transistors is substantially uniaxial process-induced strain.

6. The integrated circuit of claim 1 wherein the ferroelectric material is selected from the group consisting of LiTaO_3, Pb(Zr,Ti)O_3 (PZT), SrBi_2Ta_2O_9 (SBTN), SrTiO_3 (STO), BaTiO_3 (BST), PbTiO_3, CaMnO_3, and BiFeO_3.

7. An integrated circuit comprising:

   a first field-effect transistor having a gate stack comprising a first electrically insulating material that is ferroelectric and a first level of strain, S1, being induced in the first field-effect transistor gate stack by an element exterior to the first field-effect transistor, the first field-effect transistor having a first threshold voltage, V_t1;

   a second field-effect transistor having a gate stack comprising a second electrically insulating material that is ferroelectric and a second level of strain, S2, being induced in the second field-effect transistor gate stack by an element exterior to the second field-effect transistor, the second field-effect transistor having a second threshold voltage, V_t2; and

   a third field-effect transistor having a gate stack comprising a third electrically insulating material that is ferroelectric and a third level of strain, S3, the third field-effect transistor having a third threshold voltage, V_t3, wherein the third level of strain, S3, being induced in the third field-effect transistor gate stack;

   wherein the first and second electrically insulating materials are the same electrically insulating material and wherein the first and second electrically insulating materials and the first, second, and third level of strain S1, S2, and S3, are configured to shift at least one of the first, second, and third threshold voltages V_t1, V_t2, and V_t3 relative to each other by a predetermined amount such that V_t1, V_t2, and V_t3 are all set to different predetermined values, wherein S1, S2 and S3 are all greater than zero.

8. The integrated circuit of claim 7 wherein the gate stack in the third field-effect transistor comprises a third ferroelectric material that is the same as the first and second ferroelectric materials wherein S1 is greater than S2 which is greater than S3.

9. The integrated circuit of claim 7 wherein the strain induced in the gate stacks of the first, second and third field-effect transistors is substantially uniaxial process-induced strain.

10. The integrated circuit of claim 7 wherein the ferroelectric in the third field-effect transistor is ferroelectric only when strain is induced in the gate stack.

11. The integrated circuit of claim 7 wherein S1 is greater than S2 which is greater than S3.

12. The integrated circuit of claim 7 wherein the ferroelectric material is selected from the group consisting of BaTiO_3, Pb(Zr,Ti)O_3 (PZT), SrBi_2Ta_2O_9 (SBTN), SrTiO_3 (STO), BaTiO_3 (BST), PbTiO_3, CaMnO_3, and BiFeO_3.

13. An integrated circuit comprising:

   a first field-effect transistor having a gate stack comprising a first electrically insulating material that is ferroelectric when strain is induced to a first predetermined level, the first field-effect transistor having a first threshold voltage, V_t1;

   a second field-effect transistor having a gate stack comprising a second electrically insulating material that is ferroelectric when strain is induced to a second predetermined level, the second field-effect transistor having a second threshold voltage, V_t2; and

   a third field-effect transistor having a gate stack, the third field-effect transistor having a third threshold voltage, V_t3, wherein the first and second electrically insulating materials are the same and the first electrically insulating material is strained to at least the first predetermined level so that the first electrically insulating material is ferroelectric while the second electrically insulating material is unstrained or strained to below the second predetermined level so that the second electrically insulating material is not ferroelectric and wherein the first and second electrically insulating materials are configured to shift V_t1 relative to V_t2 and V_t3 by a predetermined amount such that V_t1, V_t2 and V_t3 are all set to different predetermined values.

14. The integrated circuit of claim 13 wherein the third field-effect transistor comprising a third electrically insulating material that is ferroelectric when strain is induced to a third predetermined level and the third electrically insulating material is different from the first and second electrically insulating materials.

15. The integrated circuit of claim 14 wherein the third electrically insulating material is strained at least to the third
predetermined level so that it is ferroelectric and the strain induced on the first electrically insulating material is greater than the strain induced on the third electrically insulating material.

16. The integrated circuit of claim 15 wherein the strain induced in the gate stacks of the first, second and third field-effect transistors is substantially uniaxial process-induced strain.

17. The integrated circuit of claim 13 wherein the gate stack in the third field-effect transistor does not comprise an electrically insulating material that is ferroelectric in the third field-effect transistor or can become ferroelectric in the third field-effect transistor when strain is induced in the gate stack.

18. The integrated circuit of claim 13 wherein the first and second electrically insulating materials are ferroelectric only when strain is induced in the gate stack in a predetermined amount, S1 is greater than S2 such that the first electrically insulating material is ferroelectric and the second electrically insulating material is not ferroelectric.

19. The integrated circuit of claim 18 wherein the gate stack in the third field-effect transistor does not comprise an electrically insulating material that is ferroelectric in the third field-effect transistor or can become ferroelectric in the third field-effect transistor when strain is induced in the gate stack.

20. The integrated circuit of claim 13 wherein the first, second and third electrically insulating materials are selected from the group consisting of SrTiO₃ (STO), EuTiO₃, and CaMnO₃ (CMO).