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(71) Applicant: **MIMOS BERHAD** [MY/MY]; Technology Park Malaysia, 57000 Kuala Lumpur (MY).

(72) Inventors: **ABD WAHID Khairul Anuar Bin**; c/o MIMOS BERHAD, Technology Park Malaysia, 57000 Kuala Lumpur (MY). **LEE, Wai Yee**; c/o MIMOS BERHAD, Technology Park Malaysia, 57000 Kuala Lumpur (MY). **Daniel BIEN Chia Sheng**; c/o MIMOS BERHAD, Technology Park Malaysia, 57000 Kuala Lumpur (MY). **ABD RASHID Amirul Bin**; c/o MIMOS BERHAD, Technology Park Malaysia, 57000 Kuala Lumpur (MY).

(74) Agent: **MIRANDAH, Patrick**; Patrick Mirandah Co. (Malaysia) Sdn Bhd, Suite 3B-19-3 Plaza Sentral, Jalan Stesen Sentral 5, 50470 Kuala Lumpur (MY).

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[Continued on next page]

(54) Title: METHOD OF FORMING NANOMATERIALS ON PACKAGED DEVICE PLATFORM

(57) Abstract: A method of forming nanomaterials (10) on packaged sensor-device platform, the method comprising the steps of fabricating (11) a sensor device platform on full scale wafer to form a fully packaged sensor device platform for nanomaterials forming process (10) which comprises the steps of protecting the wire bond with epoxy while leaving the sensing area exposed for receiving coating of catalyst precursor for the nanomaterial growth, nucleating (1.6) the coated catalyst precursor at low temperature for forming an active nanoparticle, and providing the active nanoparticle nucleation with nutrient solution for turning them into solid and forming nanostructures for integration of readout circuit for sensing.

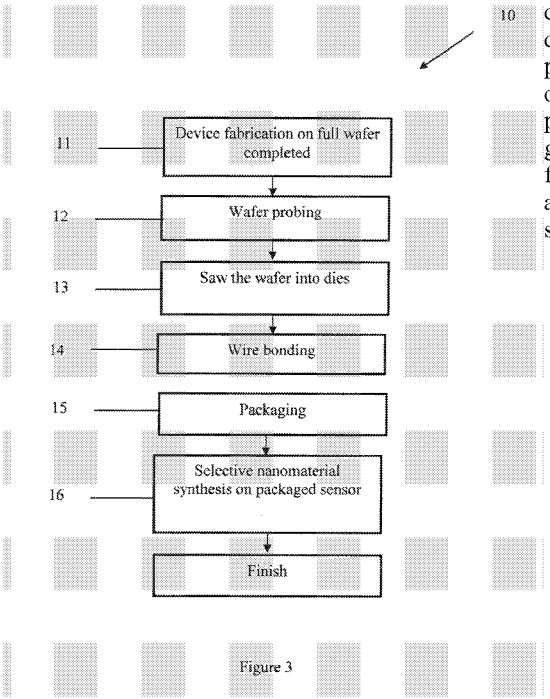

Figure 3

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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

Method of Forming Nanomaterials on Packaged Device Platform

Field of Invention

The present invention relates generally to a method of forming nanomaterials on packaged device, and more particularly, to a method to form nanomaterials on packaged device at low temperature and the forming process is separated from wafer fabrication manufacturing line.

Background of the Invention

The use of nanomaterial as a sensing element has attracted vast attention since it can remarkably enhance the sensor performance especially in term of sensitivity and resolution. This is because of the quality of material properties at nanoscale size as well as the factor of high surface area to volume ratio. Due to these reasons, many industries are now starting to utilize nanomaterials to increase their sensor performance.

The nanomaterial synthesis method generally grouped into wet chemical based and gaseous-vapor based. The wet chemical method such as hydrothermal synthesis is considered a cost efficient process since it requires a very low synthesis

temperature and a simple synthesis set-up. However, the main challenge arises when using hydrothermal method is the accumulated residue in the growth solution during growth process in the form of particles, dust or flakes. These residues are not allowed to exist in wafer fab process in order to prevent any contamination that will lead to defects and yield loss. Another problem arises in hydrothermal method is the selective growth process.

In comparison to the gaseous-vapor method, the thickness of catalyst required for the gaseous-vapour method is only a few nanometer while for hydrothermal is in a few microns. Such thick catalyst is hard to be removed via typical lift-off process. As a result, the nanomaterial will grow at sensing areas and at other device areas as well, such as electrical contact pads which will affect the wire bonding and packaging process.

The gaseous-vapor synthesis method can be done via Chemical Vapor Deposition (CVD). In CVD process, several gaseous precursors will employed such as Ar, O_2, H_2, NH_3 and nanomaterial gas precursor. However, with CVD, a high synthesis temperature is required which is typically above 400^0C in vacuum condition with high precision gas flow ratios. Such high temperature will limit the type of metal

electrode that can be used in the sensor element while high precision gas flow rate is very hard to control and this will affect the uniformity of nanomaterial on full wafer. Besides, some type of metal catalyst used to assist nanomaterial growth in CVD process such as gold is not compatible with integrated circuit wafer fabrication processes. It is known in wafer fabrication industries that the heavy metal such gold will introduce electrical states into silicon wafer which act as trap for charge carrier which in return will degrade the performance of integrated circuit conductivity.

Therefore the present invention discloses a method of forming nanomaterial on packaged devices at low temperature and the nanomaterial will be formed at separate process from wafer fabrication manufacturing line. Thus, the contamination issues, uniformity, tight process control, wire bonding and packaging problem can be avoided. In the present invention, the device platform such as interdigitated electrodes (IDEs) and field effect transistors (FETs) will be packaged first and the nanomaterial such as nanowires or nanoplatlets will be formed on it thereafter. The process allows the use of printed circuit board (PCB) as the packaging materials as it

is typically not able to withstand temperatures of above 200°C.

Summary of Invention

In view of foregoing, embodiments herein provide a method of forming nanomaterials on packaged device platform.

A method of forming nanomaterials on packaged sensor device platform comprises the steps of fabricating a sensor device platform on full scale wafer, sawing the wafer to individual sensor die element, bonding of conductive wires for connecting the sensor element to the sensor device package, protecting the wire bond with epoxy while leaving the sensing area exposed for receiving coating of catalyst precursor for the nanomaterial growth, nucleating the coated catalyst precursor at low temperature for forming an active nanoparticle, and providing the active nanoparticle nucleation with nutrient solution for turning them into solid and forming nanostructures for integration of readout circuit for sensing.

Preferably the method further comprises the step of testing and qualifying the device sensor platform at full scale

wafer by charactering the device electrical properties after the step of fabricating.

Preferably the step of nucleating comprises the step of heating the coated catalyst precursor die on hotplate for surface treatment and annealing the die for activating it to form the active nanoparticle.

Preferably the packaged device sensor platform includes interdigitated electrode (IDE) or field effect transistor (FET).

Preferably the readout circuit includes analogue or digital circuit.

Preferably the nanomaterials include nanotubes, nanowires, nanorods, or nanoplatlets.

These and other objects and features of the present invention will be more fully understood from the following detailed description which should be read in light of the accompanying drawings in which corresponding reference numerals refer to corresponding parts throughout the several views.

Brief Description of the Drawings

Figure 1 shows a typical synthesis or forming method (100) to integrate nanomaterials on device platform;

Figure 2a depicts an example of the nanomaterial synthesis on full wafer that is not uniformed with other typical synthesis or forming method;

Figure 2b illustrates an example of the nanomaterial synthesis with residue particles that will lead to contamination in manufacturing line with other typical synthesis or forming method;

Figure 2c shows an example of the nanomaterial growth on device contact pad with other typical synthesis or forming method;

Figure 3 is a flowchart showing a method to form nanomaterials on packaged sensor devices at low temperature where the synthesis process is carried out in separate process from wafer fabrication manufacturing line of the present invention; and

Figure 4 is a process flow showing the diagrams of the present method to form nanomaterial on packaged device.

Detailed Description of the Preferred Embodiments

To facilitate an understanding of the principles and features of the invention, it is explained hereinafter with reference to its implementation in illustrative embodiments. In more detail, the present invention is directed to a method to form nanomaterial on packaged device at low temperature in which the nanomaterial forming process is separated from wafer fabrication manufacturing line. By using this method, it can eliminate the risks of contamination, non-uniformity, inconsistency, peel off problem, wire bonding and packaging problem, and defects on wafer fabrication equipment.

Figure 1 shows a typical synthesis or forming method (100) to integrate nanomaterials on device platform in which the nanomaterials could be the nanotubes, nanowires, nanorods, nanoplatlets and nanoparticles. The device platform such as the interdigitated electrode (IDE) and field effect transistor (FET) platform is first prepared on full wafer (110) where all the fabrication process has been carried out in wafer fabrication manufacturing line as shown in Figure

1. The device will be checked for its qualification by using a standard integrated circuit (IC) test such as wafer probing (120) to measure the resistance, capacitance and IV characteristics. The nanomaterial will then be synthesized on full wafer (130) either by using wet chemical based or gas based method in which the wet chemical based method will introduce contamination during synthesis process that is not allowed in wafer fabrication manufacturing line.

Whereas in the gas based method, the catalyst in hydrothermal method is very difficult to remove by using typical lift off process hence will affect the wire bonding and packaging process. Besides that, the gaseous-vapour method requires very high temperature synthesis temperature of typically above 400°C, which in turns limits the type of metal that can be used as electrodes in the device platform and the examples of such high temperature metals are gold and platinum which is very expensive. Moreover, the gas based method needs a very high precision gas flow rate into the chamber in vacuum state, otherwise it will affect the uniformity of nanomaterial synthesis on full wafer. Figure 2a to 2c show the examples of issues that occurred when integrating nanomaterials at wafer level in which Figure 2a showing the nanomaterial synthesis on full wafer that is not uniform, Figure 2b showing the residue particles that will

lead to contamination in manufacturing line and Figure 2c showing the nanomaterial growth on device contact pad.

A method of forming nanomaterials (10) on packaged sensor devices at low temperature where the forming process is carried out in separate process from wafer fabrication manufacturing line is shown in Figure 3. The nanomaterial is used as sensing elements to detect different type of ions. The low synthesis temperature could be below 200°C. The nanomaterials could be the nanotubes, nanowires, nanorods, and nanoplatlets. Preferably, the nanomaterial in the present invention is conductive metal oxide nanowire which is formed at temperature as low as 80°C.

The complete device platform such as IDEs or FETs is fabricated on full scale wafer (11) as shown in Figures 3 and 4. The fabrication could be with standard integrated circuit processing technique and flow which includes photolithography, etching and metal deposition. This device platform will be fabricated in wafer fabrication manufacturing line after all the process condition has been standardized.

Then, the device on full wafer level will be tested and qualified by standard electrical testing (12) to check but

not limited to the overall resistance, capacitance and current-voltage characteristics. The passed wafer will be sent for wafer sawing process (13) where the wafer will be sawn into dies where each die represents an individual sensor platform for subsequent device packaging. The dies then sent for wire bonding (14) and pre-packaged (15) comprising of printed circuit boards or ceramic boards to complete the sensor circuit design. The wire bond will be protected with epoxy while sensing area remains exposed (17) for nanomaterial growth as sensing element as shown in Figure 4.

After that, the nanomaterial is formed on die (16) at the final stage where the forming process will be carried out at separate process from wafer fabrication manufacturing line as shown in Figure 4. The exposed sensor area will then be coated with a catalyst precursor as a seed for nanomaterial growth. Preferably, the spinner is rotated at 3000rpm for 30 second for the catalyst precursor coating. The coated pre-packaged dies will then be heated up on hotplate at about 90°C for surface treatment. After that, the pre-packaged dies will anneal at about 100°C for approximately 1 hour to activate the nucleation sites of catalyst to form the active nanoparticle seed. The annealed pre-packaged dies will then be immersed on nanomaterial nutrition in solution that has

been heated up at 80°C for about 3 to 9 hours. During the immersion, the active nucleation sites will absorb the nutrition from solution and turn them into solid and form the nanostructures. Lastly, the pre-packaged die with nanomaterial at sensing area will be integrated (18) with readout circuit such as analogue or digital circuit and use for intended applications as shown in Figure 4.

By using the method of forming the nanomaterial after the device has been packaged will overcome the problems encountered by other typical methods and also introduces several advantages such as the flexibility of process condition employed during nanomaterial synthesis or forming as different applications may needs different types of nanomaterial structure for optimum sensitivity. Therefore the process condition needs to be changed in order to introduce different types of nanomaterial structures onto the device platform. However, having different and multiple process recipes in a wafer fabrication line is not encouraged as it will affect the process stability and also the production throughput. Hence by forming the nanomaterial on packaged device platform allow both low and high volume production of different sensors catering for different applications. Moreover, by forming the nanomaterial packaged devices will eliminate the potential risk or issue of

nanomaterial peeling off during the wafer back-grinding and sawing process.

While the disclosed system has been particularly shown and described with respect to the preferred embodiments, it is understood by those skilled in the art that various modifications in form and detail may be made therein without departing from the scope of the invention. Accordingly, modifications such as those suggested above but not limited thereto are to be considered within the scope of the invention, which is to be determined by reference to the appended claims.

CLAIMS

1. A method of forming nanomaterials (10) on packaged sensor device platform, said method comprising the steps of:

fabricating (11) a sensor device platform on full scale wafer;

sawing (13) said wafer to individual sensor die element;

bonding (14) of conductive wires for connecting said sensor element to the sensor device package;

protecting said wire bond with epoxy (17) while leaving the sensing area exposed for receiving coating of catalyst precursor for said nanomaterial growth;

nucleating (16) said coated catalyst precursor at low temperature for forming an active nanoparticle; and

providing said active nanoparticle nucleation with nutrient solution for turning them into solid and forming nanostructures for integration of readout circuit (18) for sensing.

2. The method of forming nanomaterials (10) on packaged sensor device platform as claimed in claim 1, wherein said method further comprising the step of testing and qualifying (12) said device sensor platform at full scale wafer by charactering the device electrical properties after the step of fabricating (11).

3. The method of forming nanomaterials (10) on packaged sensor device platform as claimed in claim 1, wherein said step of nucleating (16) comprises the step of heating said coated catalyst precursor die on hotplate for surface treatment and annealing said die for activating it to form the active nanoparticle.

4. The method of forming nanomaterials (10) on packaged sensor device platform as claimed in claim 3, wherein said step of heating on hotplate is preferably at about 90°C for surface treatment.

5. The method of forming nanomaterials (10) on packaged sensor device platform as claimed in claim 1, wherein said packaged device sensor platform includes interdigitated electrode (IDE) or field effect transistor (FET).

6. The method of forming nanomaterials (10) on packaged sensor device platform as claimed in claim 1, wherein said nutrient solution is heated up prior to the step of providing nutrient solution.

7. The method of forming nanomaterials (10) on packaged sensor device platform as claimed in claim 6, wherein said

nutrient solution is preferable heated at about 80°C for about 3 to 9 hours.

8. The method of forming nanomaterials (10) on packaged sensor device platform as claimed in claim 1, wherein said readout circuit includes analogue or digital circuit.

9. The method of forming nanomaterials (10) on packaged sensor device platform as claimed in claim 1, wherein said nanomaterials include nanotubes, nanowires, nanorods, or nanoplatlets.

10. The method of forming nanomaterials (10) on packaged sensor device platform as claimed in claim 1, wherein said sensor device package comprises printed circuit board or ceramic boards.

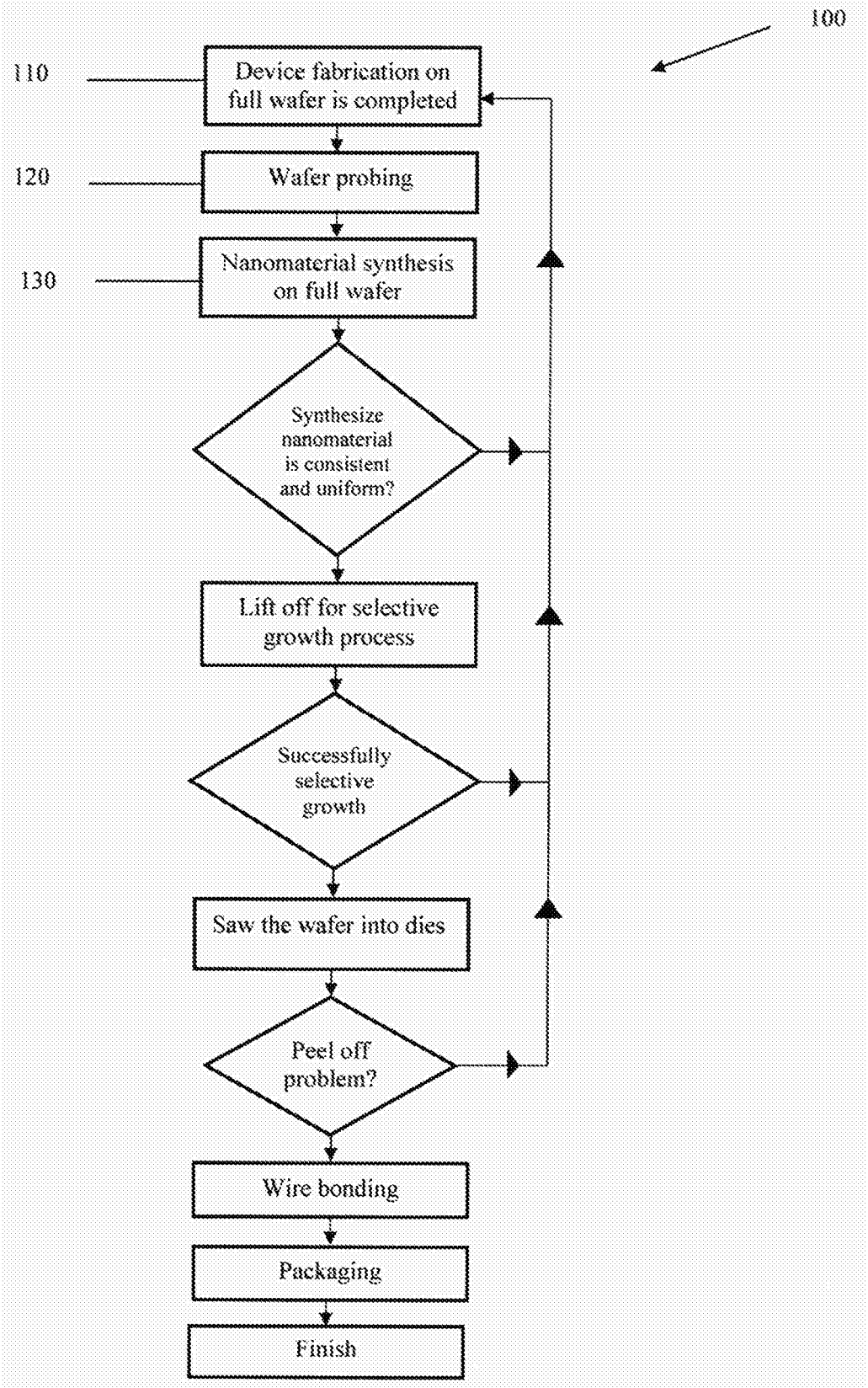

Figure 1 (Prior Art)

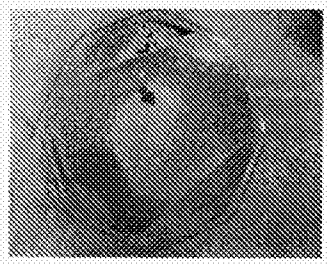

Figure 2a (Prior Art)

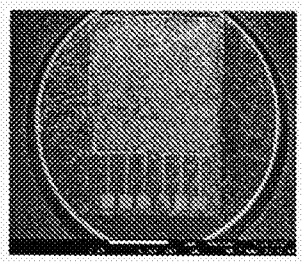

Figure 2b (Prior Art)

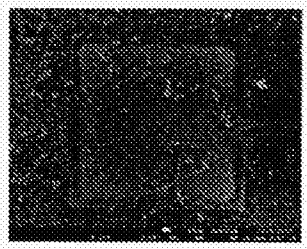

Figure 2c (Prior Art)

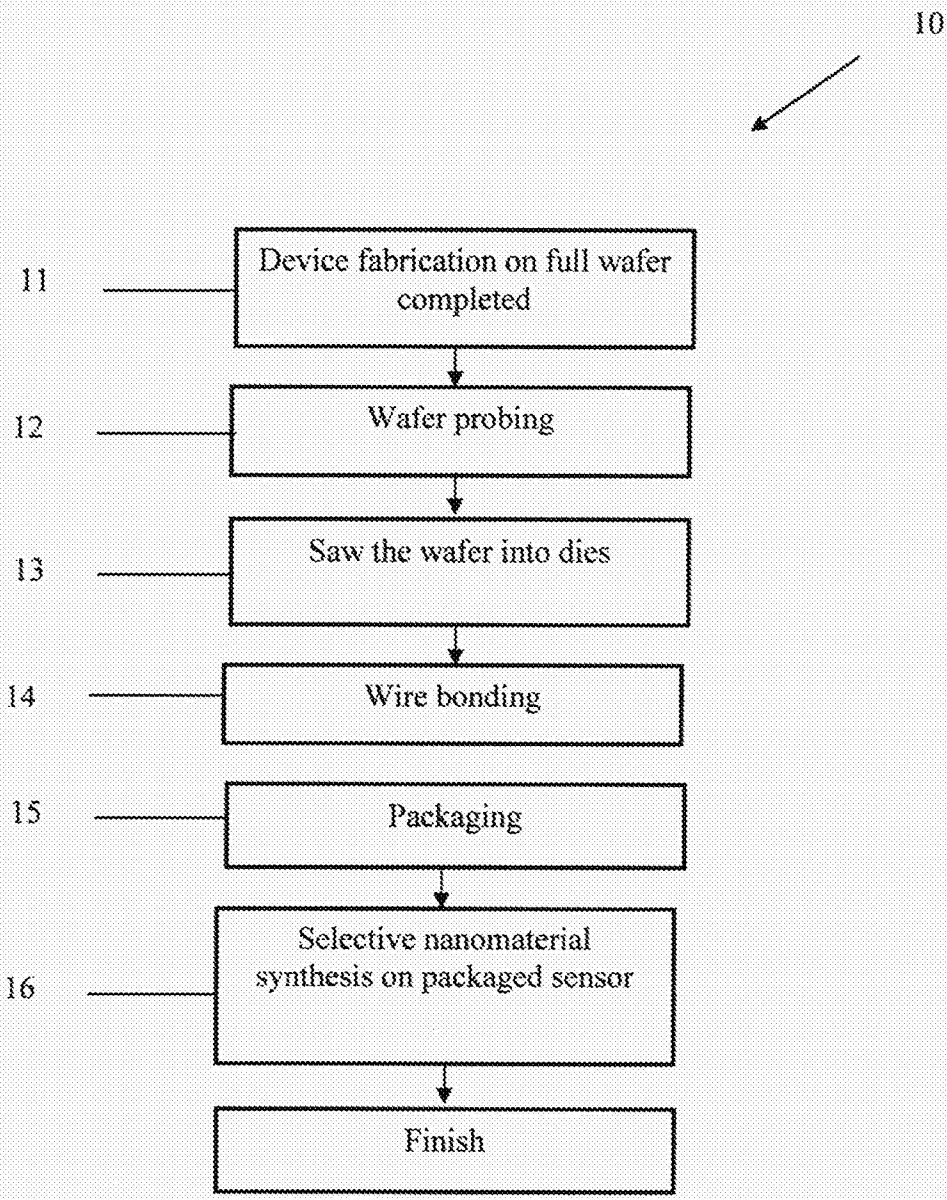
10
11
Device fabrication on full wafer completed
12
Wafer probing
13
Saw the wafer into dies
14
Wire bonding
15
Packaging
16
Selective nanomaterial synthesis on packaged sensor
Finish

Figure 3

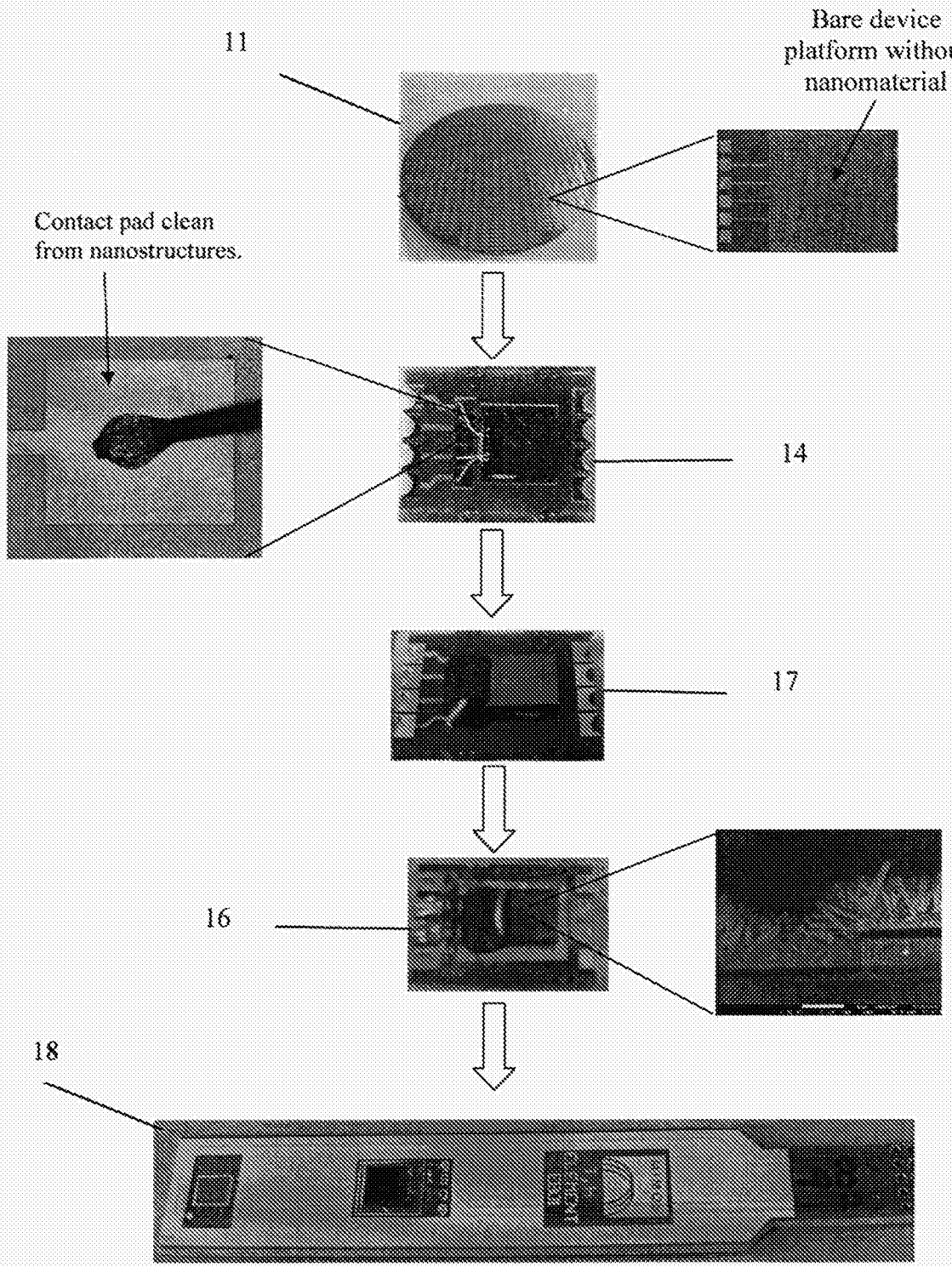
11
Bare device platform without nanomaterial
Contact pad clean from nanostructures.
14
17
16
18

Figure 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/MY2014/000118

A. CLASSIFICATION OF SUBJECT MATTER
INV. B81C1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
B81B B81C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CHANG C-Y ET AL: "Volatile organic compounds sensor with stacked interdigitated electrodes coated with monolayer-protected gold nanoclusters", 2013 TRANSDUCERS & EUROSENSORS XXVII: THE 17TH INTERNATIONAL CONFERENCE ON SOLID-STATE SENSORS, ACTUATORS AND MICROSYSTEMS (TRANSDUCERS & EUROSENSORS XXVII), IEEE, 16 June 2013 (2013-06-16), pages 1170-1173, XP032499191, DOI: 10.1109/TRANSDUCERS.2013.6626981 [retrieved on 2013-10-09] figures 2-5 section "Fabrication" section "Experimental" ----- -/--	1

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 November 2014	18/12/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Meister, Martin

INTERNATIONAL SEARCH REPORT

International application No
PCT/MY2014/000118

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011/210411 A1 (BINAPAL SUKHMINDER S [CA] ET AL) 1 September 2011 (2011-09-01) figure 5 paragraph [0003] -----	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/MY2014/000118

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011210411 A1	01-09-2011	NONE	