

March 2, 1965

R. E. BONNER ETAL

3,171,986

PASSIVE ANALOG HOLDING CIRCUIT

Filed Dec. 31, 1959

2 Sheets-Sheet 1

FIG. 1

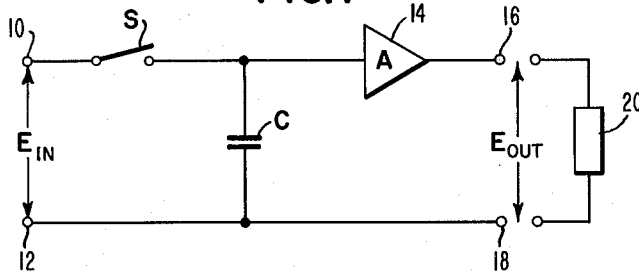


FIG. 2

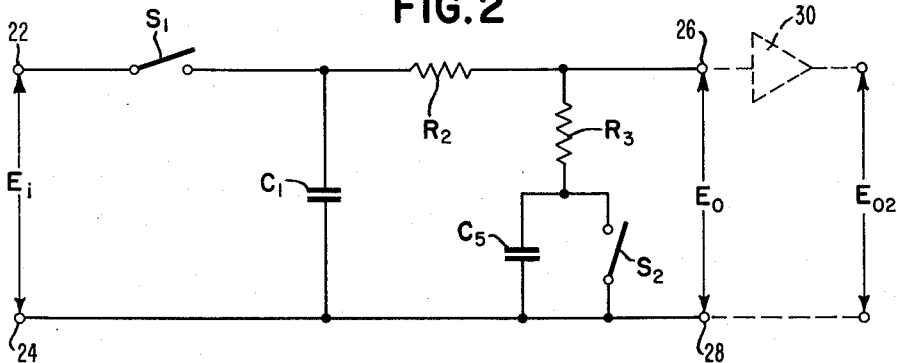
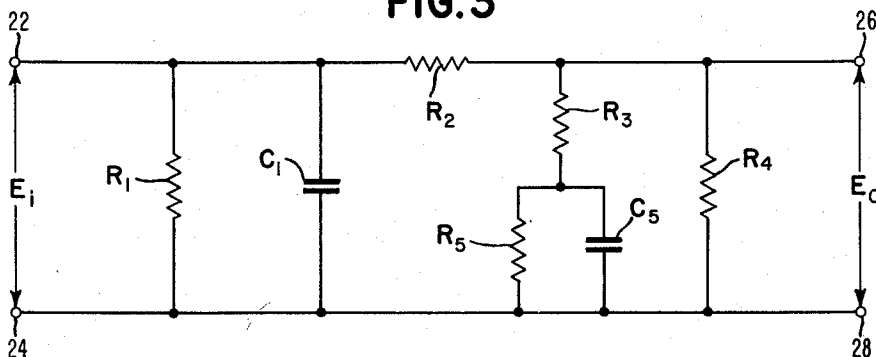


FIG. 3



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FIG. 4

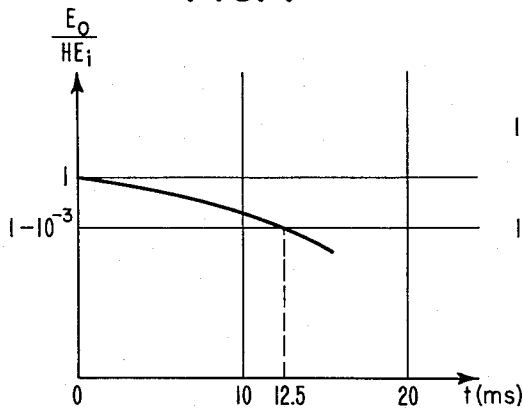


FIG. 5

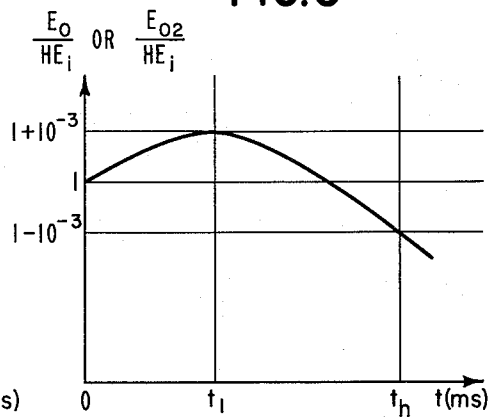
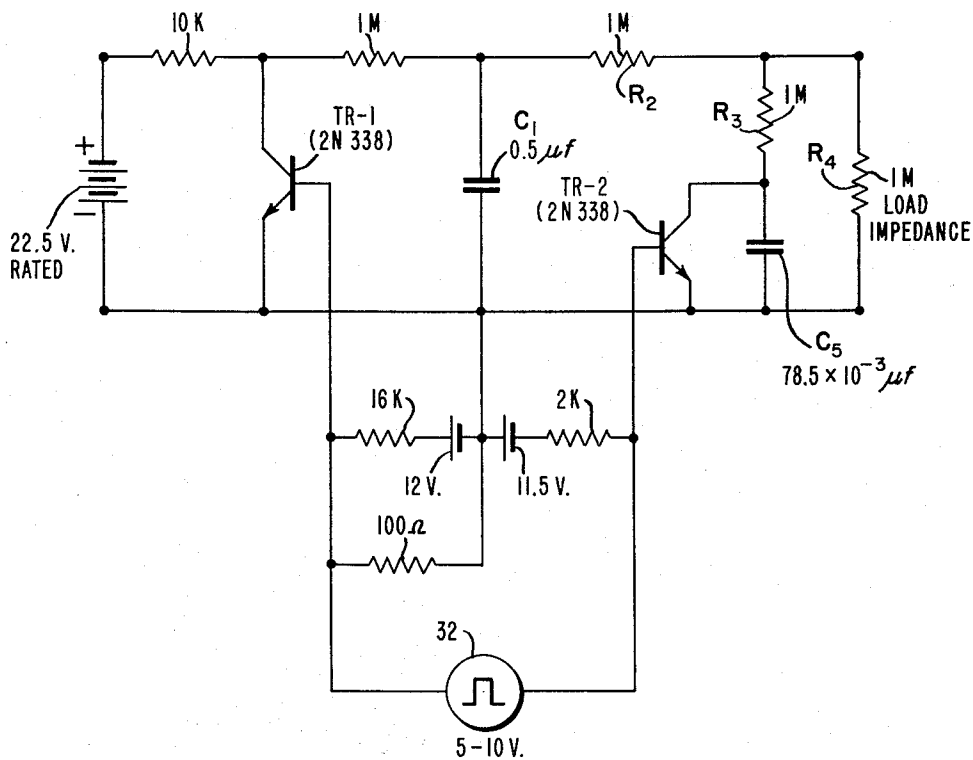


FIG. 6



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PASSIVE ANALOG HOLDING CIRCUIT

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7 Claims. (Cl. 307-109)

This invention relates generally to an analog voltage holding circuit and more specifically to a passive circuit connected to transfer electrical energy between two storage devices so that the output voltage of the circuit remains proportional to an analog input voltage long after the input voltage is removed from the circuit.

Analog voltage holding circuits are broadly well known in the prior art. However, in the past an analog voltage has been held by storing electrical energy in a device, such as a capacitor, and the development of the prior art has been directed toward circuits for keeping the energy stored in this device. The inherent problem of these prior art circuits is that a load must be connected to the storage device in order to utilize the electrical energy stored therein, and as the energy is dissipated through the load, the analog voltage across the storage device decreases and remains substantially equal to the original input analog voltage for only a relatively short time. Therefore, it is the principal object of this invention to provide an analog holding circuit in which the stored energy is purposely discharged from a storage device in order to lengthen the time during which the output voltage of the circuit remains substantially equal or proportional to an input voltage.

Another object of this invention is to provide a circuit for charging and discharging a capacitor so that the circuit output voltage during both charging and discharging is substantially proportional to the circuit input voltage.

A further object is to provide an analog holding circuit having a first capacitor which is charged by an analog input voltage connected thereto and an output circuit including a second capacitor which is charged by the discharge of the first capacitor when the input voltage is disconnected from the circuit.

Still another object of this invention is to provide an analog holding circuit in which a capacitor charged by an input analog voltage is discharged through an output circuit having a second capacitor and a resistor connected in series so that the sum of the voltages developed in the output circuit is proportional to the input analog voltage.

Other objects of the invention will be pointed out in the following description and claims and illustrated in the accompanying drawings which disclose, by way of example, the principle of the invention and the best mode which has been contemplated of applying that principle.

In the drawings:

FIG. 1 shows a typical prior art analog holding circuit; FIG. 2 shows a practical analog holding circuit embodying this invention;

FIG. 3 shows an equivalent circuit representation of FIG. 2;

FIGS. 4 and 5 show curves representing the holding time of circuits embodying this invention; and

FIG. 6 shows a passive holding circuit incorporating transistor switches.

The simplest electrical storage device is a charged capacitor which may hold its voltage for days with fairly good accuracy. A basic prior art circuit utilizing this concept is shown in FIG. 1.

In FIG. 1, an analog input voltage E_{in} is applied

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across input terminals 10 and 12. This voltage is applied through switch S across capacitor C to charge the capacitor to a voltage equal to E_{in} . E_{in} also is applied to the input of amplifier 14 whose output appears across terminals 16 and 18. The output voltage E_{out} of amplifier 14 is directly proportional to E_{in} as long as switch S is closed. A load 20 may be connected across terminals 16 and 18 and represents a utilization circuit to which E_{out} is applied. Amplifier 14 may represent the input amplifier of a following digital voltmeter or merely the input impedance of a network connected to the holding device.

Immediately after switch S is opened, E_{out} remains proportional to E_{in} . However, the capacitor begins to discharge exponentially and, therefore, E_{out} begins to decrease accordingly. If the leakage impedance of the opened switch and the input impedance of amplifier 14 are very large, this change will be slow and a long holding time is possible. When solid state devices are used, however, both the backward impedance of the switch and the input impedance of the amplifier may not be larger than 1M which is too small to be negligible. If we assume a reasonable value for C of 1 uf., the discharging time constant for the capacitor is 0.5 second. This means the time during which E_{out} is accurate within 0.1 percent is only 500 μ s. which is too short for many applications. The circuit shown in FIGS. 2 and 3 enable this holding time to be lengthened considerably, the holding time in an example to be described below being 58 times longer than that of the basic circuit of FIG. 1.

A circuit embodying this invention is shown in FIG. 2 where an input analog voltage E_1 is applied to input terminals 22 and 24 through normally closed switch S_1 to capacitor C_1 . R_2 and R_3 act as a voltage divider and switch S_2 is normally closed so that the output analog voltage E_o appearing across output terminals 26 and 28 is equal to the voltage drop across R_3 and therefore is directly proportional to E_1 .

The closed position of switch S_1 may represent the sampling time of the analog voltage E_1 . Capacitor C_1 also charges to the voltage E_1 while S_1 is closed. C_5 is connected in series with R_3 but is bypassed by switch S_2 .

When the sampling time is terminated, E_1 is removed. This may be represented by the opening of switch S_1 . Switch S_2 is opened simultaneously with switch S_1 . In an actual circuit S_1 and S_2 may be transistor switches. When the two switches are open, capacitor C_1 discharges through R_2 , R_3 and C_5 so that E_o is the voltage developed across R_3 and C_5 . During discharging of C_1 , output voltage E_o may be represented by the following equation:

$$(1) \quad E_o = E_1 \left[\frac{C_1}{C_1 + C_5} + \left(\frac{C_3}{R_2 + R_3} - \frac{C_1}{C_1 + C_5} \right) e^{-\rho t} \right]$$

where

$$(2) \quad \rho = \frac{C_1 + C_5}{C_1 C_5 (R_2 + R_3)}$$

It can be seen that if

$$(3) \quad \frac{R_3}{R_2 + R_3} = \frac{C_1}{C_1 + C_5}$$

then E_o is proportional to E_1 and the holding time is theoretically infinite.

In actual circuit design, the circuit shown in FIG. 2 is not obtainable because of the backward impedance of the switches and the input impedance of the network connected to output terminals 26 and 28 of the holding circuit. In addition, we have to take into account that the holding circuit will have to work repetitively and, therefore, C_5 has to be discharged at the end of each holding cycle by means of the transistor switch S_2 connected across C_5 . The backward impedance of this switch will also

have to be taken into account. Furthermore, it will not be possible to discharge C_5 completely so that we have to take into account its residual voltage E_{50} . A circuit taking into account all these practical considerations is shown in FIG. 3.

In FIG. 3, elements corresponding directly to elements in FIG. 2 carry the same reference characters. In addition, R_1 represents the backward impedance of the open switch S_1 , R_5 represents the backward impedance of open switch S_2 , and R_4 represents the input impedance of an amplifier or other utilization network connected to terminals 26 and 28.

The output voltage E_o for the circuit shown in FIG. 3 is represented by the following equation:

$$(4) \quad E_o = (E_i D + E_{50} F) \frac{e^{-\delta_1/2t} - e^{-\delta_2/1t}}{\delta_1 - \delta_2} + (E_i H + E_{50} G) \frac{\delta_1 e^{-\delta_1 t} - \delta_2 e^{-\delta_2 t}}{\delta_1 - \delta_2}$$

where E_{50} is the residual voltage across capacitor C_5 at $t=0$ (when S_1 is first opened) due to an incomplete discharge at the end of the previous cycle, and D, F, G, H, δ_1 and δ_2 are constants determined by the values of the resistances and capacitors of the circuit. Equations for calculating these constants are presented below.

The above equation may be simplified by using a series for the general term $e^{\delta t}$ as follows

$$(5) \quad e^{-\delta t} = 1 - \frac{\delta t}{1!} + \frac{\delta^2 t^2}{2!} - \frac{\delta^3 t^3}{3!} + \dots$$

For a holding circuit operating with a 0.1 percent accuracy, the time constants $1/\delta_1$ and $1/\delta_2$ must be considerably larger than the maximum holding time of the circuit. In other words,

$$(6) \quad \delta^2 t^2 \ll 1$$

If we then neglect the residual voltage E_{50} appearing across capacitor C_5 at $t=0$, it can then be shown that the output voltage E_o is proportional to the input voltage E_i if C_5 has the following value:

$$(7) \quad C_5 = \frac{C_1}{R_3} \cdot \frac{R_1 R_2 R_4}{R_1 R_4 + R_2 R_4 + R_1 R_3 + R_2 R_3 + R_3 R_4}$$

Using this value of C_5 , it would appear that E_o does not change at all with time, but such a result is true only so long as the assumption $\delta^2 t^2 \ll 1$ remains valid. For a somewhat longer holding time, we must take the square component, $\delta^2 t^2$, into account. Once again assuming that $E_{50}=0$, it can be shown that the output voltage E_o is represented by the following equation.

$$(8) \quad E_o = E_i H (1 - \frac{1}{2} B t^2)$$

where B is a constant determined by the values of the resistances and capacitors in the circuit and may be calculated by an equation presented below.

If we now assume some actual values for the circuit components of FIGURE 3, the holding time for 0.1 percent accuracy may be easily determined. Let us assume that the resistors of FIGURE 3 have a value of 1M and capacitor C_1 has a value of 1 μ f. Capacitor C_5 may then be calculated to have a value of 0.2 μ f. The calculated maximum holding time within 0.1 percent accuracy is, therefore,

$$(9) \quad t_h = 12.5 \text{ ms.}$$

The operation of this holding circuit may be physically represented by plotting

$$\frac{E_o}{HE_i}$$

vs. time as shown in FIG. 4. In FIG. 4, $1-10^{-3}$ represents the minimum allowed deviation of the proportionality of E_o with respect to E_i . It is clearly shown here that the holding time t_h is equal to 12.5 ms.

The maximum holding time of the circuit of FIG. 3

may be increased even more as shown by the plot of FIG. 5. As this plot shows, the output voltage E_o may actually be caused to rise above the input voltage E_i for a portion of the time between $t=0$ when switch S_1 is opened and the maximum holding time t_h , reaching a maximum at some time t_1 . This time t_1 may be calculated by differentiating the general Equation 4 representing the circuit shown in FIG. 3.

For E_{50} assumed to be zero, then

$$(10) \quad \frac{E_o}{HE_i} = 1 + Qt - \frac{1}{2}(B + AQ)t^2$$

and by differentiating,

$$(11) \quad t_1 = \frac{Q}{B + AQ} \text{ (peak value of curve)}$$

where

$$(12) \quad Q = \frac{D}{H} - A$$

$$(13) \quad D = \frac{R_4(R_3 + R_5)}{C_5 R_5 \sum R R}$$

$$(14) \quad H = \frac{R_3 R_4}{\sum R R}$$

$$(15) \quad A = \frac{1}{C_1 C_5 R_1 R_5 \sum R R} [C_1 (R_1 R_2 R_4 + R_1 R_3 R_4 + R_1 R_2 R_3 + R_1 R_2 R_5 + R_1 R_4 R_5) + C_5 (R_1 R_4 R_5 + R_2 R_1 R_5 + R_1 R_3 R_5 + R_2 R_3 R_5 + R_3 R_4 R_5)]$$

$$(16) \quad B = \frac{1}{C_1 C_5 R_1 R_5 \sum R R} (R_1 R_4 + R_2 R_4 + R_1 R_5 + R_2 R_5 + R_4 R_5 + R_1 R_3 + R_2 R_3 + R_3 R_4)$$

$$(17) \quad \sum R R = R_2 R_3 + R_2 R_4 + R_3 R_4$$

For any desired value of

$$\frac{E_o}{HE_i}$$

i.e.,

$$1 \pm \frac{\text{percent accuracy}}{100}$$

Equation 10 may be solved for t to determine the holding time.

The maximum value of

$$\frac{E_o}{HE_i}$$

at t_1 is

$$(18) \quad \left. \frac{E_o}{HE_i} \right|_{t_1} = 1 + k$$

where

$$(19) \quad k = \frac{Q^2}{2(B + AQ)}$$

The value of k is equal to the percent accuracy required divided by 100, i.e., $k=10^{-3}$ in FIG. 5. After the desired value of k is selected, C_5 may be varied to obtain this value. The maximum holding time may then be determined by

$$(20) \quad t_h = t_1 + \sqrt{\frac{2(k + 10^{-3})}{B + AQ}}$$

By making some valid assumptions, the approximate optimum value of C_5 may be determined from the following equation:

$$(21) \quad \frac{1}{C_5} \cong \frac{|k_1|}{k_2} \left[1 + \frac{k(k_3 + |k_1|k_4 + k_2 k_5)}{|k_1|k_2} + \sqrt{\frac{2k k_3}{|k_1|k_2}} \right]$$

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where

$$(22) \quad Q = k_1 = \frac{k_2}{C_5}$$

$$(23) \quad B = \frac{k_3}{C_5}$$

$$(24) \quad A = \frac{k_4}{C_5} + k_5$$

and k_{1-5} are not functions of C_5 and can be easily determined by combining the C_5 term in Equations 12 through 17. The assumptions referred to above are that k_2 , k_3 and k_4 are all of the same order of magnitude and all much less than k_1 which in turn is of the order of magnitude of k_5 and $k < 1$.

Once again, assuming that the resistors in FIG. 3 have a value of 1M and C_1 has a value of 1 μ f., C_5 may be calculated to be 0.180 μ f. for $k=10^{-3}$. The time at which the peak value occurs in the plot of FIG. 5 may be calculated to be $t_1=11.0$ ms. The maximum holding time for 0.1 percent accuracy may be calculated to be $t_h=26.6$ ms. The holding time then for a circuit operating in accordance with the plot of FIG. 5 is about twice as long as that for a circuit operating in accordance with FIG. 4.

Further improved holding can be obtained by feeding output E_o of the holding circuit in FIG. 3 to an amplifier 30 whose output is E_{o2} . Normally, this amplifier will provide a gain of $1/H$ (H is an attenuation constant and equals 3) for the chosen values of FIG. 3 to compensate for the loss in the holding circuit. In the plot of FIG. 4, the maximum value at t_1 was made equal to $1+10^{-3}$. If, however, the gain of the amplifier is reduced to

$$\frac{1-10^{-3}}{H}$$

and C_5 is calculated for $k=2 \times 10^{-3}$, a greater holding time may be obtained by using the output E_{o2} of amplifier 30. For this condition, $C_5=0.172$ μ f., the time of the peak $t_1=14.5$ ms., and the maximum holding time $t_h=29$ ms. Therefore, the holding time has been increased by about 3 ms. By increasing the holding time to this degree, the effect of the $\delta^3 t^3$ in Equation 5 may not be negligible and may effect the accuracy of the above value for t_h and, therefore, the 29 ms. value should be taken as an indication of order of magnitude.

As a practical matter, in practicing this invention C_5 may be calculated to obtain an approximate optimum value, and then a trimmer capacitor may be connected in parallel with C_5 and varied to obtain the best value of capacitance.

If we did not use the holding circuit of FIG. 3, but instead a simple 1 μ f. capacitor, this capacitor would discharge through the two parallel 1M resistors R_1 and R_4 . The time constant for the discharging capacitor would be 0.5 second and the holding time within 0.1 percent accuracy would be only 0.5 ms. Thus, the holding circuit of FIG. 3 increases the holding time a maximum of 58 times for the chosen values.

We have used numerical values in describing a specific embodiment of this invention, however, it should be stressed that very similar results can be obtained by using other values for the resistors and capacitors in accordance with the equations presented above.

As a practical matter, an output amplifier would normally be connected to the output of the holding circuit shown in FIG. 3. The resistors R_2 , R_3 , R_4 and R_5 act as a voltage divider and thus E_o will be only a fraction of E_1 . For example, with the previously discussed numerical values for the resistors, $E_o=1/3 E_1$. Therefore, the output amplifier is necessary to raise E_o back to the original input voltage level. An output amplifier will, however, be necessary in most applications in any event to match the input impedance of the following network connected to the holding circuit. It is then only necessary to increase

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the gain of the amplifier to 3 instead of 1 as when only an impedance match is necessary.

Since the holding circuit will have to work normally in repetitive cycles, it may be difficult to discharge C_5 completely. However, R_3 , R_4 and R_5 , serve as a voltage divider and, therefore, only a fraction of E_{50} will appear at the output terminals of the holding circuit. If, for example, we have an output voltage range of 10 mv. to 10 v. and a 0.1 percent accuracy is required, it can be calculated by Equation 4 that E_5 should be smaller than 30 mv. For other values of R_3 , R_4 and R_5 , the tolerable residual voltage across C_5 may be greater or smaller.

It is completely possible to use 10 percent tolerance circuit components since the final compensation can be achieved by selecting the correct value for C_5 . However, the actual value of resistors and capacitors should not change appreciably with time. An analysis of the change which can be tolerated may be made by the use of partial derivatives.

In order to obtain an order of magnitude for the effect of component variation with time, the case of FIG. 4 has been analyzed. In this case $Q=0$, $t_h=12.5$ ms., and for the assumed circuit components, the percentage change in the output voltage E_o becomes

$$(25) \quad \begin{aligned} (\text{Percent } E_o) = & .00975(\text{percent } R_1) - .6534(\text{percent } R_2) \\ & -.0238(\text{percent } R_3) + .0077(\text{percent } R_4) \\ & -.00195(\text{percent } R_5) \\ & + .0226(\text{percent } C_1) - .0164(\text{percent } C_5) \end{aligned}$$

It can be seen that the most critical parameter is R_2 . This is due to its effect on H , the attenuation of the holding circuit.

If it is assumed that all component variations are random and statistically independent and that the percentage value of the variable represents the standard deviation about the mean, the standard deviation of E_o about its mean can be obtained for small deviations by the sum of the square rule. When the following standard deviations are assumed

$$(26) \quad \begin{aligned} \text{Percent } R_1 = & 5 \\ \text{Percent } R_2 = & .1 \\ \text{Percent } R_3 = & .1 \\ \text{Percent } R_4 = & .1 \\ \text{Percent } R_5 = & 5 \\ \text{Percent } C_1 = & 1 \\ \text{Percent } C_5 = & 1 \end{aligned}$$

The result is

$$(27) \quad (\text{Percent } E_o) = .0866$$

Therefore, if the change "accuracies" of Equations 26 prevail, E_o will always be within its 0.1% limitation for small t and the holding time could be either increased or decreased from its mean of 12.5 ms.

If the "accuracies" of R_1 and R_2 were changed to 1% and .01%, respectively, the "accuracy" of E_o would improve to

$$(28) \quad (\text{Percent } E_o) = .0344$$

The switches S_1 and S_2 may be in the form of a transistor, electronic tube, cryogenic device or magnetic device. An actual test circuit incorporating transistor switches is shown in FIG. 6. TR-1 and TR-2 are NPN transistors corresponding respectively to switches S_1 and S_2 in FIG. 2. A square wave generator 32 supplies switching pulses to the bases of TR-1 and TR-2 in order to turn these transistors on and off. TR-1 is used to discharge C_1 whose charging and discharging times are both equal to 30 ms. TR-2 discharges C_5 after each holding cycle down to a voltage of 12 mv. within a time of about 80 μ s.

While there have been shown and described and pointed out the fundamental novel features of the invention as applied to the preferred embodiment, it will be understood that various omissions and substitutions and changes in

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the form and details of the device illustrated and in its operation may be made by those skilled in the art without departing from the spirit of the invention. It is the intention, therefore, to be limited only as indicated by the scope of the following claims.

What is claimed is:

1. A passive electrical analog holding circuit comprising a source of voltage, a first electrical energy storage means connected across said source, a pair of output terminals, an output circuit connected to said first storage means and across said output terminals, said output circuit including a second electrical energy storage means and a resistive impedance connected in series, means for disconnecting said source from said first storage means and for transferring the electrical energy stored in said first storage means through said resistive impedance to said second storage means so that the voltage developed across said output terminals is substantially proportional to the voltage of said source both before and after said source is disconnected from said first storage means.

2. A passive electrical analog holding circuit comprising a first capacitor, a pair of output terminals, an output circuit connected across said first capacitor and said output terminals, said output circuit including a second capacitor and a resistor connected in series, means for connecting an analog voltage to said first capacitor to charge said first capacitor and cause current to flow through said resistor, and switching means operative simultaneously to disconnect said analog voltage and connect said first capacitor to said second capacitor so that said first capacitor discharges through said resistor and into said second capacitor, whereby the voltage developed across said output terminals both before and after the operation of said switching means is proportional to said analog voltage.

3. An electrical analog holding circuit comprising a first capacitor, a first resistor connected to said first capacitor, an output circuit connected across said first resistor and said first capacitor, said output circuit including a second resistor and a second capacitor connected in series, a pair of output terminals connected across said output circuit, normally closed first switching means for connecting an analog voltage across said first capacitor, and normally closed second switching means for short circuiting said

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second capacitor so that when said first and second switching means open simultaneously, said first capacitor discharges through said second resistor and into said second capacitor whereby the voltage developed across said output circuit is substantially proportional to said analog voltage both before and after said first and second switching means are open.

4. An electrical analog holding circuit comprising a source of analog voltage, a first capacitor, normally closed first switching means connecting said source to one side of said capacitor, a first resistor having one end connected to said source and to said one side of said capacitor, an output circuit connected between the other end of said first resistor and the other side of said first capacitor, said output circuit including a second resistor and a second capacitor connected in series, a pair of output terminals connected across said output circuit, second normally closed switching means shunting said second capacitor, and means for simultaneously opening said first and second switching means to cause said first capacitor to discharge through said first and second resistors and into said second capacitor so that the voltage developed across said output terminals remains substantially proportional to said analog voltage even though said source is disconnected from said first capacitor.

5. An electrical analog holding circuit as defined in claim 4 wherein said second capacitor has a smaller value of capacitance than said first capacitor.

6. An electrical analog holding circuit as defined in claim 4 wherein said first and second switching means are transistors.

7. A passive electrical analog voltage circuit as defined in claim 1 wherein each of said first and second storage means includes a capacitor.

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UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,171,986

March 2, 1965

Raymond E. Bonner et al.

It is hereby certified that error appears in the above numbered patent requiring correction and that the said Letters Patent should read as corrected below.

Column 2, equation (1), for that portion of the equation reading

$$\int_e^{-\rho t} \quad \text{read} \quad \int_e^{-\rho \bar{t}}$$

column 3, equation (5), for that portion of the equation reading

$$=| \quad \text{read} \quad =1$$

same column 3, equation (6), for that portion of the equation reading

$$<| \quad \text{read} \quad <1$$

column 4, equation (20), for that portion of the equation reading

$$2(k+10^{-3}) \quad \text{read} \quad 2(k+10^{-3})$$

same column 4, equation (21), for that portion of the equation reading

$$[1+ \quad \text{read} \quad [1+$$

3,171,986

column 5, equation (22), the equation should appear as shown below instead of as in the patent:

$$Q \equiv k_1 + \frac{k_2}{C_5}$$

same column 5, line 44, for "effect" read -- affect --; column 6, equation (27), the equation should appear as shown below instead of as in the patent:

$$(\text{Percent } E_o) = .0866$$

Signed and sealed this 7th day of December 1965.

(SEAL)

Attest:

ERNEST W. SWIDER
Attesting Officer

EDWARD J. BRENNER
Commissioner of Patents