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(54) TIMING CIRCUITS

(71) We, ROBERT BOSCH GmbH., a German Company, of Postfach 50, 7 Stuttgart 1, Federal Republic of Germany, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to a timing circuit having time constants which may be predetermined by the charging and discharging times of a capacitor.

Such timing circuits are known and in fact there is associated with a capacitor either a discharging and a charging resistor or only a single resistor which is used for charging and discharging. If differing time constants are required which are predetermined by the charging and discharging time, usually several resistor-capacitor arrangements are used. In integrated circuits this has the disadvantage that capacitors are not integrable and therefore the integrated timing circuit component according to prior art has to be wired externally to several capacitors insofar as differing time constants are required.

In accordance with the present invention there is provided a timing circuit in which at least two charging resistors and at least two discharging resistors are associated with a common capacitor and in which electrical switches are provided for selectively completing charging and discharging circuits to and from said capacitor through such resistors, time constants of the timing circuit being determined by the charging and discharging times of the capacitor.

Control of the electrical switches is preferably effected in that comparators are connected to the capacitor, each comparator being associated with a charging and discharging system including a respective charging resistor and a respective discharging resistor, the output of each comparator being connected to the control input of a respective one of the electrical switches which is connected to said respective discharging resistor.

In order that one of the charging and discharging systems shall be a dominant system, at least two charging and discharging systems are connected to one another by a blocking logic element so that one system will block the other in particular in that the output of the comparator associated with the dominant system and the input of the dominant system itself are connected to the blocking logic element so that, during the charging and discharging phase of the dominant system, the systems may be blocked which are non-dominant and are connected to the output of the blocking logic.

The advantages of the invention are particularly that a single integrated circuit as a result of external wiring to resistors and a capacitor may be used for as many and as varied time functions as desired. Thus, for example, it is possible using such an integrated timing circuit in a motor vehicle to control both the windscreen wiper interval switching and the wipe-wash device of the windscreen wiper. Other possible uses in the motor vehicle are, for example, control of blinker units, of rear window heating, of the preliminary heating automatics in diesel engines and of the cold-start enrichment of fuel. A more economical and simpler control of time-controlled processes is made possible by a single standardized integrated timing circuit component which may be programmed for any use by external wiring to resistors.

The present invention is further described hereinafter, by way of example, with reference to the accompanying drawing which is a circuit diagram of a timing circuit in accordance with the invention.

On-and-off signals applied to two terminals 10, 11 for controlling two different time-controlled functions are applied through current-limiting resistors 12, 13 to two input terminals 14, 15 of an integrated timing circuit. The terminal 14 is connected to the control input of a first electrical switch 16 in the form of an NPN-transistor. The terminal 14 is also connected through the series connection of a first NOR-gate 17 with a

second NOR-gate 18 to the control input of a second electrical switch 19 also in the form of an NPN-transistor. The terminal 14 is also directly connected to an input of the second NOR-gate 18. The emitter of the first switching transistor 16 is connected by a first charging resistor 20 and a first discharging resistor 21 to the collector of the second switching transistor 19. A capacitor 22 is connected by one terminal to the junction between the two resistors 20, 21 and by its other terminal to earth. The switches 16, 19, the resistors 20, 21 and the capacitor 22 form a first charging-discharging system, i.e. an internal timer having a specific time constant or a time constant for the charging process and a time constant for the discharging process.

The terminal 15 is connected through the series connection of a first inverter 23 with a third NOR-gate 24 to the control input of a third electrical switch 25 also in the form of an NPN-transistor. The output of the first inverter 23 is connected by a second inverter 26 to the control input of a fourth electrical switch 27 also in the form of an NPN-transistor.

The control input, i.e. the base, of the control transistor 27 is connected to another input of the third NOR-gate 24. The emitter of the third switching transistor 25 is connected through the series connection of a second charging resistor 28 with a second discharging resistor 29 to the collector of the fourth switching transistor 27. The junction between the two resistors 28, 29 is also connected to the capacitor 22. The switching transistors 25, 27, the resistors 28, 29 and the capacitor 22 form a second charging-discharging system, i.e. a second internal timer having a specific time constant.

The common junction of the resistors 20, 21, 28, 29 is connected to an input of each of two comparators 30, 31. The output of the first comparator 30 is connected to a second input of the first NOR-gate 17 and the output of the second comparator 31 is connected to the control input of the fourth electrical switch 27. The output of the first comparator 30 is also connected by an OR-gate 32 to the control input of a fifth electrical switch 33 which also takes the form of an NPN-transistor. The positive pole 34 of a voltage source is connected to earth through the series connection of the solenoid of a relay 35 with the collector-to-emitter path of the switching transistor 33. Any other load may be provided instead of the relay 35.

For direct control of the relay 35 bypassing the timing circuit, a further input terminal 36 is connected to a second input of the OR-gate 32. For this purpose, an on-off signal on a terminal 37 is applied through a current-limiting resistor 38 to the input terminal 36.

The first comparator 30 is associated with the first charging-discharging system 16, 19, 20, 21, 22. This system is a dominant system, i.e. when there is an input signal at the terminal 10, any signal on the terminal 11 remains ineffective. For this purpose, the output of the second comparator 31 is connected by a fourth NOR-gate 39 to a third input of the OR-gate 32. Moreover, the output of the first inverter 23 is connected to a second input of the fourth NOR-gate 39. The output of the first NOR-gate 17 is connected to the input of the first inverter 23. The positive pole 34 of the voltage source is connected by another current-limiting resistor 40 and another input terminal 41 to the collectors of the switching transistors 16, 25. The emitters of the switching transistors 19, 27 are connected to earth.

To explain the mode of operation of the integrated timing circuit it is stated that the logic members used should be so constructed that at the simultaneous appearance of a 0-signal and a 1-signal at a point the 0-signal predominates. Logic elements for which the reverse is true could equally well be used. The logic circuit in this case would have to be somewhat modified but it is not difficult for an expert to achieve the corresponding logic functions using other logic switching elements. Using a Karnaugh diagram, the various switching possibilities may be indicated and selected at random. The terms 1-signal and 0-signal usual in digital technology are used respectively to denote a potential in the order of magnitude of the positive potential and a potential corresponding approximately to the earth potential.

As long as there is a 1-signal at the terminal 10 or the terminal 14 which is produced, for example, by a switch connected to the positive pole 34 of the voltage source, the first electrical switch 16 is opened and the capacitor 22 is charged through the first charging resistor 20. A discharge through the discharging resistor 21 and the second electrical switch 19 is not possible during this time since the second electrical switch 19 is blocked from the terminal 14 because of the second NOR-gate 18. If the 1-signal at the terminal 14 is completed and at the same time the upper threshold voltage of the first comparator 30 is attained or exceeded, the 1-signal at the output of the comparator 30 is applied through the two NOR-gates 17, 18 acting as inverters as a 1-signal to the control input of the second electrical switch 19 which is consequently closed and leads to the discharging of the capacitor 22 through the first discharging resistor 21 and the second electrical switch 19.

At the end of the 1-signal at the terminal

14, the first electrical switch 16 is blocked, thus preventing a further charging of the capacitor 22. If the voltage of the capacitor 22 drops below the value of the lower threshold voltage of the comparator 30, a 0-signal is again applied to the output of the comparator 30 and blocks the electrical switch 19 through the two NOR-gates 17, 18.

For the duration of the 1-signal at the output of the comparator 30 the fifth electrical switch 33 is closed through the OR-gate 32 and the relay 35 is actuated.

While there is a 1-signal at the terminal 14 or a 1-signal at the output of the comparator 30 there is a 0-signal at the output of the first NOR-gate 17. This 0-signal is converted by the first inverter 23 into a 1-signal and is applied to an input of the fourth NOR-gate 39 at whose output a 0-signal therefore is produced. This 0-signal at the output of the fourth NOR-gate 39 arises independently of whether there is a 0-signal or a 1-signal at the output of the second comparator 31. The influence of the second comparator 31 is therefore eliminated.

If there is a 1-signal at the terminals 11 and 15, the electrical switch 25 is closed through the first inverter 23 and the third NOR-gate 24, acting as an inverter, and the capacitor 22 is charged through the second charging resistor 28. The electrical switch 27 associated with the discharging resistor 29 is blocked at that instant since a 0-signal from the output of the second comparator 31 is applied to the control input of the electrical switch 27. The voltage on the capacitor 22 increases until the upper threshold voltage of the second comparator 31 is attained and a 1-signal appears at the latter's output. This 1-signal leads through the NOR-gate 24 to the blocking of the third electrical switch 25 and to the fourth electrical switch 27 becoming conducting. The capacitor 22 is discharged through the discharging resistor 29 until its voltage reaches or drops below the lower threshold voltage of the second comparator 31. Since a 0-signal is then applied again to the output of the second comparator 31, the third electrical switch 25 again becomes conducting and the fourth electrical switch 27 is blocked. This process is repeated as long as there is a 1-signal at the terminal 11 or at the terminal 15. Only when a 1-signal is applied to the terminal 10 or 14 or when there is a 1-signal at the output of the first comparator 30 owing to such a signal lying at the terminals 10, 14, is the 1-signal at the terminal 15 made ineffective by the 0-signal at the output of the first NOR-gate 17. An input signal at the terminal 10 therefore dominates an input signal at the terminal 11.

As already mentioned, during running of the first comparator 30, owing to a signal at the terminals 10, 14 the output of the second comparator 31 is blocked from the fifth electrical switch by the fourth NOR-gate 39. However, if there is a 0-signal at the terminals 10, 14 and a 1-signal at the terminals 11, 15, the fourth NOR-gate 39 is not blocked and signals at the output of the second comparator 31 control the fifth electrical switch 33. During this time a 0-signal remains at the output of the first comparator 30 since the upper threshold voltage of the first comparator 30 lies above the upper threshold voltage of the second comparator 31.

The described timing circuit may be fully integrated but the charging- and discharging resistors 20, 21, 28, 29 and the capacitor 22 are disposed externally as discrete components for external wiring and programming of the timing circuit. The current-limiting resistors 12, 13, 38, 40 and the relay 35 are similarly externally disposed. These current-limiting resistors 12, 13, 38, 40 do not have to be provided in every case and may—if the overall design allows—possibly be omitted. The supply voltage source is preferably a stabilized voltage which may have a safety circuit against excessive voltages to protect the integrated timing circuit. The components for the stabilized voltage source may of course also be combined with the timing circuit into a single integrated component. The timing circuit may naturally be arbitrarily extended, i.e. other charging-discharging systems comprising a charging- and a discharging resistor and two associated electrical switches may be additionally included in the described arrangement. A third comparator would also have to be provided. The wiring of the other charging-discharging systems by means of logic switching elements may be effected in a similar manner and connection lines for creating dominant systems could be provided if desired.

The arrangement shown in the drawing is particularly suitable for the time control of the windscreen wiper motor of a motor vehicle. For this purpose, the signal for the wipe-wash operation is applied to the terminal 10, i.e. on the strength of a signal the spraying system is actuated and—conditioned by the delay as a result of the charging process of the capacitor 22 through the resistor 20—the windscreen wiper motor is then started. The signal for the interval operation of the windscreen wiper may then be applied to the terminal 11.

If several loads 35 and therefore several associated electrical switches 33 are to be provided, the outputs of the relevant comparators may either be connected directly to the control inputs of the relevant electrical switches or several comparators may be connected through gates to the respective

control input of the relevant electrical switch.

Connection of the outputs of comparators may be effected not through the OR-gate—as shown in the drawing—but alternatively through an AND-gate which optionally has inverting and non-inverting inputs. In this manner, the switch 33 is only triggered when there is a specific output signal combination of comparators. Furthermore, if a greater number of comparators or charging-discharging systems is provided, part of the comparator output may be interconnected through AND-logics and another part through OR-logics and individual comparators may also be associated with both logic connections.

WHAT WE CLAIM IS:—

1. A timing circuit in which at least two charging resistors and at least two discharging resistors are associated with a common capacitor and in which electrical switches are provided for selectively completing charging and discharging circuits to and from said capacitor through such resistors, time constants of the timing circuit being determined by the charging and discharging times of the capacitor.

2. A timing circuit as claimed in claim 1, which is an integrated circuit apart from the charging and discharging resistors and the capacitor.

3. A timing circuit as claimed in claim 1 or 2, which has a separate input associated with each charging resistor.

4. A timing circuit as claimed in any preceding claim, which includes comparators connected to the capacitor, each comparator being associated with a charging and discharging system including a respective charging resistor and a respective discharging resistor, and in which the output of each comparator is connected to the control input of a respective one of the electrical switches which is connected to said respective discharging resistor.

5. A timing circuit as claimed in claim 4, in which the input of at least one of the charging and discharging systems is connected both to the control input of that electrical switch which is connected to the respective charging resistor, and through a logic element to the control input of that electrical switch which is connected to the respective discharging resistor, such logic element blocking the discharging switch when an input signal is applied to said one charging and discharging system.

6. A timing circuit as claimed in claim 4 or 5, in which the comparator associated with at least one of the charging and discharging systems is connected to the control inputs of the respective switches to form a multivibrator which is triggered by means of an input signal applied to the input of such charging and discharging system.

7. A timing circuit as claimed in claim 4, 5 or 6, in which at least two charging and discharging systems are connected to one another by a blocking logic element for blocking one system by means of the other system.

8. A timing circuit as claimed in claim 7, in which the output of the comparator associated with one dominant system and the input of the dominant system itself are connected to the blocking logic element so that, during the charging and discharging phase of the dominant system, the non-dominant system connected to the output of the blocking logic element may be blocked.

9. A timing circuit as claimed in any of claims 4 to 8, in which the outputs of at least two comparators are connected by a logic element to the control input of a further electrical switch which serves for controlling loads, and the further electrical switch is alternatively controllable by the comparators by virtue of each logic element.

10. A timing circuit as claimed in claim 9 when appendant to claim 7 or 8, in which a further logic element is connected between the output of the comparator of the non-dominant charging and discharging system, and the previously mentioned logic element, the control input of said further logic element being connected to a blocking connection line from the dominant system.

11. A timing circuit as claimed in any of claims 4 to 8, in which the outputs of at least two comparators are connected through a logic element to the control input of a further electrical switch which serves for, controlling loads, and the further electrical switch is only actuable at specific output signal combinations of the comparators by virtue of such logic element.

12. A timing circuit as claimed in any of claims 9 to 11, in which a bypass input by passing the charging and discharging systems, is connected at least indirectly to the control input of the further electrical switch.

13. A timing circuit as claimed in claim 12 in which said bypass input is connected to an input of said further logic element.

14. A timing circuit constructed and adapted to operate substantially as hereinbefore described with reference to and as illustrated in the accompanying drawing.

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1576058 COMPLETE SPECIFICATION

1 SHEET

This drawing is a reproduction of the Original on a reduced scale